International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 02 Issue 03
March 2015

ZVS based DC/AC Modular Hybrid converter for HVAC Applications

Chilaka Udaya Kumar1, M Lakshminarayana[2], Kurivindala Ravi[3], Medi Murali Krishna[4]

[1]Assistant Professor, Department of EEE, Anubose Institute of Technology, Paloncha , Telangana, INDIA
[2]M.Tech (Electrical Power Systems)
[3]Assistant Professor, Department of EEE, Sreenidhi Institute of Science Technology Hyderabad, Telangana, INDIA
[4]Assistant Professor, Department of EEE, Adams Engineering College, Paloncha, Telangana, INDIA

Abstract: The basic configurations of the voltage-mode resonant switches are presented. The circuit's operating principles are described using a voltage-mode quasi-resonant boost converter. This paper proposes a zero voltage switching (ZVS) technique for bidirectional dc/dc converters. The dc/dc unit considered consists of two distinct bidirectional dc/dc cells paralleled at both input and output and whose two input bridges are coupled by means of passive inductive branches. In this topology, the NPC is used to supply the active power while the HBs operate as series active filters, improving the voltage waveform quality by only handling reactive power.

I. INTRODUCTION

Electronic power processing technology has evolved around two fundamentally different circuit schemes: duty-cycle modulation, commonly known as pulse width modulation (PWM), and resonance. The PWM technique processes power by interrupting the power flow and controlling the duty cycle, thus, resulting in pulsating current and voltage waveforms. The resonant technique processes power in a sinusoidal form. Due to circuit simplicity and ease of control, the PWM technique has been used predominantly in today's power electronics industries, particularly, in low-power power supply applications, and is quickly becoming a mature technology. Resonant technology, although well established in high-power SCR motor drives and uninterrupted power supplies, has not been widely used in low-power dc/dc converter applications due to its circuit complexity.

With available devices and circuit technologies, PWM converters have been designed to operate generally at 30- 50-kHz switching frequency. In this frequency range, the equipment is deemed optimal in weight, size, efficiency, reliability and cost. In certain applications where high power density is of primary concern, the conversion frequency has been chosen as high as several hundred kilohertz. With the advent of power MOSFET'S, devices switching speed as high as tens of megahertz is possible. Accompanying the high switching frequency, however, are two major difficulties with the semiconductor devices, namely high switching stress and switching loss. For a given switching converter, the presence of leakage inductances in the transformer and junction capacitances in semiconductor devices causes the power devices to operate in inductive turn-off and capacitive turn-on. As the semiconductor device switches off an inductive load, voltage spikes are induced by the sharp di/dt across the leakage inductances, On the other hand, when the switch turns on at high voltage level, the energy stored in the device's output capacitances, 0.5 CV2, is trapped and dissipated inside the device. Furthermore, tum-on high voltage levels induces a severe switching noise known as the Miller effect which is coupled into the drive circuit, leading to significant noise and instability.

The paper presents the concept of Zero Current Switching Technique and Zero Voltage Switching Technique in detail. For the zero current switching technique, the objective is to use auxiliary LC resonant elements to shape the switching device's current waveform at on-time in order to create a zero-current condition for the device to turn off. The dual of the above statement is to use auxiliary LC resonant elements to shape the switching device's voltage waveform at off-time in order to create a zero-voltage condition for the device to turn on. This latter statement describes the principle of zero voltage switching. The recognition of the duality relationship between these two techniques leads to the development of the concept of voltage-mode resonant switches and a new family of converters operating under the zero voltage switching principle.

II. ZERO VOLTAGE SWITCHING

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of

time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.

Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converters.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (Co& has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch.

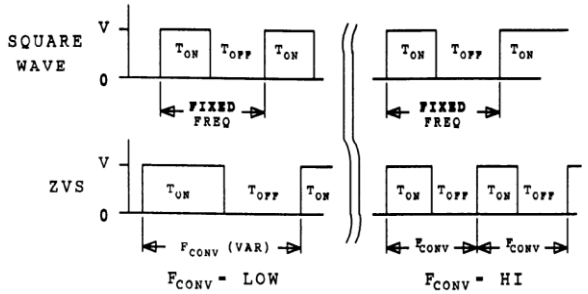

Fig 1: Zero Voltage Switching vs. Conventional Square Wave

Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V& equals zero.

The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few.

III. HYBRID CONFIGURATION

The considered hybrid topology is composed by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase. The power circuit is illustrated in Fig. 2, with only the H-bridge of phase a shown in detail. For testing as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, arranged in a twelve-pulse configuration. The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy detailed in Section III. In the hybrid topology considered, the NPC inverter provides the total active power flow.

For high-power medium voltage NPC, there are advantages to using latching devices such IGCTs rather than IGBTs, due to their lower losses and higher voltage blocking capability imposing a restriction on the switching frequency. In this work, an NPC operating at a low switching frequency (of 250Hz) is considered. In contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of IGBT.

The proposed converter, shown in Fig.2, can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, achieved by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC Bridge is to be modulated at a low switching frequency, as proposed in this work, the second interpretation would seem to be more appropriate to devise a control algorithm, leading to the following two design challenges:

To determine the lowest value of H-bridge dc-link voltage (VH) that achieves adequate voltage harmonic compensation.

To devise a control algorithm that ensures that the floating dc-links are properly regulated at this value.

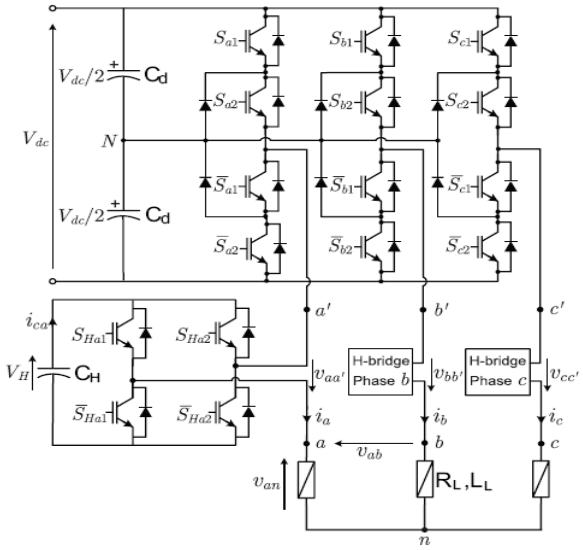

Fig 2: Hybrid topology

IV. NEUTRAL POINT CLAMPED (NPC) CONNECTION

Three-level SHE is an established and well documented modulation strategy. A qualitative phase output voltage waveform is presented considering a 5-angle realization,so five degrees of freedom are available. This enables theamplitude of the fundamental component to be controlled andfour harmonics to be eliminated. Since a three-phase systemis considered, the triple harmonics are eliminated at the loadby connection, and hence, they do not require elimination bythe modulation pulse pattern.

The addition of the series H-bridge results in more levels being added on the output voltage waveform of the converter va_N. In particular, if the value of VH is smaller than Vdc/4, no redundant switching states are created and the output voltage waveform of the converter will have the maximum number of levels (nine), generating similar waveforms to those achieved by cascade H-bridge inverters with unequal dc sources.

The voltage distortion remaining from the SHE modulation of the NPC converter can be computed as the difference from the NPC output voltage and the reference value. The NPC output voltage is calculated including the interaction between the phases, i.e. excluding the common mode voltage from the resulting waveform.

On the other hand, considering that the NPC converter is modulated using the synchronous SHE method, the H-bridge should be modulated to compensate for the distortion created by the modulation of the NPC. This is done at a higher frequency using carrier based unipolar PWM.

When deciding the value for the dc-link voltage of the H-bridges VH, a sufficiently large value should be selected to achieve appropriate compensation of the remaining distortion, while at the same time the value of VH should be kept as low as possible in order to minimize the additional switching losses.

V. CONTROL SYSTEM

During operation, the fundamental load current is generated by the NPC converter. In order to synchronize the voltage reference vaa(f1) with this current, a phase lock loop (PLL) algorithm is used, which guarantees zero phase shift between both signals and therefore maximizes the active power transfer to the capacitors for any power factor. The magnitude of this voltage reference is obtained from the DC-link voltage controller shown in Fig. 3. For the design of this voltage controller, the dynamic model (2) of the dc-link voltage vHa as a function of ^vaa0 is used. Each series H-bridge converter is independently controlled by two complementary references, as shown in Fig. 3. The first reference vaa(fn) corresponds to the inverse of the harmonics remaining from the SHE pulse pattern, calculated as described in the previous section from the difference between the NPC pulsed voltage pattern and its sinusoidal voltage reference. This calculation provides a fast and straightforward distortion estimation allowing for simple feed-forward compensation.

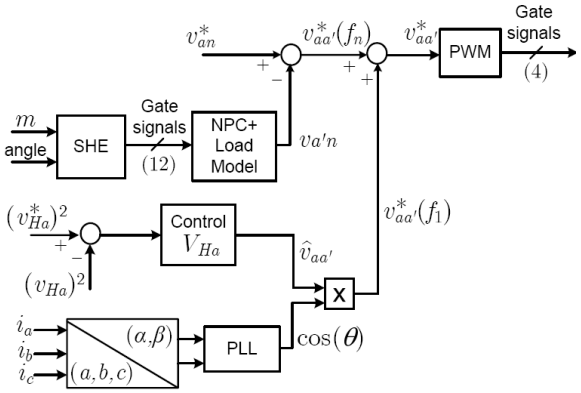

Fig 3: Phase-A control diagram

It is important to note that, in applications with low frequency switching patterns, such as the SHE modulation, the use of direct synchronous sampling of the currents is not adequate to obtain the fundamental current because the switching harmonics do not cross zero at regular intervals. Instead, observers are needed to extract the fundamental current values [34] otherwise complex nonlinear control schemes are required [35]. In the present work, this problem is overcome by the compensating effect of the series connected H-bridges, which moves the spectra from the non-eliminated SHE harmonics to the high frequency H-bridge carrier band. This effectively simplifies the outer load current control loop design, resulting in a standard dq frame linear current regulator as shown in Fig. 4.

For good dynamic performance, an outer load current loop can be implemented as shown in Fig. 4. As low order harmonics are compensated by the H-bridges, the current can be synchronously sampled with the H-bridge carrier, providing a good estimation of its fundamental value. Moreover, as a high sampling frequency is used, a high current bandwidth can be achieved.

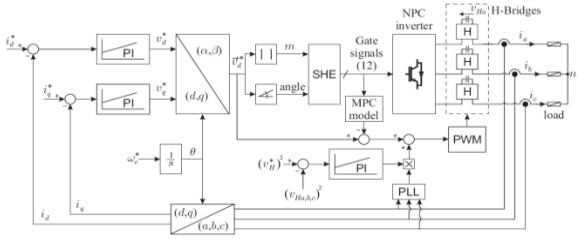

Fig 4: Current control loop for the proposed topology

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 02 Issue 03
March 2015

In regenerative operation, such as active front end applications for regenerative drives, the power flow needs to be controlled bidirectional. This is possible due to the interaction between the converter and load voltages through the grid impedance, usually an inductive filter.

VI. SIMULATION RESULTS

This section presents results to ascertain converter's performance under closed loop conditions. First, the converter is run without the use of the series H-bridges. The series H-bridges have compensated for the output distortion and enabled the use of a highly dynamic closed loop current control, without introducing additional commutation in the NPC Bridge. The main objective of current waveform improvement has been achieved; thanks to the additional voltage levels introduced by the series connected H-Bridges, without the need for extra DC-link power supplies.

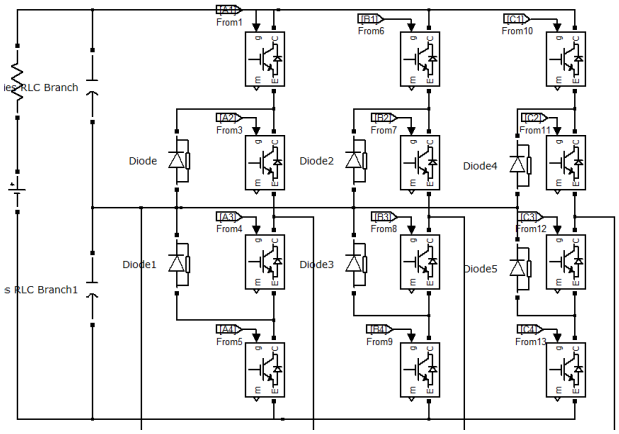

Fig 5: Neutral point clamped converter

During the transient however, small oscillations are presentin the currents due to the limited compensation capability ofthe H-bridges, which is a result of their low voltage and tothe limited amount of energy stored on them. Nevertheless,this additional oscillation decreases rapidly once the NPCstabilizes and reaches a quasi-steady state.

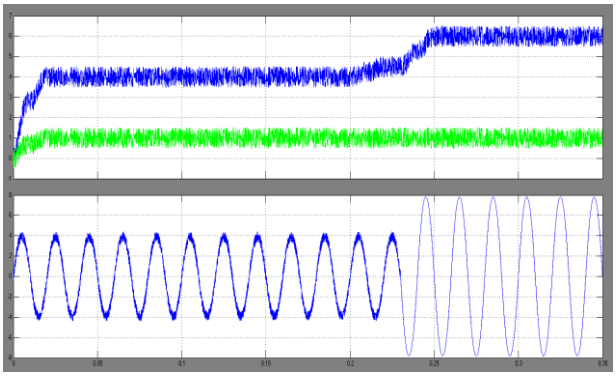

Fig 6: Closed loop current response: a) Measured currents in the synchronous frame d/q; b) Phase current.

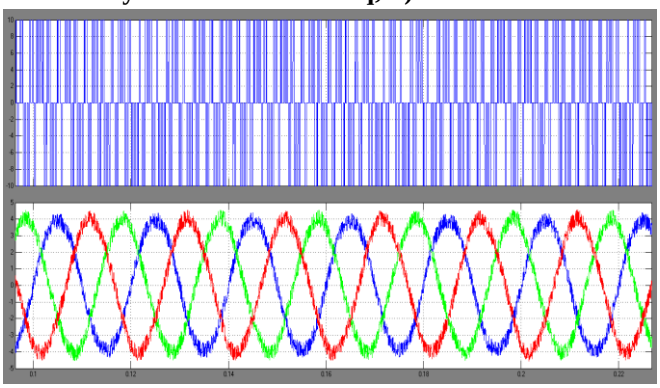

Fig 7: Voltage during current step: NPC voltage response; Total load phase voltage

VII. CONCLUSION

The addition of the H-bridge series activefilter or additional converter stage is not intended to increasethe power rating of the overall converter. Rather, the maingoal is to improve, in a controllable or active way, thepower quality of the NPC Bridge which may have a relativelylow switching frequency.This paper presents the series connection of a SHEmodulatedNPC and H-bridge multilevel inverter with a novelcontrol scheme to control the floating voltage source of theH-bridge stage.The proposed series H-bridge filter control scheme can beused either as a grid or load interface, depending on whetherthe NPC converter is used as an AFE or inverter respectively.Both possibilities can be combined if used in a back to backconfiguration.

REFERENCES

[1] J. Rodr´ıguez, S. Bernet, B. Wu, J. Pontt and S. Kouro, "Multilevelvoltage-source-converter topologies for industrial medium-voltagedrives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec.2007.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu,J. Rodr´ıguez, M. P´erez and J. Le´on,"Recent Advances and IndustrialApplications of Multilevel Converters," IEEE Trans. Ind. Electron.,vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] J.S. Lai and F.Z. Peng, "Multilevel converters-A new breed of powerconverters," IEEE Trans. Ind. Applicat., vol. 32, no. 2, pp. 509–517,May/Jun. 1996.

[4] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications,"Eur. Power Electron. J., vol. 2, no. 1, pp. 45–50, Mar. 1992.

[5] T. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob andM. Nahrstaedt, "Multicell converters: Basic concepts and

industry applications,"IEEE Trans. Ind. Electron., vol. 49, no. 5,
pp. 955–964, Oct.2002.

Author Details:

CHILAKA UDAYA KUMAR
Assistant Professor
Department of EEE
Anubose Institute of Technology
Paloncha , Telangana, INDIA

M LAKSHMINARAYANA
M.Tech (Electrical Power Systems)

KURIVINDALA RAVI
Assistant Professor
Department Of EEE
Sreenidhi Institute of Science Technology
Hyderabad, Telangana, INDIA

MEDI MURALI KRISHNA
Assistant Professor
Department of EEE
Adams Engineering College
Paloncha, Telangana, INDIA