A Future Technology for Enhanced Operation in Flip-Flop

Sujeet Kumar & Ashish Kumar Gupta
Department of Information and technology Dronacharya College of Engineering Gurgaon-122001, India
Email: sujeet.16939@ggnindia.dronacharya.info; Email: ashish.16907@ggnindia.dronacharya.info

ABSTRACT
In this paper a new technique is proposed based on the comparison between Conventional Transistorized Flip-flop and Data transition Look ahead D flip flop here we are checking the working of DLDFF and the conventional D Flip-flop after that we are analyzing the characteristic comparison using power & area constraints after that we are proposing a Negative Edge triggered flip-flop named as Switching Transistor based D Flip Flop (STDFF) with reduced number of transistors which will reduce the overall power area as well as delay. The simulations are done using Microwind & DSCH analysis software tools and the result between all those types are listed below. Our proposed system simulations are done under 50nm technology and the results are tabulated below. In that our proposed system is showing better output than the other flip-flops compared here.

Keywords:

Flip-flop; Low Power; Edge triggered

I.INTRODUCTION:

In electronics, a **flip-flop** or **latch** is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of *state*, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variablytimed input signals to some reference timing signal.

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edgetriggered); the simple ones are commonly called latches. The word *latch* is mainly used for storage elements, while clocked devices are described as *flip-flops*

D-flip-flop

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops. By setting S = R = 0, the flipflop can be used as described above.

The flip-flops are very useful, as they form the basis for shift registers, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is that some flipflops have a "reset" signal input, which will reset Q

(to zero), and may be either asynchronous or synchronous with the clock.
The above circuit shifts the contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

Types of D Flip-Flops
a. Classical Negative-edge-triggered D flipflop
b. Master–slave pulse-triggered D flip-flop
c. Edge-triggered dynamic D storage element

a. Conventional Low Power D Flip-flop
Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flipflops, have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes. In a conventional D Flip Flop shown in Figure 2, the clock signal always flows into the D flip-flop irrespective of whether the input changes or not. Part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power.

The gatingfunction is derived within the flip flop without any external control signal. The external clock signal of the flip-flop still switches. But, the clock signalflowing into the flip flop is deactivated when thereare no data transitions.

Generally flip- flop finds its best application in the counters. Counters can be classified as synchronous and asynchronous counters based on the application of clock to the flip-flops. A synchronous counter is clocked by a single clock for all the stages and the output for each stage changes at the same time.

I. Our Proposed Negative Edge Triggered Flip-Flop Design (STDFF)
Edge-triggered flip-flops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. A dual pulse clock generator is needed to generate pulses at both rising and falling edges of a lowswing clock. This Particular clock pulse is used to switch the ground of the flip-flop circuit. This ground will be utilized by the NMOS and PMOS connected directly to the D input of the circuit.

By using the Transistor switching logic only we are designing this circuit so it will be consuming only less power when compared to all other circuits. As well as we are having only 8 Transistors including the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption.
The input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it's a negligible amount only. Those delays can be further reduced by reducing the sizes of the transistor we are using in this circuit. Or by reducing the nano meter technology also we can reduce the constraints.

II. Tabulation

Power & Area Comparison Table

Type Power	Power Consumption	Area Consumption
Consumption	1.686uW	252um^2
Area Consumption	2.634uW	270um^2
Conventional D Flip-Flop	0.384uW	162um^2

Thus the Proposed Switching Transistor Based D Flip-flop design shows much less power & Area constraints than the Existing two Flip-Flop designs.

Figures

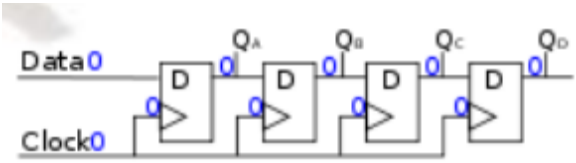

Figure 1 SIPO(shift register)

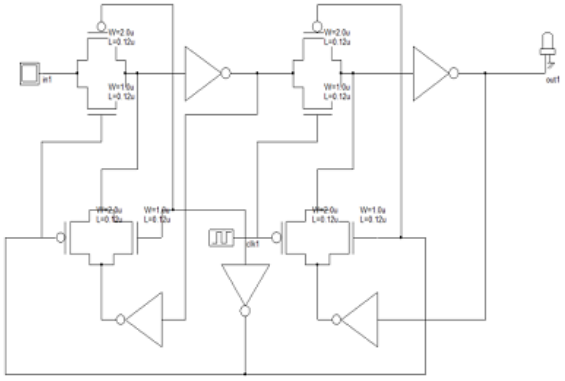

Figure 2.conventional D flip flop design

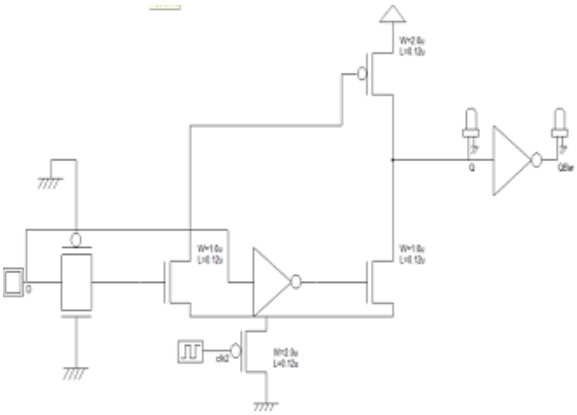

Figure 3 negative edge trigger flip flop

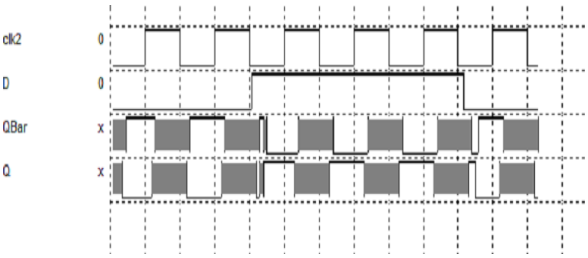

Figure 4 waveform of negative edge trigger flip flop

III.CONCLUSION:

In this Paper we proposed a new D flip flop design which is named as Switching Transistor Based D Flip Flop (STDFF). The Proposed system shows 85% Power improvement than the Existing Data Transition look ahead D Flip-Flop and it shows an improvement of 40% in area constraints. Thus our proposed system is having very less power and area constraints which will lead to improvement in the case implementation in future mobile devices. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced.

VII.REFERENCE:

[1] *M. Nogawa and Y.Ohtomo, "A Data-Transition Look-Ahead DFF circuit for Statistical Reduction in power consumption," IEEE J. Solid State Circuits, Vol. 33, pp.702–706, May, 1998.*

[2] H. Jacobson, P. Bose, Z. Hu, A. Buyuktosunoglu, V. Zyuban, R. Eickemeyer, L. Eisen, J. Griswell, D. Logan, B. Sinharoy, and J. Tendler, "Stretching the limits of clock-gating efficiency in server lass processors," in Proc. Int. Symp. HighPerform Compute. Archit., pp. 238–242, Feb. 2005.

[3] M.R.Stan, A.F.Tenca , and M.D. Ercegovac , "Long and fast up/down Counter ," IEEE Trans .Comput.,vol.47,no.7,pp.722–735, Jul.1998.

[4] N. H .E .Weste and D .Harris, CMOS VLSI Design. Reading, MA Pearson Education, Inc., 2005.

[5] J. M. Labaey and M. Pedram, Low Power Design Methodologies. Norwell, MA: Kluwer, ch.3, 1996.

[6] H. Kawaguchi and T. Sakurai, "A reduced clockswing flip-flop (RCSFF) for 63% power reduction," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 807–811, May 1998.

[7] A. Chandrakasan, W. Bowhill, and F. Fox, Design of High-Performance Microprocessor Circuits, 1st ed. Piscataway, NJ: IEEE Press, 2001.

[8] G. Gerosa, "A 2.2W, 80 MHz superscalar RISC microprocessor," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1440–1454, Dec. 1994.

[9] B. Nikolic, V. G. Oklobzija, V. Stojanovic, W. Jia, J. K. Chiu, and M. M. Leung, "Improved senseamplifier-based flip-flop: Design and measurements," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876–883, Jun. 2000.

[10] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in ISSCC Dig., Feb. 1996, pp. 138–139.

[11] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R.Wang, A. Mehta, Heald, and G. Yee, "Semi-dynamic and dynamic flip-flops with embedded logic," in Symp. VLSI Circuits, Dig. Tech. Papers, Jun. 1998, pp. 108–109.

[12] D. Markovic, B. Nikolic, and R. Brodersen, "Analysis and design of low-energy flip-flops," in Proc. Int. Symp. Low Power Electron. Des. ,Huntington Beach, CA, Aug. 2001, pp. 52–55.

[13] J. Tschanz, Y. Ye, L. Wei, V. Govindarajulu, N. Borkar, S. Burns, T. Karnik, S. Borkar, and V. De, "Design optimizations of a high performance microprocessor using combinations of dual-Vt allocation and transistor sizing," in IEEE Symp. VLSI Circuits, Dig. Tech. Papers, Jun. 2002, pp. 218–219.

[14] J. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits. Englewood Cliffs, NJ: Prentice-Hall, 2003.

[15] Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, "A 1-V high-speed MTCMOS circuit scheme for power-down application circuits," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 861–869, Jun. 1997.

[16] T. Sakurai, "Low –power CMOS design through Vth control and lowswing circuits," in Proc. ISLPED, 1997, pp. 1–6.

[17] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and highperformance systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[18] D. A. Hodges, H. G. Jackson, and R. A. Saleh, Analysis and Design of Digital Integrated Circuits, 3rd ed. New York: McGraw-Hill, 2004.
[19] V. G. Oklobdzija, "Clocking in multi-GHz environment," in Proc. 23rd IEEE Int. Conf. Microelectron., 2002, vol. 2, pp. 561–568.

[20] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low power system," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999

.
[21] N.Weste and D. Harris, CMOS VLSI Design.