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Implementation of Islanding Detection Using Phase-Locked Loops in Three-Phase Electrical Grid-Interface Power Convertors

Mahesh Thati & Mahesh Jonnala
[1]Assistant Professor, Dept of EEE, Institute of Aeronautical Engineering college, Dundigal, Hyderabad.
E-mail:maheshthati216@gmail.com
[2]Masters in Power Electronic Systems from Osmania University, Hyderabad.
E-mail:mahesh.vikram023@gmail.com

ABSTRACT:*In order to encounter the necessities for gridinterconnection, it is essential that the control of DistributedPower Generation systems (DPGSs) should be improved.Therefore, grid synchronization algorithms play a vital rolefor Distributed Power Generation Systems (DPGSs).Phase locked loop and synchronization techniques are one of the most important issues for operating grid-interfaced converters inpractical applications, which involve Distributed Power Generation Systems, Flexible AC Transmission Systems (FACTS), and High Voltage DirectCurrent (HVDC) Transmission, and so on.This paper proposes a systematic PLL modeling anddesign approach to evaluate different frequency-based islandingdetection methods. Two different types of PLL-based islandingdetection solution are discussed, accounting for a majority ofthe existing methods. The first method is to modify the PLL toconstantly move the stable equilibrium point. The second methodis to modify the PLL small-signal characteristics to achieve amonotonic instability behavior under the islanded conditions.The design procedures of these methods are presented using theproposed PLL modeling approach.*

KEYWORDS-Converter stability, distributed generation (DG),islanding detection, phase-locked loop (PLL).

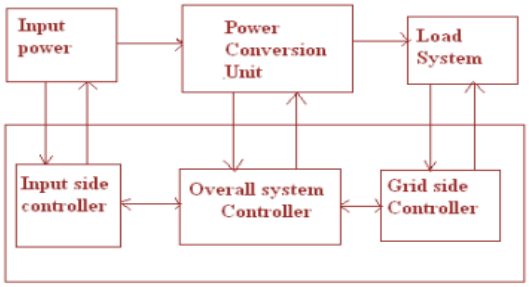
I. INTRODUCTION

Renewable energy resources are being widely used now adays for power generation. Three phase inverterimplemented in the unified control strategy is effective andgives the better inductor current [1]. Distributed generation(DG) is emerging as a viable alternative when renewable ornonconventional energy resources are available, such as windturbines, photovoltaic arrays, fuel cells, micro turbines [2], [4].

Most of these resources are connected to the utility throughpower electronic interfacing converters, i.e., three-phaseinverter. Moreover, DG is a suitable form to offer high reliableelectrical power supply, as it is able to operate either in thegrid-tied mode or in the islanded mode [3]. In the grid-tiedoperation, DG deliveries power to the utility and the localcritical load. Upon the occurrence of utility outage, theislanding is formed. Under this circumstance, the DG must betripped and cease to energize the portion of utility as soon aspossible according to IEEE Standard 929-2000 [5]. However,in order to improve the power reliability of some local criticalload, the DG should disconnect to the utility and continue tofeed the local criticalload [6]. The load voltage is key issue of these two operationmodes, because it is fixed by the utility in the grid-tiedoperation, and formed by the DG in the islanded mode,respectively. Therefore, upon the happening of lonely i.e.,islanding, DG must take over the load voltage as soon aspossible, in order to reduce the transient in the load voltage.And this issue brings a challenge for the operation of DG.Droop-based control is used widely for the power sharing ofparallel inverters [12], [13], which is called as voltage modecontrol in this paper, and it can also be applied to DG torealize the power sharing between DG and utility in the gridtied mode [14]. In this situation, the inverter is alwaysregulated as a voltage source by the voltage loop, and thequality of the load voltage can be guaranteed during thetransition of operation modes. However, the limitation of thisapproach is that the dynamic performance is poor, because thebandwidth of the external power loop, realizing droop control,is much lower than the voltage loop. Moreover, the gridcurrent is not controlled directly, and the issue of the inrushgrid current during the transition from the islanded mode tothe grid-tied mode always exists, even though phase lockedloop (PLL) and the virtual inductance are adopted. In thehybrid voltage and current mode control, there is a need toswitch the controller when the operation mode of DG ischanged. During the interval from the occurrence of utilityoutage and switching the controller to voltage mode, the loadvoltage is neither fixed by the utility, nor regulated by the DG,and the length of the time interval is determined by theislanding detection process.

A Microgrid or aportion of the power grid can be isolated from grid.However, the synchronization of

microgrids that operatewith multiple distributed generators (DGs) and loadscannot be controlled by a traditional synchronizer. It isnecessary to control multiple distributed generators andenergy storage systems in a coordinated way for themicrogrid synchronization. Power converter system can beoperated in islanded or standalone mode. In idealcondition, the output voltage parameters like amplitude,frequency and phase cannot be controlled for a gridtogether where multiple DGs are working in parallel;whereas the same parameters for standalone inverter to beconnected to grid can be controlled by means of the variouscontrol strategies [1].



General structure of distributed powersystem [1]

Therefore, the main issue in thisapproach is that it makes the quality of the load voltageheavily reliant on the speed and accuracy of the islandingdetection method [7]-[11].Therefore, it is necessaryand also our intention to investigate the inherent mechanismand the converter output frequency dynamic behaviors usinga systematic approach, which can be eventually applied tomultiple-inverter conditions.This paper is dedicated to the modeling and design procedures for frequency-based islanding detection.

The Inverter which working in standalone modeand is ready for synchronization to go for grid connectedmode, has to closely track the grid frequency [2]. Normallygrid frequency is varying according to load variations [3].Any mismatch on frequency may lead to generateunwanted circulating currents and may lead to damageelectronic devices. In this regard use of PLL is widelypreferred technique that enables tracking the grid frequency[4].Various techniques of synchronization of theinverter based on the Phase Locked Loop (PLL) aredescribed in the second section named Methodology.Different issues and solutions related to different PLLmethods are also described in it.

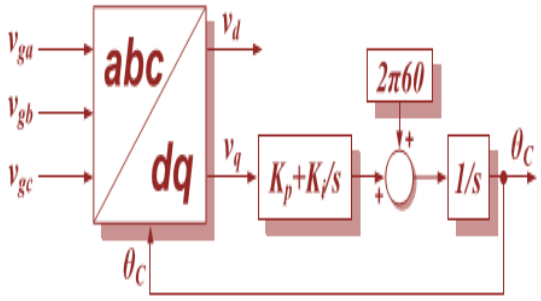


Fig. 1. Synchronous reference frame PLL linear model.

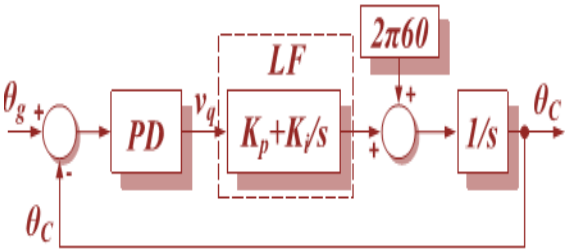


Fig. 2.Typical PLL linear model.

Two typesof PLL-based islanding detection methods will be discussedand compared with the typical PLL. Figs. 1 and 2 show thetypical SRF PLL structure and its linear model. The closedloop response is shown in (1), where the phase-detectorgainkPD equals the input ac voltage amplitude V_g.

II. ISLANDING DETECTION BASED ON PLLLARGE-SIGNAL STABILITY

Fig. 3 shows a three-phase power converter system whereZ_L and Z_g are the paralleled RLC local load and gridimpedances, respectively. The islanding event occurswhenthe point-of-common-coupling (PCC) switch opens. I_c is theinjection current amplitude of the inverter.The modeling of PLL frequency behavior at the islandedcondition was presented in [5]. In most cases,the islanding events would be effectively detected by directlymonitoring the PLL output frequency. However, for the paralleled RLC load with 60 Hz resonant frequency, the PLLoutput frequency will stay at the resonant frequency and thesystem cannot detect the islanding event. Therefore, the PLL orinternal control loops are usually modified to detect islandingunder such a loading condition.

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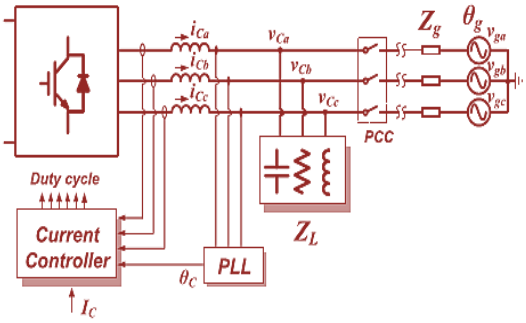

Fig. 3.Three-phase grid-interface power converter system.

The nonlinear PLL modelunder the islanded condition is shown in Fig. 4. Under theislanded condition, the PLL still tracks the inverter terminalvoltage produced by the inverter's current flowing to Z_L.Therefore, there is a self-synchronization loop shown in themodel.

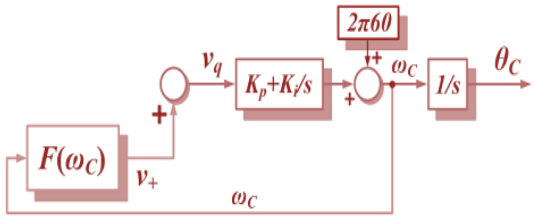

Fig. 4.SRF PLL model under the islanded condition.

This nonlinear PLL model can be linearized around the linefrequency to obtain the small-signal model [5], as shown in Fig. 5. I_cR_L is considered as k_{PD}.

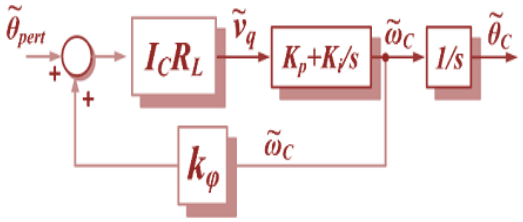

Fig.5. Linearized small-signal PLL model under islanded condition.

If the equilibrium point changes, the PLL output will automatically react to this change. Therefore, many islanding-detectionmethods are proposed to actively perturb the equilibrium point.Fig. 6 shows an example of PLL-based islanding detectionusing such a way.An additional large-signal feedback loop is introduced andmultiplied by a gain k_{pt} (a 0.5 or 1 Hz small triangular signalbetween 0 and k_{max}). This additional feedback loop constantlyshifts the equivalent resonant frequency. Thus, the PLL outputfrequency will keep moving all the time.As shown in Fig. 7, the output frequency will follow theinput injection signal k_{pt}. Eventually, the average value ω_{av}ofthe PLL output will stay lower than 60 Hz to ensure F = 0.

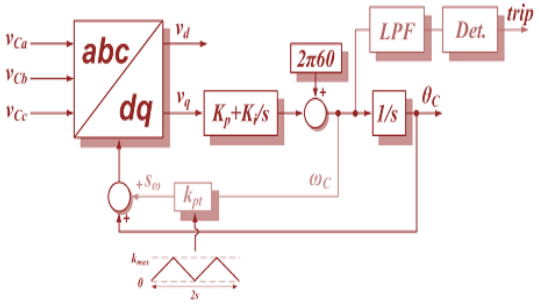

Fig. 6.Modified PLL with a large-signal feedback for islanding detection.

According to Fig. 7, the PLL output ω_C can be directlymonitored to detect the islanding condition, and a low-passfilter (LFP) is used to eliminate the high-frequency noise.The islanding-detection protection signal is set when ω_C islower than the ωth or the variation range of ω_C is beyond thethreshold.The only design parameter is kpt, because it is a very lowfrequency signal, much lower than the PLL bandwidth. Theoutput of the PLL can be assumed to be at the steady state allthe time.

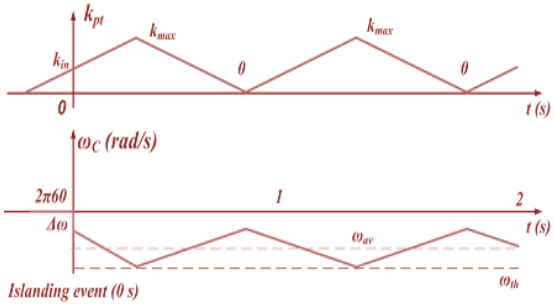

Fig. 7. First PLL output behavior when the islanding condition occurs.

The change of the grid synchronization performance owingto the additional feedback loop can be investigated by exploring the PLL model at the stiff grid-tied mode,

as shownin Fig. 9.

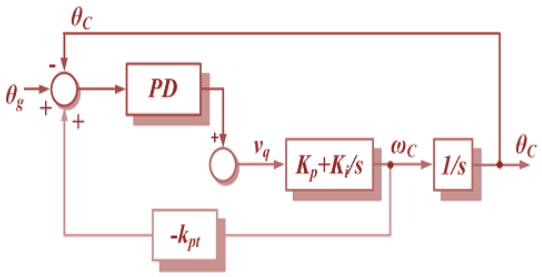

Fig. 9.Modified PLL model under the stiff grid-connected condition.

III. ISLANDING DETECTION BASED ON PLLSMALL-SIGNAL STABILITY

The PLL cannot detect the paralleled RLC load, becausethe PLL is stable according to (5). Therefore, the equilibriumpoint itself can be modified to be unstable. With this idea, thePLL can be modified as shown in Fig. 15. An additional smallsignal feedback term is introduced with a constant gain N.Then, the equivalent small-signal PLL model aroundthe equilibrium point at the islanded condition is shown
in Fig. 16

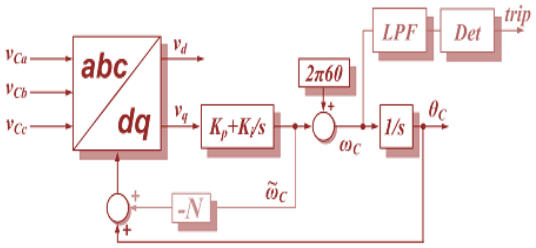

Fig. 15. Modified PLL with a small-signal feedback for islanding detection.

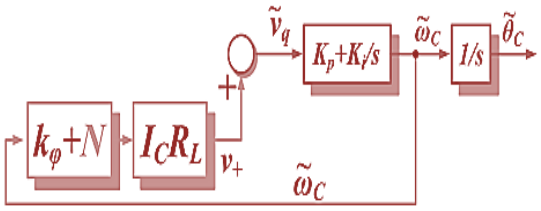

Fig. 16. Small-signal model of the modified PLL for islanding detection.

IV. SIMULATION RESULTS

The PLL behavior is verified in a 2.5 kW two-level three-phase PWM converter system shown below

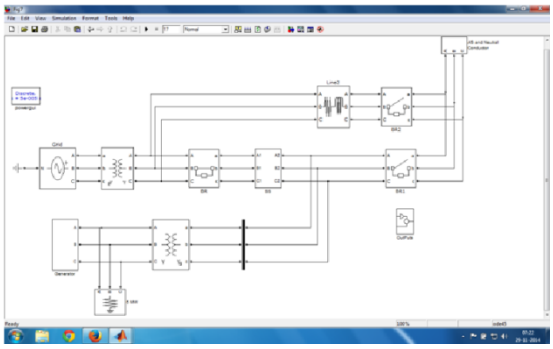

Fig. 17

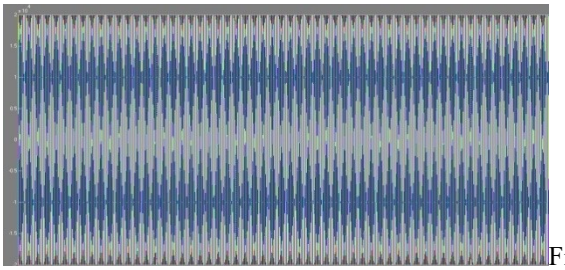

Fig. 18

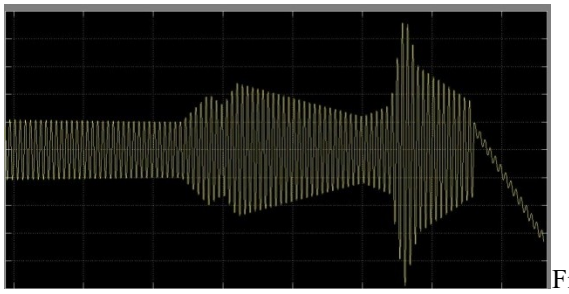

Fig. 19

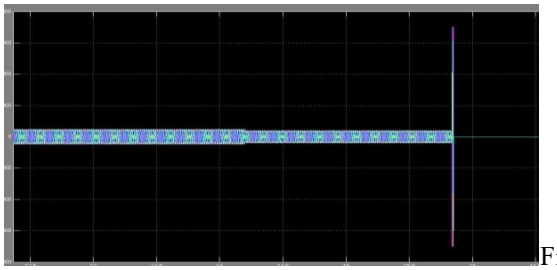

Fig. 20

V. CONCLUSION

The proposed PLL model can be used to analyze and explain the underlying theory for both large-signalperturbation-based and small-signal positive-feedback-basedislanding-detection solutions. For the large-signal perturbationbased method, the PLL keeps tracking the constantly movingequilibriumpoint. The change of PLL's grid synchronizationperformance is very limited and is robust in grid-tied conditions. The detection speed is inherently slow due to the slowPLL

bandwidth, thereby requiring a low-frequency, for example, 1 Hz, signal injection. For the small-signal instabilitybased method, the proposed small-signal PLL model showsthat the additional small-signal loop gain design is determined by the local load power quality factor and its resonantfrequency to ensure islanding-detection performance.

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BIODATA

Mahesh Thati, a teaching experience of 6 years i.e. from 2012 to 2017 and currently Working as Assistant Professor in Institute of Aeronautical Engineering college, Dundigal, Hyderabad.

Mahesh Jonnala completed Masters in Power Electronic Systems from Osmania University, Hyderabad.