International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue14
November 2017

A Carrier-Based Neutral Voltage Modulation Strategy for Seven Level Cascaded Inverters under Unbalanced Dc Sources

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ABSTRACT:*This specific project offers a pulse widthmodulation technique to achieve balanced line-to-line output voltages and maximize this modulation index inside the linear modulation range the place that the output voltage could be linearly adjusted inside the multilevel cascaded inverter (MLCI) running under unbalanced dclink conditions. Here we are implementing seven level cascade inverter. In these conditions, this linear modulation variety is lowered, and an important output voltage difference may happen as voltage references increase. So that you can analyze these effects, the voltage vector living space for MLCI can be evaluated in depth. From this analysis, the theory behind this output voltage difference is defined, and the ideal linear modulation variety considering the unbalanced dc-link problem is evaluated. After that will, a neutral voltage modulation tactic is proposed to obtain output voltage balancing and also to lengthen the linear modulation range around the greatest reachable point theoretically. In this proposed method, too large of any dclink difference precludes this balancing of the output voltages. This limitation is also discussed. Both this simulations plus the experiments for just a seven-level phase shifted modulated MLCI pertaining to electric vehicle traction engine drive show that the proposed method will be able to balance line-to-line productivity voltages and also to maximize the linear modulation range beneath unbalanced dc-link disorders.*

Keywords: Harmonic Injection, Multilevel Cascaded Inverters (Mlcis), Neutral Voltage Modulation (NVM), Phase-Shifted (PS) Modulation, Space Vector Pulse Width Modulation (PWM) (SVPWM).

I. INTRODUCTION Multilevel inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low dv/dt characteristics and generally have low harmonics in the output voltage and current. In addition, the switching of very high voltages can be achieved by stacking multilevel inverter modules [1]–[3]. Due to these advantages, multilevel inverters have been applied in various application fields [6]–[10]. Among various topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one of the prominent topologies because of its simple

structure for modularization and fault-tolerant capability. Therefore, MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction drives. In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods. Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives, where dynamic properties are very important, whereas SHEPWM is preferred in some highpower static power conversion applications. an SVPWM method has been studied to cover the over modulation range in the multilevel inverter. To reduce the common-mode voltage, a multilevel SVPWM has been proposed in . The series SVPWM method has been reported to easily implement SVPWM for the MLCI an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range are easily obtained through simple arithmetic calculations. In the proposed method, too large of a dc-link imbalance precludes the output voltages from being balanced. This limitation is also discussed. In addition, a faulttolerant operation is naturally covered, because the MLCI undergoing an unbalanced dc-link condition can be considered as an MLCI operating under a faulty condition on switch modules. Compared to the existing methods, the proposed strategy is very simple to implement, compensates the output voltage imbalance in real time, and maximizes the voltage utilization of the dc links. Therefore, if this scheme is applied to applications such as EV traction drive systems, the dynamic characteristics can be greatly improved. This paper is organized as follows. In Section II, the voltage vector space.

II. MULTILEVEL INVERTER In response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter

(imbricated cells), and the diode clamping inverter. As reported in the literature, the H-bridge cascade inverter has been used in several practical instances for broadcasting amplifier [4], plasma [3], industrial drive [6] as well as STATCOM [7] applications etc. The main limitation of the H-bridge cascade inverter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. For STATCOM application, where the isolated supplies are not required, the power pulsation at twice output frequency occurring with the dc link of each H-bridge cell necessitates oversizing of the dc link capacitors. The capacitor clamping inverter, though the three-level scheme of which was published in the early 1980's [8], had been rarely discussed until the introduction of the ―imbricated cells‖ [9]. The individual clamping capacitor needs only to smooth the switching frequency ripple voltage and the required capacity for each clamping capacitor is therefore small. However, as the number of level increases, such problems as thermal designing, low-inductance designing, as well as insulation designing of the system will become critical. Medium voltage drives using four-level capacitor clamping inverter has recently been available on the market. The diode clamping inverter, as shown in Fig. 5, published by different researchers in the early 90's can be deemed as the extension of the neutral-point-clamped (NPC) inverter introduced in the early 80's . Unlike the NPC inverter which has been extensively used today in industrial drives, tractions as well as FACTS systems, the diode clamping inverter is right under investigation. In addition to the dc link unbalance problem identified in the other problems with the diode clamping inverter.

III. PROPOSED MODULATION TECHNIQUE The maximum synthesizable voltage in the linear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

A. Traditional Offset Voltage Injection Method The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load [43], [44]. For example, the offset voltage v ∗sn isinjected to the phase voltage references v ∗ as, v ∗bs, and v ∗cs to implement carrier-based SVPWM as in

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$$v_{sn}^{*}=\frac{v_{\max}^{*}+v_{\min}^{*}}{2} \qquad v_{\max}^{*}=\max\left(v_{as}^{*},v_{bs}^{*},v_{cs}^{*}\right)$$
$$v_{\min}^{*}=\min\left(v_{as}^{*},v_{bs}^{*},v_{cs}^{*}\right). \qquad (1)$$

Then, the pole voltage references v ∗ an, v ∗bn, and v ∗cn, which will be converted to PWM duty references, are

$$v_{an}^{*}=v_{as}^{*}-v_{sn}^{*} \quad v_{bn}^{*}=v_{bs}^{*}-v_{sn}^{*} \quad v_{cn}^{*}=v_{cs}^{*}-v_{sn}^{*}. \qquad (2)$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

B. Proposed NVM Method If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches V 1 ph-max. This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage reference in the linear modulation range, the other phases can be saturated or go into the ove modulation region. In this situation, a neutral voltage can be produced by the saturated or over modulated phase.

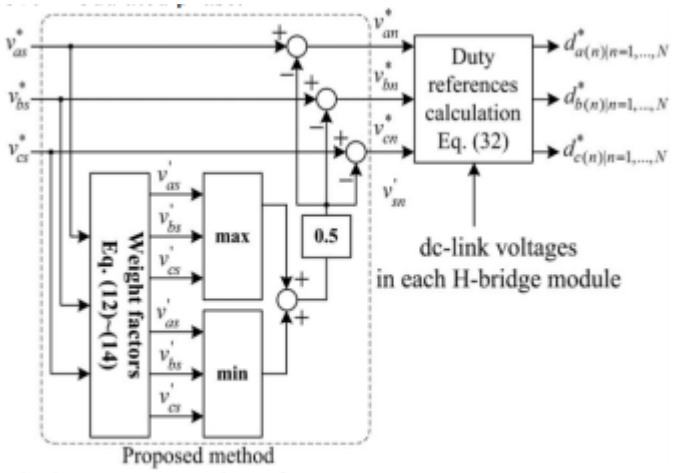

Fig.1. Implementation of the NVM method.

In order to resolve this issue and to synthesize the output voltage to V 1 phmax in the linear modulation range, the NVM technique is proposed in this paper. Fig1 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points n and s in Fig. 1 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant Kw is defined as

$$K_w=\frac{V_{\text{dc\_mid}}+V_{\text{dc\_min}}}{2}. \qquad (3)$$

By using (12), the weight factors are calculated as

$$K_{w\_a}=\frac{K_w}{V_{\text{dc\_a}}} \quad K_{w\_b}=\frac{K_w}{V_{\text{dc\_b}}} \quad K_{w\_c}=\frac{K_w}{V_{\text{dc\_c}}} \qquad (4)$$

Where, Kw_a ,Kw_b, and Kw_c represent the weight factors for phases a, b, and c, respectively. Next, the weight factors areTo

reduce the common-mode voltage, a multilevel SVPWM has been proposed. The series SVPWM method has been reported to easily implement SVPWM for the MLCI. An SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the threephase references. Some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain an optimal output voltage in the multilevel inverter. On the other hand, MLCIs require separated dc links. Therefore, if there is one or more faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI can be unbalanced without proper compensation. To resolve this issue, some studies have been conducted. It is shown that the available modulation index is reduced under faulty conditions on switch modules in multilevel inverters, and compensation algorithms are proposed for phasedisposition PWM and phase-shifted (PS) PWM cases. For a STATCOM application, a zero sequence voltage to decouple a three-phase MLCI into three single-phase MLCIs is applied as well as zero average active power techniques to operate the MLCI under unbalanced source or load conditions. Reference explains why the optimum angles and modulation indexes are necessary to obtain maximum balanced load voltages in the MLCI undergoing a fault on switching modules. A neutral voltage shifting technique has been introduced for balancing the state of charge in the MLCI-based battery energy storage system. A duty cycle modification method has been proposed to compensate an output voltage imbalance caused by single-phase power fluctuations. Reference has shown that a zero sequence component helps to obtain the maximum balanced output voltages in a fault condition. An offset voltage injection technique is studied to balance the output voltage of the MLCI, but the use of an integrator in the compensation method may reduce dynamic characteristics in applications such as EV motor drives. Recently, the multilevel multiphase feed forward space vector modulation technique called MFFSVM is proposed to compensate the voltage imbalances in MLCIs. In this paper, a carrier-based PWM strategy to balance line to line output voltages and to maximize the linear modulation range where the output voltage can

be linearly controlled in the MLCI operating under unbalanced dc-link conditions is proposed. In unbalanced dc-link conditions, the maximum synthesizable voltage in each phase is not uniform. Consequently, the linear modulation range is reduced, and a significant output voltage imbalance may occur as output voltage references increase. In order to analyze the imbalance effect, the voltage vector space for the MLCI is evaluated in detail. From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering unbalanced dc sources is evaluated. After that, a neutral voltage modulation (NVM) strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range are easily obtained through simple arithmetic calculations. In the proposed method, too large of a dc-link imbalance precludes the output voltages from being balanced. This limitation is also discussed. In addition, a faulttolerant operation is naturally covered, because the MLCI undergoing an unbalanced dc-link condition can be considered as an MLCI operating under a faulty condition on switch modules. Compared to the existing methods, the proposed strategy is very simple to implement, compensates the output voltage imbalance in real time, and maximizes the voltage utilization of thedc links. Therefore, if this scheme is applied to applications such as EV traction drive systems, the dynamic characteristics can be greatly improved.

CONCLUSION The NVM technique for MLCIs under unbalanced dc-link conditions has been in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the method.

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