

Design and Implementation of High Speed Multiplier in DSP Applications Using Mesochronous Pipelining In FPGA

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Abstract:

A novel mesochronous pipelining scheme is described in this paper. In this scheme, data and clock travel together. At any given time a pipeline stage could be operating on more than one data wave. The clock period in the proposed pipeline scheme is determined by the pipeline stage with largest difference between its minimum and maximum delays. This is a significant performance gain compared to conventional pipeline scheme where clock period is determined by the stage with the largest delay. Also, the number of pipeline stages and pipeline registers is small. The clock distribution scheme is simple in the mesochronous pipeline architecture. An 8-bit Wallace tree multiplier has been implemented in mesochronous pipeline architecture using modest TSMC 180-nm (drawn length 200 nm) CMOS technology. The multiplier architecture and simulation results are described in detail in this paper.

Keywords: High performance, mesochronous pipeline, multiplier, pipelined system, register delays.

I. INTRODUCTION

In today scenario low power consumption and smaller area are the most important parameter for the fabrication of DSP systems and high performance systems. To save notable power consumption of a DSP system, it is good to reduce its dynamic power that is the important part of total power dissipation. Digital filter are essential elements of DSP system. Digital filter can be realized by different digital filter structure such as direct form-I & II, transposed structure etc. These structures provide a space for selection of appropriate structure for minimizing of power consumption and improvement in speed of digital filter which is play important role in all high performance

DSP applications.[4] FIR filter and IIR filter are two types of Digital filter. FIR filter mostly prefer over IIR filter due to its linear phase characteristics, low coefficient sensitivity, guarantee stability.

Multiplication and addition occurs frequently in „Finite Impulse Response“ (FIR). In FIR filter, multiplier and adder plays an important role. A multiplier in a FIR filter is most power consumption component. Multiply and Accumulate (MAC) is an important unit of DSP system. It decides the power consumption and speed of operation of DSP system.

Most of DSP consumption involve the use of multiplier accumulate operation and therefore the design of fast and efficient multiplier

imperative. . The dynamic switching power consumption of digital FIR filter is reduced by using data transition power diminution technique. This technique is used on adder, multiplier and applied for filters to remove power consumption caused by unwanted data transmission.

II. FIR FILTER THEORY

Finite Impulse Response (FIR) filter are type of digital filter and consist of weighting sequence (impulse response) among non-recursive digital filters which is finite in

length. FIR filters are non-recursive digital filters has been selected for this thesis due to their good characteristics.[4] FIR filter has no feedback and its input-output relation is given by

$$y[n] = \sum_{k=0}^{N-1} a[k] \cdot x[n - k]$$

Here, $x[n]$ and $y[n]$ are the filter input and filter output respectively, $a[k]$ is the filter coefficients, N is the filter coefficient number.

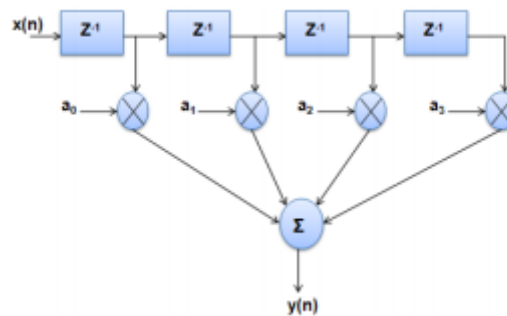


Fig. 1: FIR Filter

As shown in figure output $y[n]$ of a FIR filter is a function only of the input signal $x[n]$. The response of such a filter to an impulse consists of a finite sequence of $N+1$ samples, where N is the filter order.

III. PROPOSED RESEARCH DESIGN

With increase in number of pipeline stages, clock network load increases and distributing high-speed clock signal on longer wires with increased line parasitics (resistance, capacitance and inductance) is a complex task. This is further aggravated with technology

scaling. Also, in technology scaling, clock uncertainties like uncontrolled transmission line effects, clock skew and clock jitter do not scale like the device delays. There is an additional overhead on clock period to counter these uncertainties. With increase in size of clock network its power consumption also has increased to around 50% of the total chip power consumption [2]. In order to achieve significant performance gains, architecture can be modified to eliminate large pipelines and complex clock distribution mechanism. Architectures like wave-pipelining [3], [4], micro pipelines [5] and package wiring [6]

have been proposed, but the performance gains are not significant. An asynchronous pipelining scheme like micropipelines may be appealing since it does not require a clock signal. However, it is complex compared to synchronous schemes and the performance improvement is higher in alternate synchronous schemes [6], [7]. In order to improve the performance of pipelined systems

and greatly reduce the issues mentioned above, we propose a novel pipeline scheme called mesochronous pipelining. In this paper we introduce the mesochronous pipeline concept, followed by performance gains from the proposed scheme and finally a mesochronous pipeline design example. For clarity we shall refer to the pipelining scheme reviewed in this section as conventional pipelining.

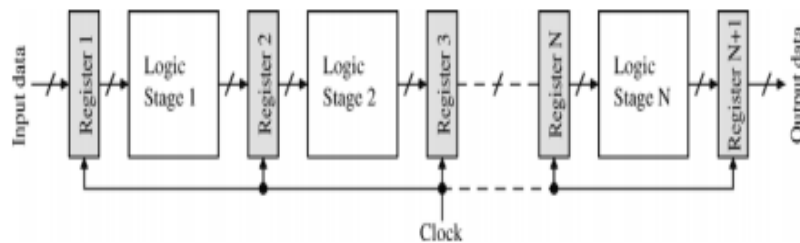


Fig. 1. N-stage pipelined system.

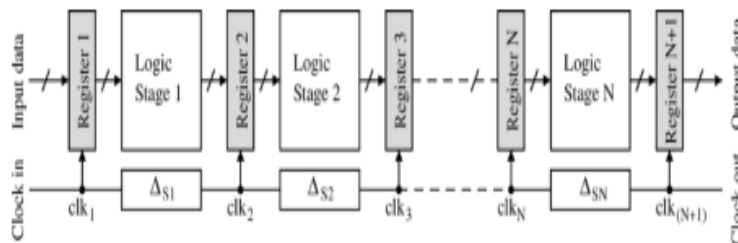


Fig. 2. Mesochronous pipelining scheme.

The proposed mesochronous pipeline scheme modifies conventional pipeline scheme to achieve performance gains. The term mesochronous has been used in the communications field; it has been defined as: the relationship between two signals such that their corresponding significant instances occur at the same rate. In the proposed scheme, the system is clocked such that a pipeline stage is operating on more than one data wave

simultaneously. At any given time, multiple waves can be present in a stage and the waves are separated based on physical properties of internal nodes in the logic stage. This concept has some similarities to the wave-pipeline scheme [3], [4]. Clock signal in this scheme is delayed so that it travels along with the data. The schematic of this scheme is shown in Fig. 2. Clock signal path includes delay elements which emulate the delay experienced by data

in pipeline stages. In this pipelining scheme, higher clock frequencies are possible, complexity of clock distribution is greatly reduced and influence of clock uncertainties is mitigated. This architecture can be used in design of any high performance pipelined system. Temporal and spatial variation of the proposed mesochronous pipeline architecture is shown in Fig. 3 for a three-stage system. In

Fig. 3 it is assumed that Stage 2 has the maximum delay difference. We shall refer to the difference between maximum and minimum propagation delays of a Stage as the delay difference of that stage. The delay difference of any stage, gives this amount of time the values generated at have to be held, till the computation is complete in that stage.

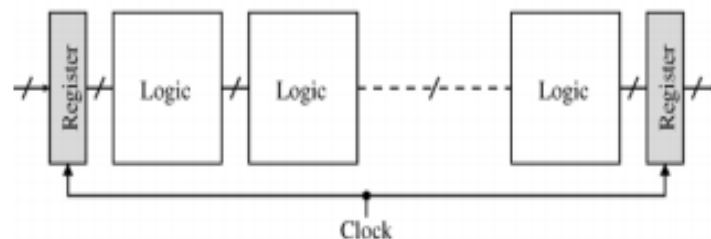


Fig. 3. Wave pipeline architecture.

To achieve the same performance (i.e., achieve), a large number of stages (in turn more registers) will be required in conventional pipeline implementation compared to mesochronous pipeline scheme. It should be noted that using thin pipeline stages (i.e., reducing) in conventional scheme, will make register delays the main delay component in each stage. On the other hand, in the mesochronous pipeline, the objective is to decrease the delay difference. The proposed mesochronous pipeline scheme has been shown to be superior to conventional pipeline scheme.

Mesochronous pipeline scheme provides a far better performance than conventional pipeline scheme, with a small number of pipeline registers.

WALLACE TREE MULTIPLIER

Wallace tree is an implementation of adder tree designed for minimum propagation delay. It has three stages such as partial product generation stage, compression and reduction. The fig (5) shows the operation of Wallace tree multiplier. Here uses (8×8) Wallace tree multiplier [8]. Multiply each bit of the argument by each bit of the other;. Which can generate 8 set of partial products in row order. Depending on position of the multiplier bits the wires carry different weights. Reduce the number of partial products by layer of full adder and half adder. In this full adder is implemented using 3:2 compression technique and half adder is implemented using 2:2 compression technique. Group the wires into two numbers and add them using carry propagation adder.

IV. RESULTS AND DISCUSSION

We perform the simulation and synthesis and summarize the results of all adders and

multiplier. Functional verification of all the adders and multiplier are performed and these modified architectures are applied in 4-tap FIR filter finally results are summarized.

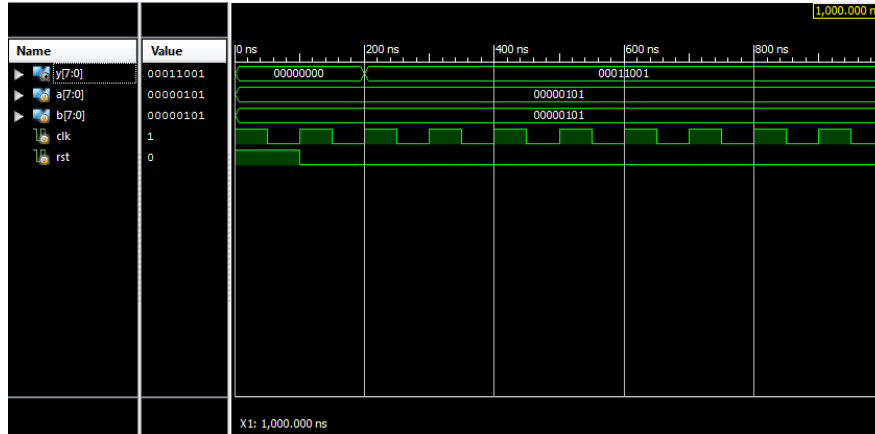


Fig 4: simulation result for the proposed system.

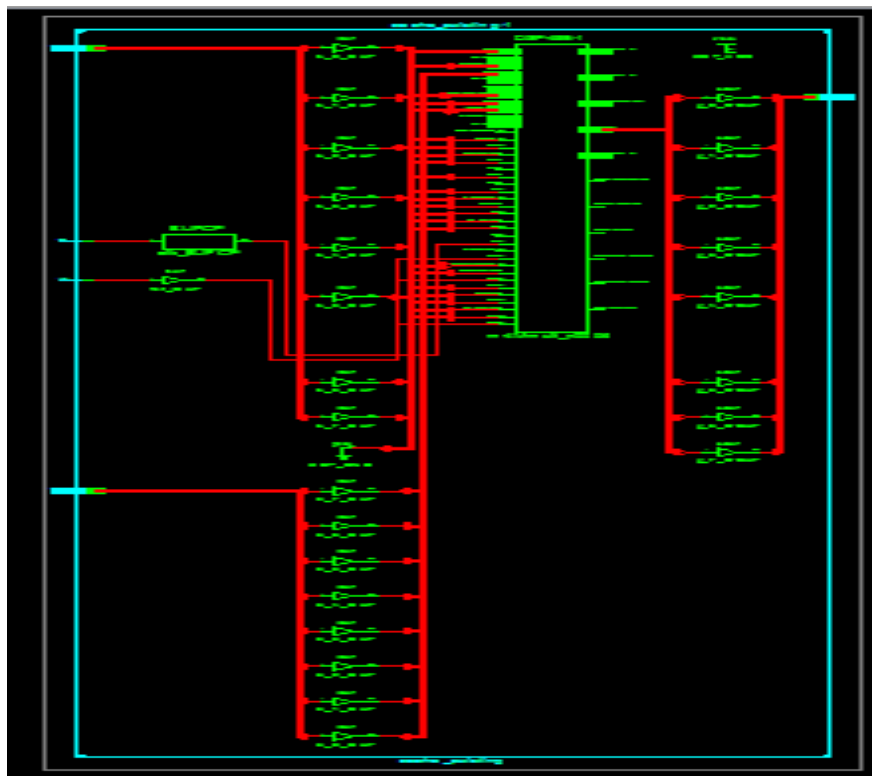


Fig 5: technology schematic for the proposed system.

V. CONCLUSION

In this paper, novel mesochronous pipeline architecture has been presented which

achieves better performance compared to conventional pipeline architecture. The performance gain possible and design aspects of this architecture have been discussed in

detail here. A CSA multiplier implemented in mesochronous pipeline architecture as a design example has been described in detail and the performance improvements have been discussed. Following are the features of the mesochronous pipeline architecture in comparison with conventional pipeline scheme.

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