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Improved Multipliers Based On Non Redundant Radix-4 Signed Digit Encoding

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ABSTRACT:

It's observed the pre-encoded NR4SD architectures tend to be more area efficient compared to conventional or pre-encoded MB designs regarding their performance within the cheapest possible clock period. Within this paper, we introduce architecture of pre-encoded multipliers for Digital Signal Processing programs according to off-line encoding of coefficients. Multimedia and Digital Signal Processing (DSP) programs (e.g., Fast Fourier Transform (FFT), audio/video Codes) execute a lot of multiplications with coefficients that don't change throughout the execution from the application. A CSD-based pglable multiplier design was suggested for categories of pre-determined coefficients that share certain features. For this extend, the Non-Redundant radix-4 Signed-Digit (NR4SD) encoding technique, which utilizes the digit values, is suggested resulting in a multiplier design with less complex partial items implementation. The performance from the suggested designs is recognized as with regards to the width from the input figures. Extensive experimental analysis confirms the suggested pre-encoded NR4SD multipliers, such as the coefficients memory, tend to be more area and power efficient compared to conventional Modified Booth plan.

Keywords: Multiplying circuits, Modified Booth encoding, Pre-Encoded multipliers, VLSI implementation

I. INTRODUCTION

Because the multiplier could be a fundamental component for implementing computationally intensive application-locations, its architecture seriously affects their performance. Constant coefficients may be encoded to aid minimal non-zero figures when using the Canonic Signed Digit (CSD) representation. CSD multipliers comprise minimal non-zero partial items, which decreases their switching activity. However, the CSD encoding involves serious restrictions [1]. Folding technique, which reduces plastic area by time multiplexing many techniques into

single functional models, e.g., adders, multipliers, isn't achievable because the CSD-based multipliers are hard-wired to specific coefficients. A CSD-based parable multiplier design was suggested for categories of pre-determined coefficients that share certain features. Also, this process cannot be easily extended to large categories of pre-determined coefficients attaining concurrently high quality. Modified Booth (MB) encoding occupies these restrictions and reduces to half the amount of partial items making reduced area, critical delay and power consumption. What size ROM acquainted with keep categories of coefficients is considerably reduced combined with area and power technique circuit. Multimedia and Digital Signal Processing (DSP) programs (e.g., Fast Fourier Transform (FFT), audio/video Codes) execute plenty of multiplications with coefficients that don't change with the execution within the application [2]. However, this multiplier design lacks versatility because the partial items generation unit was created for several coefficients and cannot be reused for the following group... However, a separate encoding circuit is needed along with the partial items generation is much more complex. Kim et al. suggested a method similar, for creating efficient MB multipliers for categories of pre-determined coefficients sticking with the same restrictions described in the last paragraph. Because the values of constant coefficients are known ahead of time, we encode the coefficients off-line while using MB encoding and MB encoded coefficients (i.e., 3 bits per digit) in a ROM. We reference this design as pre-encoded MB multiplier. Then, we explore a Non-Redundant radix-4 Signed-Digit (NR4SD) encoding plan stretching the serial encoding techniques. The suggested NR4SD encoding plan uses among the following categories of digit values. To be capable of cover the dynamic selection of the 2's complement form, all figures within the suggested representation are encoded based on NR4SD except the key one that's MB encoded. When using the suggested encoding formula, we pre-encode the standard coefficients and store them in a ROM within the condensed form (i.e., 2 bits per digit). In comparison for that pre-encoded MB multiplier where the encoded coefficients need 3 bits per digit, the suggested NR4SD plan cuts lower round the memory size. Also, in comparison for that MB form, which utilizes five digit values the suggested NR4SD encoding uses four digit values [3]. Thus, the NR4SD-based pre-encoded multipliers give a less complex partial items generation circuit. We explore the efficiency within the aforementioned pre-encoded

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multipliers considering what size the coefficients' ROM.

II. EXISTING ALGORITHMS

Modified Booth (MB) is really a redundant radix-4 encoding technique. Thinking about the multiplication from the 2's complement figures A, B. we present the Non-Redundant radix-4, Signed-Digit (NR4SD) encoding technique. As with MB form, the amount of partial items is reduced to half. When encoding the 2's complement number B, as noticed in the NR4SD- encoding technique, the NR4SD form has bigger dynamic range compared to 2's complement form. Thinking about the 8-bit 2's complement number N, two typical values of N, and is definitely the MB, NR4SD- and NR4SD numbers that result when using the related encoding strategies to each worth of N we considered. We added a bar over the adversely signed numbers to be able to distinguish them in the positively signed ones.

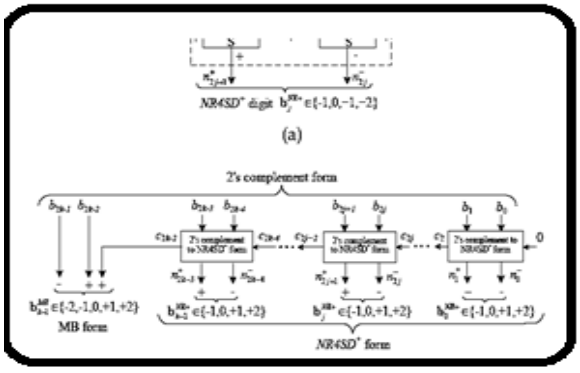

Fig.1. Block diagram of NR4SD+

III. PROPOSED IMPLEMENTION

We explore the implementation of pre-encoded multipliers. Among the two inputs of those multipliers is pre-encoded in both MB or perhaps in NR4SD_ / NR4SD representation. We take into account that this input develops from a group of fixed coefficients (e.g. the coefficients for several filters by which this multiplier is going to be utilized in a devoted system or even the sine table needed within an FFT implementation. The coefficients are encoded off-line according to MB or NR4SD calculations and also the resulting items of encoding are kept in a ROM. Since our purpose would be to estimate the efficiency from the suggested multipliers, we first present overview of the traditional MB multiplier to be able to compare it using the pre-encoded schemes. The architecture from the system which comprises the traditional MB multiplier and also the ROM with coefficients in 2's complement form [4]. Within the pre-encoded MB multiplier plan, the coefficient B is encoded off-line based on the conventional MB form. The multiplier and also the PPG from the pre encoded MB, NR4SD+ and NR4SD designs present within the conventional MB plan. The comparison one of the designs starts in the cheapest common achievable clock period for those designs and

continues at greater clock periods by growing the time period by step .2 ns until it reaches 4 ns. It's observed the pre-encoded NR4SD architectures tend to be more area efficient compared to conventional or pre-encoded MB designs regarding their performance within the cheapest possible clock periods. Regarding power dissipation, the pre-encoded NR4SD+ plan consumes minimal power which, within the installments of 16 and 24 items of input width, is equivalent to the ability consumed through the pre-encoded MB design. The machine architecture for that pre-encoded NR4SD multipliers is presented we lessen the memory requirement to n 1 bits per coefficient as the corresponding memory needed for that pre-encoded MB plan is 3n/2 bits per coefficient [5]. Thus, the quantity of stored bits is equivalent to those of the traditional MB design, except which are more significant digit that requires an additional bit because it is MB encoded. As clock period increases, the data path from the multiplication circuit changes and also the standard cells employed for its synthesis dwindle complex regarding area occupation, internal capacitance and ports' load. However, the ROM utilized in each evaluated design is really a standard cell and it is critical delay, area occupation and both internal and ports' load remain unchanged as clock period increases. We used Synopsys Design Compiler and also the Faraday 90 nm standard cell library to synthesize the evaluated designs, thinking about the greatest optimization degree and maintaining your hierarchy from the designs. The performance from the suggested designs is recognized as with regards to the width from the input figures. Finally, we used Synopsys Primetime to calculate power consumption.

IV.RESULTS:

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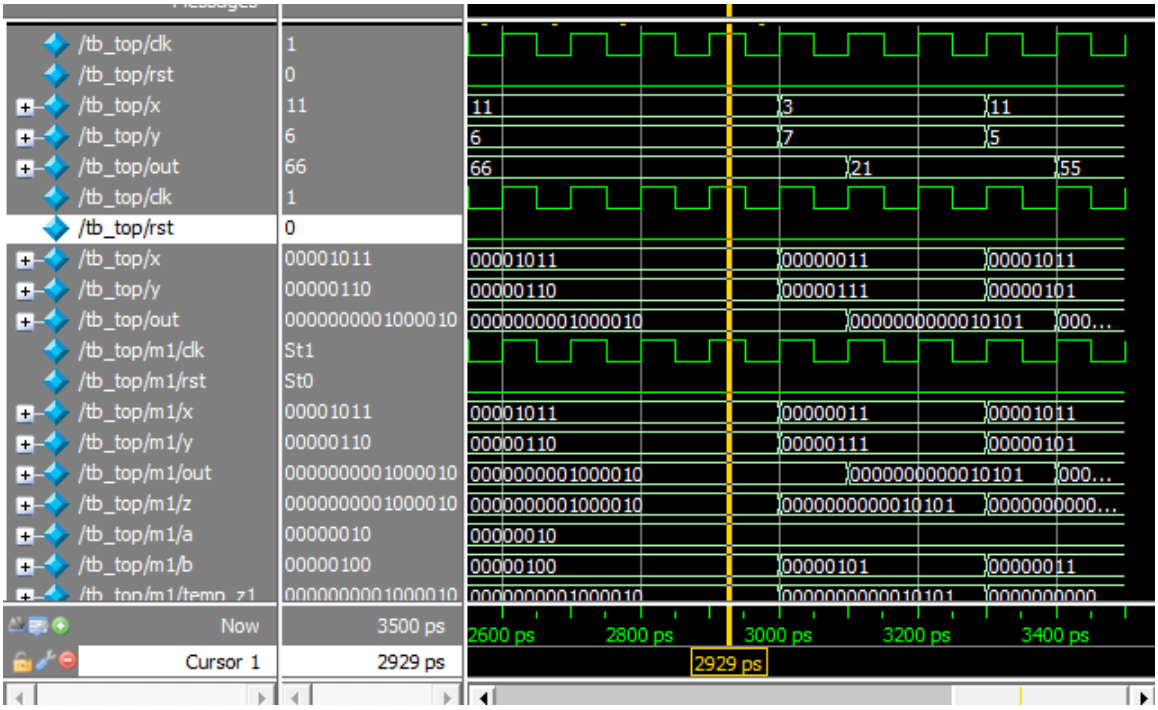
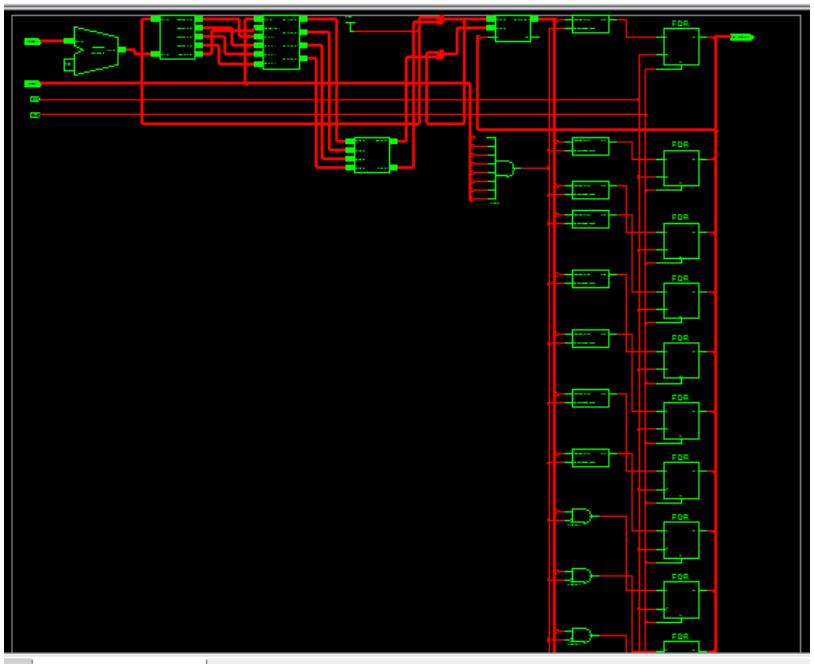


Synthesis Results:

RTL schematic:



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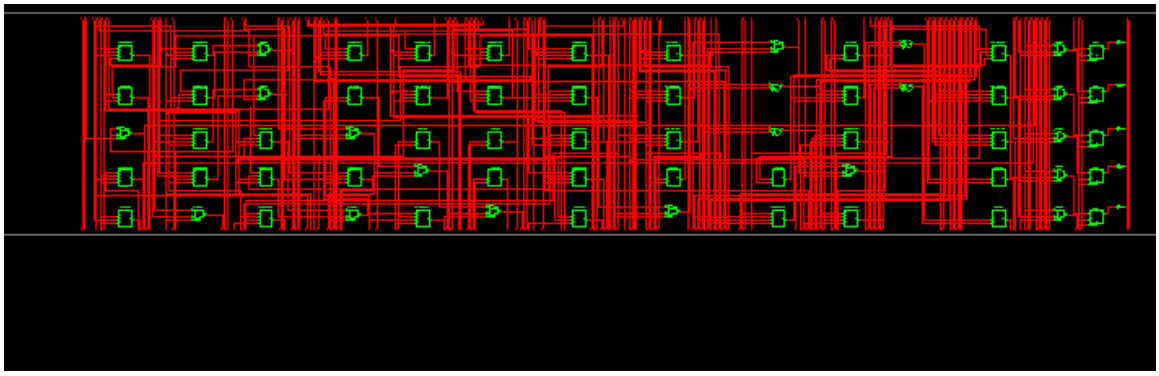
Technology Schematic:



Design Summary:

hklhlkh Project Status (09/12/2016 - 13:17:30)			
Project File:	hklhlkh.ise	Current State:	Synthesized
Module Name:	mul_NR4SD	• Errors:	No Errors
Target Device:	xc3s500e-5fg320	• Warnings:	26 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

hklhlkh Partition Summary	[-]
No partition information was found.	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	105	4656	2%
Number of Slice Flip Flops	8	9312	0%
Number of 4 input LUTs	181	9312	1%
Number of bonded IOBs	34	232	14%
Number of GCLKs	1	24	4%

Timing Report:

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: 19.392ns

Maximum output required time after clock: 4.040ns

Maximum combinational path delay: 19.392ns

V. CONCLUSION

The suggested pre-encoded NR4SD multiplier designs tend to be more area and power efficient in comparison towards the conventional and pre-encoded MB designs. We advise encoding these coefficients within the Non-Redundant radix-4 Signed-Digit (NR4SD) form. Regarding power dissipation, the pre-encoded NR4SD+ plan consumes minimal power which, within the installments of 16 and 24 items of input width, is equivalent to the ability consumed through the pre-encoded MB design. Within this paper, new types of pre-encoded multipliers are investigated by off-line encoding the conventional coefficients and storing them in system memory. The performance from the suggested designs is recognized as with regards to the width from the input figures. Extensive experimental analysis confirms increases from the suggested pre-encoded NR4SD multipliers when it comes to area complexity and power consumption in comparison towards the conventional MB multiplier.We used Synopsys Design Compiler and also the Faraday 90 nm standard cell library to synthesize the evaluated designs, thinking about the greatest optimization degree and maintaining your hierarchy from the designs.

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