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A Review: Comparison of Junction Based Transistor with Junctionless Transistor

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Abstract- *Now days, Digital Devices are designed using nanotransistor i.e. building block of any digital system. Scaling of gate in transistor device is considering main feature of fabrication technique. Smallest 10 nm Gate length devices were fabricated earlier. Now day's Junctionless transistor is a uniformly doped nanowire without junctions with a wrap-around gate. The atomic force microscopy nanolithography with two wet etching processes was implemented to fabricate simple structures as double gate and single gate junctionless silicon nanowire transistor on low doped p-type silicon-on-insulator wafer. In this paper review of structure, characteristics of junction transistor and junctionless transistor compared. This transistor in which there are no junctions and no doping concentration gradients. They have near-ideal sub threshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistor. Various simulators are available for simulation of junctionless transistor such as Silvaco ATLAS and Silvaco TCAD.*

Keywords- junctionless transistor, Gates resistor, structure of junctionless transistor, fabrication technique. ITRS Roadmap

1. INTRODUCTION: The standard of human living has been greatly revolutionized by modern technologies. This is spearheaded by the advancement in semiconductor industry. The relevance of Semiconductor research is established by the recent Semiconductor Industry Associations' Reports [1] suggesting a worldwide turnover of an overwhelming $305.6 Billion sales in the year 2013, clear 4.8% increase over the figures obtained the year before. Moores' Law [2] has guided the trends in technology in his prediction of the technology node that is eapected to half in every eighteen months.

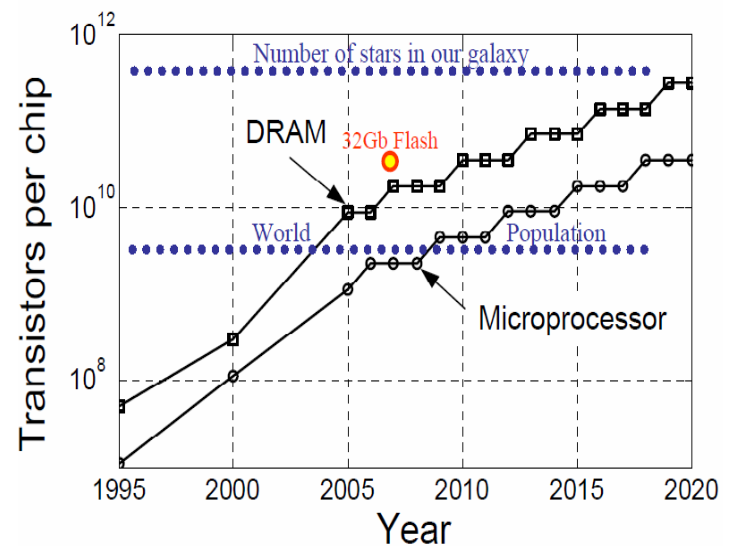

Figure 1 Moores'law of evolution

This eapects the packing density of the integrated circuits to be doubled in one and a half years. But owing to voracious geometrical scaling [3] the semiconductor device dimensions are nearing the physical limits [4, 5] such that they cannot be further scaled down without adversely affecting their performance. Thus the progress of the semiconductor industry is on the verge of stagnation owing to the limitations that have been ushered in from various technological bottle necks. Efforts are now being made to get around the problem and reach the goals set up by the industry through the International Technology Roadmap for Semiconductors [6]. Such efforts have seen various research groups exploring novel device architectures, starting from the Strained Silicon Technologies [7] spanning the Silicon-on-Insulator

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(SOI) structures [8], the multi-GATE architectures like the Fin-FETs [9-13] and other advanced Gate Engineered Transistors of late [14,15]. The main issues which stand in the way of success of the semiconductor devices in the deep sub-micron regime, (order of 10nm and below), are the sharp gradient in doping profiles, thermal budget issues for processing, various short channel effects like drain induced barrier lowering, punch through,etc. and finally the sub-threshold characteristics of such small dimensional devices. As predicted by ITRS 2012 reports, the geometrical gate length is stipulated to reach 9nm at around 2016. At such a small gate length the quantum mechanical effects like carrier quantisations become predominant. The source-substrate and drain substrate junction formation in small scale devices become very difficult as it requires sharp doping density gradient which causes thermal budgeting issues. The performance of such small scale devices deteriorate due to the various detrimental short channel effects [16]:

- drain-induced barrier lowering
- punch through
- surface scattering
- velocity saturation
- impact ionization
- hot electron effect

The narrow width effects also become predominantly large, bringing device performance metrices below tolerance limits. With the complexity of the device architectures, process variations and corresponding complexities increase manifold. Therefore the fabrication of such novel device structures involves costly equipments leading to rise in batch fabrication and production cost per chip.

2. PHYSICAL STRUCTURE AND CURRENT CONDUCTION IN JUNCTIONLESS TRANSISTOR

It has been reported by J P Colinge et.al [14] the physics of the Junctionless Transistor (JLT) is very different from that of the MOSFET. Current conduction is a bulk phenomena in JLT. The normally on-channel conducts during the on-state when bias is applied across source and drain. The gate voltage induces depletion region in the channel to turn off the current.

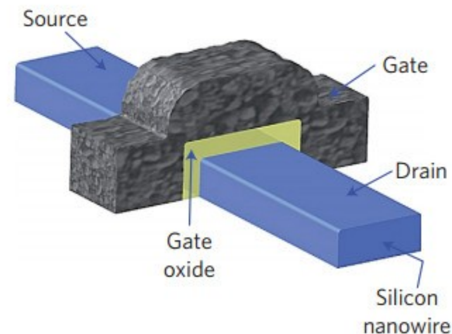

Figure 2: junctionless transistor [14]

The channel depletion constricts the cross section of the channel and reduces the current flow. Finally the channel is pinched off. Since current conduction in JLT is a bulk phenomenon, the channel needs to be made much thin for the gate voltage to be able to turn off the transistor.

Also the channel region has to be highly doped in order to turn the channel on fast. The conduction phenomena in JLT are similar to that of the Field Effect Transistor.

3. FABRICATION PROCESS

The junctionless nanowire transistor (JNT) is a heavily doped SOI nanowire resistor with an MOS gate that controls current flow. Doping concentration is constant and uniform throughout the device and typically ranges $10^{19}$from 10^{20} cm-3. The device features bulk conduction instead of surface channel conduction.

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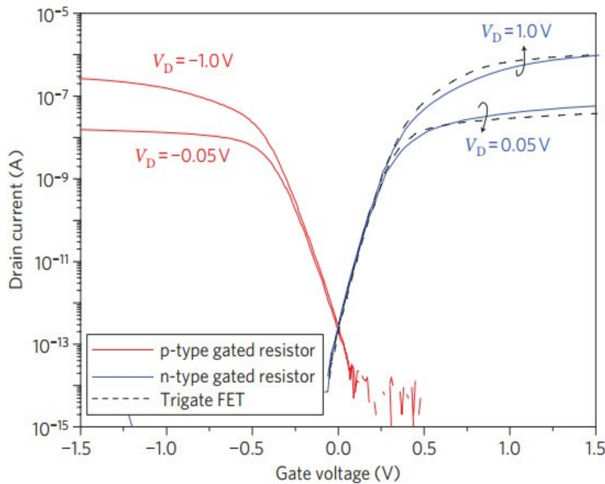

Figure 3: Current Voltage Characteristics [14]

Junctionless fabrication process is greatly simplified, compared to standard CMOS since there are no doping concentration gradients in the device. Structure with polysilicon gate is shown in figure 4.

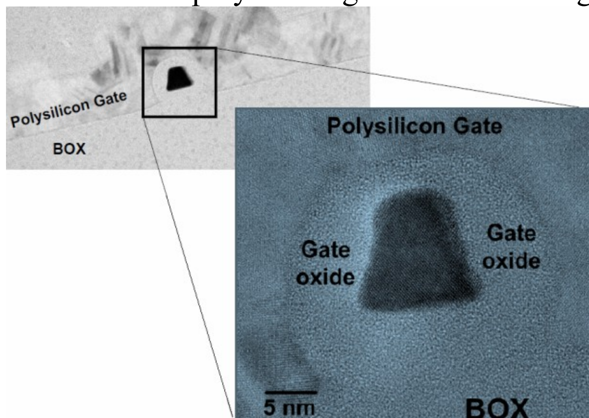

Figure 4: Cross sectional view of junctionless transistor

Junctionless nanowire transistors with gate length down to 50 nm were fabricated using the process described. The gate oxide thickness is 5 nm and beam lithography was used to pattern both the nanowires and the gates. The n-channel devices were doped using arsenic to a channel concentration of $5x10^{19}cm^{-3}$ and P+ polysilicon was used as gate material.

4. TYPES OF JUNCTIONLESS TRANSISTOR

Junctionless MuGFET

This device has no junctions, a simpler fabrication process, less variability and better electrical property than classical inversion mode.

Bulk Planar Junctionless Transistor (BPJLT)

The bulk planar junctionless transistor (BPJLT) is highly scalable source–drain junction- free field-effect transistor. It is thus junctionless in the source–channel–drain path but needs a junction in the vertical direction for isolation purposes.

Junctionless Vertical MOSFET (JLVMOS)

The junctionless VMOS is based on bulk-Si wafer. The vertical channel of a VMOS is defined by the gate spacer thus the fabrication cost can be reduced drastically. The double-gate scheme of a VMOS helps to increase the gate controllability over the channel region.

5. COMPARISON

The physics of the JNT is quite different from that of standard mitigate FETs. The comparison comparison of junctionless and junction transistors [15] in figure 5. The comparison between all modes is given in the table 1 below.

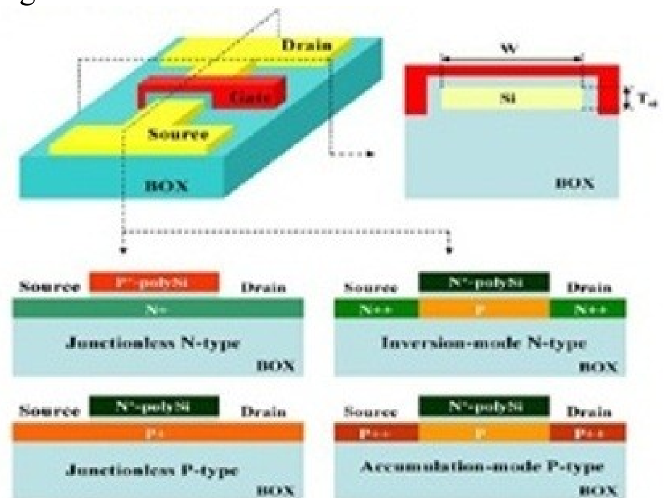

Figure 5: Comparison of junctionless and junction transistors [15]

Table1: Comparisons of conduction mode

State	Inversion - mode	Accumulation mode	Junctionless
On	Main current in surface inversion channels	-Surface accumaltion channels -small body current	-Surface accumaltion channels are unnecessary -large body current
off	Surface	body	body

	subthresold current	subthresold current	subthresold current

Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold, but above threshold the field drops to zero. This is the opposite of inversion-mode (IM) or even accumulation mode (AM) devices where the field is highest when the device is turned on. The electron concentration profiles in cross sections of IM, AM and JNT devices are shown in Figures 6

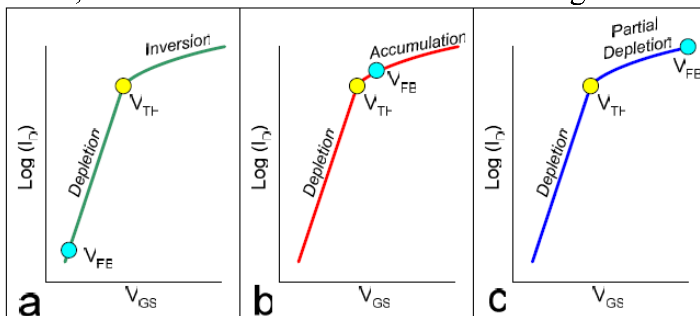

Figure 6: Current in inversion-mode (a), accumulation-mode (b) and junctionless (c)

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