International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue 14
November 2017

Design and Simulation of Low Power CMOS Ternary Full Adder

[1]V. BHANU SREE , [2]J. PRAVEEN

[1]ASSISTANT PROFESSOR, TEEGALA KRISHNA REDDY ENGINEERING COLLEGE, TELANGANA, INDIA

[2]DEPT. OF E.C.E, HYDERABAD, TELANGANA, INDIA

ABSTRACT: Ternary system is defined as a number system with radix-3. With a lot of new ternary circuits being proposed as an alternative to the digital logic, we consider a step further that in this paper we proposed to design a Ternary coded Decimal (TCD) adder circuit based on CMOS technology. Unlike a Ternary adder, the TCD adder utilizes 3-bit Ternary coded Decimal (TCD) number as input and the resulting sum will also be in TCD form. The designing of TCD adder is depends on a new custom circuit for ternary adder which is modifying for less number of transistors. In the due course we will also highlight how non-conventional, custom designed circuits give area advantage compared to the Ternary k-map based methods.

Keywords —Ternary Coded Decimal, Adder, TCD, Ternary Adder, CMOS ternary

I.INTRODUCTION

Digital computer systems that are now used are binary digital systems. But, there is a new logic which is making its way to a new future. The logic which unlike binary uses 3 symbols. A number system built with a radix 3 is called as ternary number system. Though binary circuits are easy to implement in CMOS technology, they have got their own limitations. One of the limitations is, the larger the operands, the more amounts of binary circuits needs to be cascaded.

For an example consider the following case, design of a parallel adder for unsigned number. If it is assumed that the maximum value of operand is always less than 256, it may be able to use an 8-bit adder, which is

And if it is assumed that the number can take value 64K, and then its needed to built a 16-bit adder, by cascading single bit adders.

This is because of the huge code capacity of ternary logic. In ternary logic an 8-bit code can represent a number as large as 6K (i.e. 3^8). Therefore, the above discussion suggests that ternary indeed can be a very good alternative to the binary. The only problem being, the circuit in ternary can't be that easily designed as in binary. This fact again provides a good opportunity for developing new custom circuits.

One such circuit is the one proposed in this paper. In fact, we can develop any combinational ternary circuit, if we could follow the ternary k-map, but to do that we need to have a set of basic gates for ternary. Even if we are able to implement the circuit, it is going to be very huge, consisting of hundreds of transistor if not thousands. To get the same functionality with reduced number of transistor we need to develop each circuit customarily, a lot of gates had been proposed for ternary gates, we try to propose other combinational circuits.

The chip area increases with the number of functions increases and when the number of inputs increases in binary logic. To overcome these problems multi valued logic systems are used where the radix is greater than 2 are the main trust for research. Ternary logic is one of the multi valued

logic system with base 3. For 'n' inputs the number of functions realized will be larger in ternary logic than in binary logic. So, ternary logic area can be reduced for higher bit order.

II.DESIGNING OF TERNARY CODED DECIMAL ADDER

Ternary coded decimal (TCD) is required in electronic systems e.g. where a decimal value needs to be displayed. It is better to process the data in TCD format if input and outputs are decimal, than to convert it from decimal to ternary and back to decimal. By using TCD codes, the manipulation of decimal data can be greatly simplified by considering each digit as a separate single sub-circuit.

These matches are much more close to the physical reality of decimal input and output hardware. If the numeric quantity were stored and manipulated as pure ternary, interfacing to such a display would require complex circuitry. Therefore, in cases where the calculations are relatively simple, working throughout with TCD can lead to a simpler overall system than converting to ternary.

A. TCD codes of Decimal numbers:

TCD is another method to represent decimal numbers. Each decimal number is defined by a ternary code of 3 bits.

i.e. Only 0-9 has the correct TCD code.

When two TCD numbers are added Decimal numbers greater than nine may be obtained and hence the resulting code will not be a valid TCD. In such case we need to correct the result.

TABLE I. TABLE OF TCD CODES FOR DIFFERENT DECIMAL NUMBERS

Decimal	Bit2	Bit1	Bit0
0	0	0	0
1	0	0	1
2	0	0	2
3	0	1	0
4	0	1	1
5	0	1	2
6	0	2	0
7	0	2	1
8	0	2	2
9	1	0	0

B. Method for correcting the sum after addition

After an analysis of the results it was found that the TCD sum needs the following correction process. If result is greater than 9, then correct by adding '122' to the obtained sum, to get a valid TCD output. Then carry produced will act as a higher digit.

• Case1:

If the sum is less than or equal to 9 As an example consider the case below.

$$4. \Rightarrow 011$$
$$5. \Rightarrow 012$$
$$\overline{09} \Rightarrow \overline{0100}$$

In this case there is no need to add or modify it.

• Case2:

If the sum is greater than 9. As an example consider the case below.

$$6. \Rightarrow 020$$
$$5. \Rightarrow 012$$
$$\overline{09} \Rightarrow \overline{0102}$$

The result is greater than 9 so to convert into TCD form we have to add ternary value '122'.

$$\begin{array}{r} 0102 \\ 0122 \\ \hline 1001 \end{array}$$

In this result, 001 represent first bit (1 in decimal no). Remaining carry '1' represent second bit (1 in decimal no).

C. TCD Architecture

The proposed architecture of the TCD adder is shown in the figure below

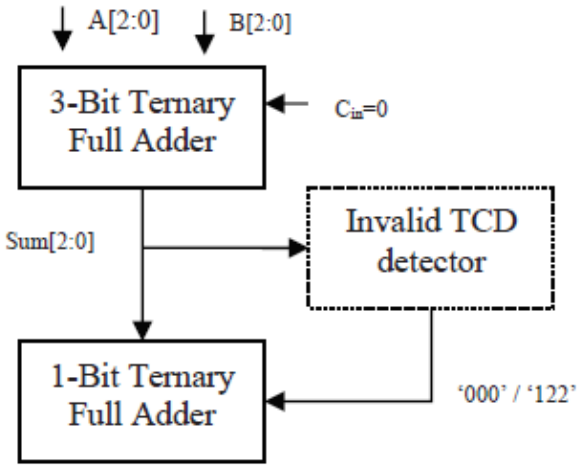

FIG. 1. TERNARY TCD ADDER BLOCK DIAGRAM

This is the basic block diagram of the ternary TCD adder and it shows the different block involved in TCD adder. Each block is designed and simulated in cadence. Later all the blocks are interfaced to get the TCD adder. A and B are two ternary input and Cin is the carry input. The 'Sum' output of the first adder may or may not be a valid TCD code. An invalid TCD code is detected by an 'Invalid TCD detector circuit'. If the code is invalid it gets modified by the next adder preset in the data path.

III. TERNARY HALF-ADDER

A. Ternary half Adder:

The truth table of a ternary half adder circuit is given by the following table II. A and B represents two input which can take three different values 0, 1, 2. The output will also consist of three levels. The expected result from the resulting nine combinations is shown in table II.

TABLE II. TRUTH TABLE OF TERNARY HALF ADDER

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

This functionality can be implemented in a variety of ways. This work uses a less transistor count half adder. An optimized ternary half adder circuit is used in this work.

IV. DESIGNING OF TERNARY FULL-ADDER

A. Ternary Full Adder:

In Ternary full adder, A, B, C in represent two input which can take three different values 0, 1, 2. The output will also consist of three levels.

This functionality can be implemented in a variety of ways. Firstly, we can use the ternary K-map. But by using it we find that the number of gates and hence the number of transistors drastically increases. The other alternative is to design a custom circuit to get the above functionality.

B. Ternary Full Adder using Ternary Half adder:

As TCD Adder circuit is built using Ternary full adders, therefore full adder circuit needs to be developed first. An optimized way to implement full adder is, with the help of half adder than that of implementing full adder itself by using k map methods.

Minimum of 3 half adders are utilized to design a complete ternary full adder. After adding A and B its sum is given to the next half adder as an input along with C. Its sum is the ultimate, full adder sum. The carry generated by Half adder (using A,B) and carry generated from the second adder for which C is given as one of the inputs are added with the help of half adder. The sum obtained by those two carries is the final carry of the full adder.

V.RESULTS

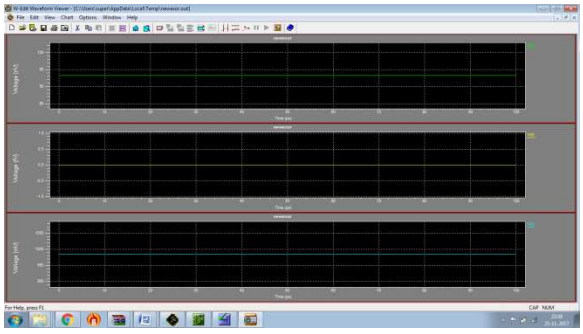

FIG. 2 OUTPUT WAVEFORM

```
Parsing                          0.03 seconds
Setup                            0.03 seconds
DC operating point               0.01 seconds
Transient Analysis               0.00 seconds
Overhead                         3.12 seconds
-----------------------------------------------
Total                            3.18 seconds
```

FIG. 3 REPORT

VI.CONCLUSION

New ternary adders have been proposed in this paper based on a logic style which is mostly composed of binary parts. Therefore, static power consumption reaches its minimum amount. Extensive different analyses have been carried out to examine efficiency in all aspects. The proposed designs benefit from low power consumption, high driving power, full-swing operation, and capability of working in low voltages and high frequencies. They can be used in larger circuits and practical environments.

VII.REFERNCES

[1] [Bianca Silveira, et. al "Power-Efficient Sum of Absolute Differences Hardware Architecture Using Adder Compressors for Integer Motion Estimation Design" Ieee Transactions On Circuits And Systems–I: Regular Papers 1549-8328, Digital Object Identifier 10.1109/TCSI.2017.2728802

[2] Jinghang Liang, Linbin Chen, Jie Han, "*Design and evaluation of multi valued logic gates using Pseudo N-type carbon Nanotube FETS*", IEEE Proceedings vol 13, No. 4, July 2014, pp. 695–708.

[3] A.P.Dhande, Satish, S.Narkhede, Shridhar and S.Dumdam, "*VLSI implementation of ternary gates using tanner tools*", 2014 2nd International Conference on Devices, Circuits and Systems.

[4] Vikram Ghiye, Sharan Bonde and Ashwinikumar Dhande, "*Investigation of Ternary Function Minimization*", 2014

Fourth International Conference on Communication Systems and Network Technologies.

[5] Viswa Saidutt, Srinivas, Sai Phaneendra and Moorthy Muthukrishnan, "*Design of Encoder for Ternary Logic Circuits*", 2012 Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PRIMEASIA), pp. 85-88.

[6] Mudhafar A. Hassan Ali, Falah J. Hassan-Alshiroofi and Hemant G. Rotithor, "*A Framework for Design of Multivalued Logic Functions and Its Application Using CMOS Ternary Switches*", IEEE transactions on circuits and systems-I: fundamental theory and applications, vol. 43, no. 4, April 1996, pp. 279-289.

[7] Chetan Vudadha, Sreehari V and M.B. Srinivas, "*Multiplexer Based Design for Ternary Logic Circuits*", PRIME 2012, Aachen, Germany Session TG1 – Analog and Mixed Signal III, pp 139-142.

[8] Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi, "*A Novel CNTFETBased Ternary Logic Gate Design*", IEEE 2009, pp. 435-438.

V. BHANU SREE working as Assistant professor in Teegala Krishna Reddy Engineering College. Completed M.Tech degree in DECS in G Narayanamma college of engineering & technology, JNTU, Hyderabad, in 2013. Received the B.Tech degree in Electronics and Communication Engineering from SLCH , JNTU, Hyderabad, in 2010, research interests include Digital, wireless communication, Radar system, Telecommunications and frontend logic design and hardware/software co-frication.

J. PRAVEEN Completed M.Tech degree in VLSI System Design from Briilaint Institute Of Engineering Techonolgy, Jntu, Hyderabad. received the b.tech degree in Electronics And Communication Engineering from Teegala Krishna Reddy College Of Engineering And Techonolgy, Jntu, Hyderabad, in 2010, His area of interest is Low Power V.L.S.I, and Digital communication.