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Dtmf Flag Age and Recognition Utilizing Successful Dft (Goertzel Calculation) Method on Fpga

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ABSTRACT: - *Double tone multi-recurrence (DTMF) is a flagging standard in telecom applications that produces two tones all the while for each key press. By utilizing proficient DTMF, this task partitioned into three stage's i.e. FFT, Split Goertzel Algorthim without Asset Sharing Methodology, and Split Goertzel Algorthim with Asset Sharing Methodology. In these three stages we investigate territory, timing and power. Initially stage is Quick Fourier Change (FFT). In FFT, recursive operation is rehashed N times. So that in FFT it requires more equipment, control and time. Second stage is spilt Goertzel Algorthim without Asset Sharing Methodology. For fast tone discovery third procedure i.e, Split Goertzel Algorithm with Asset Sharing Methodology is utilized. Here, it utilizes foreordained frequencies& extremely negligible arrangement of equipment, booked sources of info and yields are utilized at fitting clock edges. With the goal that it devours less zone and power. To identify DTMF location another kind of ZYBO board ZYNQ 7000 arrangement FPGA is utilized. Zynq is the mix of programming &hardware frameworks. For useful confirmation Tutor Designs Modelsim is utilized and for blend Xilinx ISE is utilized.*

KEYWORDS: *-DTMF, FFT, spilt Goertzel Algorthim without Resource Sharing Approach, spilt Goertzel Algorthim with Resource Sharing Approach., Xilinx ISE, FPGA, ZYNQ Platform.*

I. INTRODUCTION

DTMF telephone keypad generates a sinusoidal tone and it is a mixture of two frequencies i.e., row and column frequencies. The below figure shows that, how the frequencies are organized:

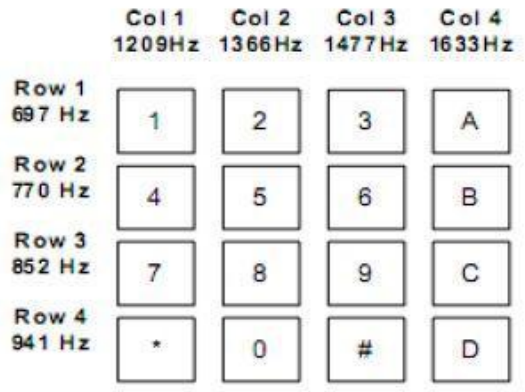


Fig.1 Keypad represents high &low frequencies:

The DTMF keypad speaks to like a 4×4 network, with every segment and each column speaks to as high and low frequencies. EX: In the event that we press a solitary key (as '2') will gives a sinusoidal tone for each of the two frequencies (1336 hertz (Hz) and 697 Hz). DTMF is for the most part used to create for media transmission gear. DTMF is where keystrokes from the phone keypad are converted into double tone motions over the sound connection. FPGA'S are parallel handling gadgets and it is utilized to enhance the execution of frameworks.

In this paper, Zynq stage assumes crucial part. It is the blend of both handling framework and programmable rationale. Here preparing framework is programming, programmable rationale is equipment. Zynq is a stage; it joins a double center ARM cortex_A9 processor with conventional FPGA rationale texture. Zynq gadgets are more adaptable. Preparing framework (PS) and Programmable rationale (PL) are utilized freely or together, and isolate control hardware is designed for both PS and PL.

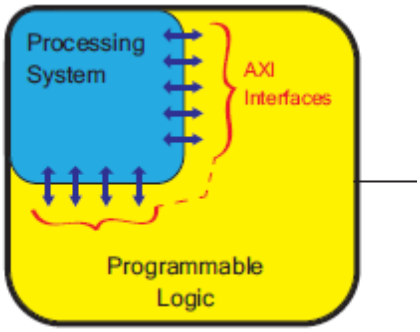


Fig 2: **Zynq Architecture**

Preparing Framework is a hard processor. It exists as a devoted and upgraded silicon component on the gadget. Hard processors can accomplish higher execution, for Zynq's ARM processor. Programmable rationale is a delicate processor like the Xilinx Miniaturized scale Blast, which is framed by consolidating components of the programmable rationale texture. The execution of a delicate processor is in this way what might as well be called some other IP piece sent in the rationale texture of a FPGA. All in all, the upside of delicate processors is that the number and exact execution of processor cases is adaptable. At least one Smaller scale Burst delicate processors can be utilized inside the PL bit of the Zynq, to work in conjunction with the ARM processor.

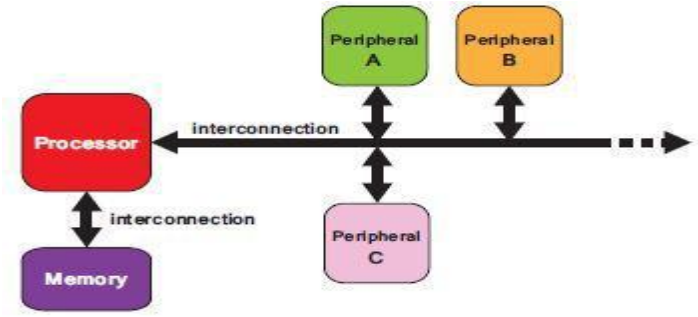


Fig.3 Hardware Architecture of Zynq

Processor acts as the focal component for equipment framework. Programming framework goes through processor. Peripherals are practical parts far from the processor. To accomplish less territory, low power, equipment improved arrangement we utilize Spilt Goertzel Calculation without RSA and Spilt Goertzel Algorthim with Asset Sharing Methodology (RSA).

For the most part this paper separated into three stages.

Stage I: In the principal stage, by utilizing Xilinx FFT center we can distinguish DTMF identification. The zone, timing and power comes about are dissected.

Stage II: In the second stage spilt Goertzel Algorthim without Asset Sharing Methodology is actualized. The range, timing and power comes about are broke down.

Stage III: In the third stage, spilt Goertzel Algorthim with Asset Sharing Methodology is examined and appropriate state machine based planning will be conveyed with constrained assets to execute split Goertzel calculation without RSA. The novel asset sharing based approach devours less power and still it can recognize productive DTMF tones.

II. IMPLEMENATION&DESIGN

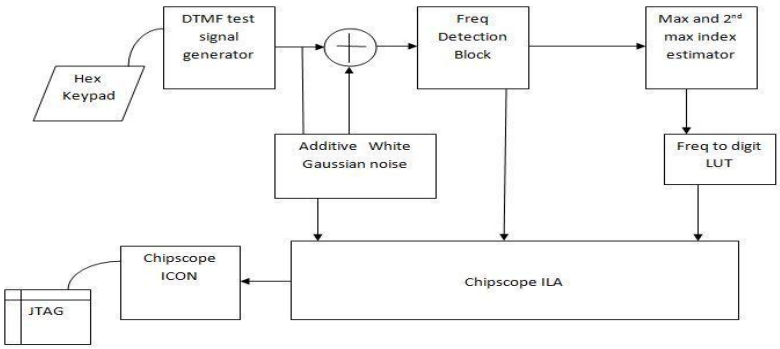


Fig.4 General Module DTMF Detection

The above figure speaks to General module DTMF Recognition. It comprises of six modules, for example, 4x4 Hex key cushion (input), Double Tone Multi Recurrence test flag generator, Added substance white Gaussian clamor, Recurrence Identification piece, Extent or list estimator and Recurrence to digit look-into table.

Hex keypad is an outer segment and it go about as contribution to DTMF module.

Recurrence Test Flag Generator square produces important transporter frequencies. FTSG is again separated into two sort's i.e, Recurrence Word Selector and Direct Advanced Synthesizer. FWS implies, it chooses recurrence as indicated by key squeezed.

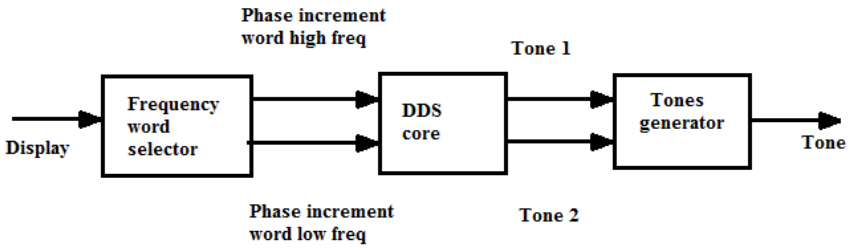


Fig. 5 Frequency Word Selector

DDS perform digital to analog conversation so that output will be in the form of analog usually a sine wave and this analog waveform combines with additive Gaussian noise then the output will be in the form of noise bits. This output gives as input to FDM i.e., Frequency Detection Module. Output will be in the form of magnitude indices. So that we can calculate 1st & 2nd max indices.

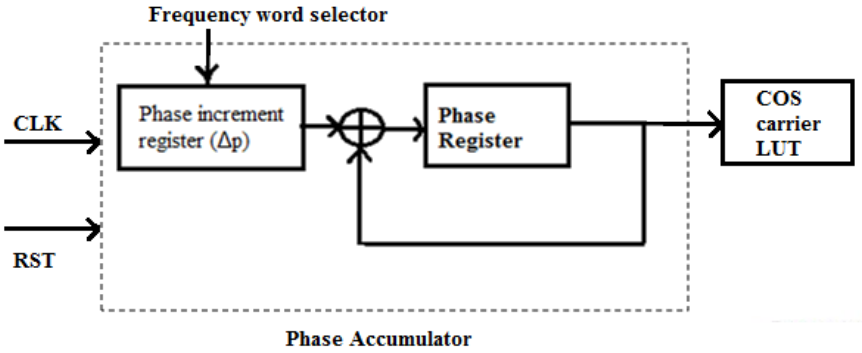


Fig. 6 Direct Digital Synthesizer

Chipscope ILA is used to monitor any internal signal of design. Chipscope ICON provides a communication path between Chipscope ILA & JTAG.

III. EXISTING PROBLEM

1. FFT- 128 core:

FFT_128 Center is utilized rather than FDB. The Quick Fourier Change (FFT) executes the Cooley-Tukey FFT calculation, and FFT is an effective calculation to register the discrete Fourier change (DFT) and it's opposite. DFT breaks down an arrangement of qualities into segments of the distinctive frequincies.DFT frequently too ease back contrast with FFT. FFT Calculations fundamentally utilized as a part of extensive variety of science from complex number math to bunch hypothesis and number hypothesis. Info information introduces in normal request and the yield information can be in either regular or bit/digit turned around arrange. In FFT it expends more power, territory, timing, and equipment. The underneath figure speaks to the FFT_128 Center as Recurrence Identification Module

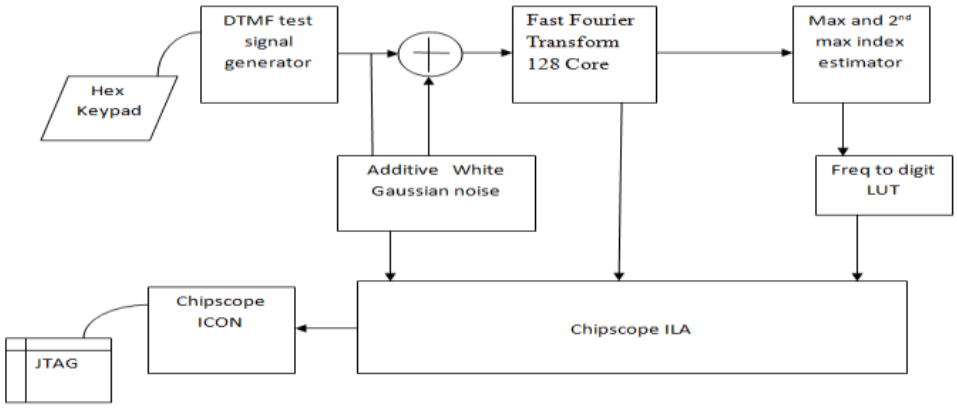


Fig.7 Block Diagram with FFT-128 Core as Frequency Detection Module

IV. PROPOSED SOLUTION

1. Spilt Goertzel Algorthim without Resource Sharing Approach.

The spilt Goertzel Algorthim without Resource Sharing Approach is a DSP technique; it is used to identify the frequency components of a signal, and published by Dr. Gerald Goertzel in 1958. Here spilt Goertzel Algorthim without Resource Sharing Approach module is added instead of FDB in DTMF Detection General Module.

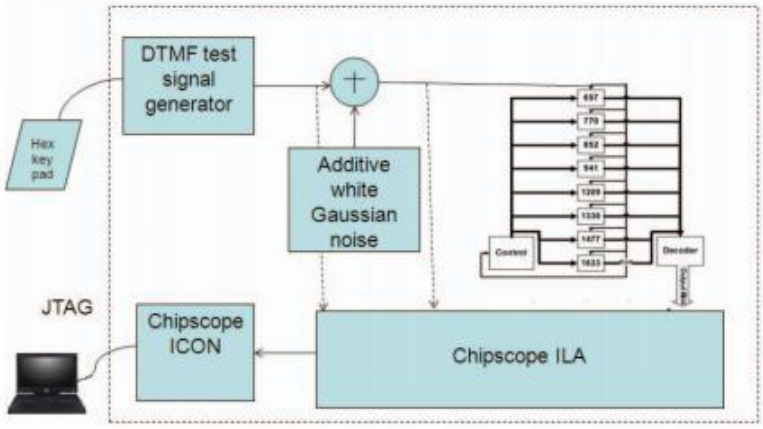


Fig.8 Spilt Goertzel Algorthim without Resource Sharing Approach as Frequency Detection Module

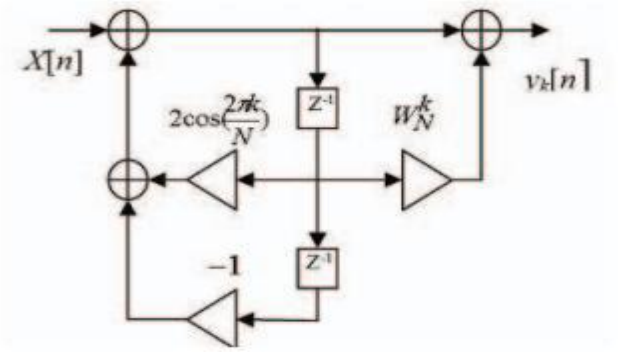
Spilt Goertzel Algorthim without Resource Sharing Approach is used to reduce the no. of real value multiplications compare to DFT. In spilt Goertzel Algorthim without Resource Sharing Approach specific &predetermined frequencies will use. So that it consumes less area, low power. The Goertzel Algorthim performs tone detection using much less CPU horse power than the Fast Fourier Transform. Spilt Goertzel Algorthim without Resource Sharing Approach series for a length of N is:

$$H_k(Z) = \frac{1 - e^{J\frac{2\pi K}{N}} z^{-1}}{\left(1 - e^{J\frac{2\pi K}{N}} z^{-1}\right)\left(1 - e^{J\frac{2\pi K}{N}} z^{-1}\right)}$$

$$K = 0, 1 \ldots\ldots N\_1$$

2. Spilt Goertzel Algorthim with Resource Sharing Approach.

Spilt Goertzel Algorthim with Resource Sharing Approach is an approach that, similar block of operations can assign. For example, +, to a common net list cell. Net list cells are be the resources; here net lists will be shared, so that it consumes less hardware. By using spilt Goertzel Algorthim without RSA we can implement spilt Goertzel Algorthim with RSA. In Goertzel algorithm all eight determined frequencies are appear, In spilt Goertzel Algorthim with RSA only 2 frequencies will used so that in spilt Goertzel Algorthim RSA consumes less hardware. The below figure shows spilt Goertzel Algorthim with Resource Sharing Approach.



V. SIMULATION AND SYNHESIS RESULTS

The below Figures represent the Simulation results for FFT, Spilt Goertzel Algorthim without Resource Sharing Approach, Spilt Goertzel Algorthim with Resource Sharing Approach.

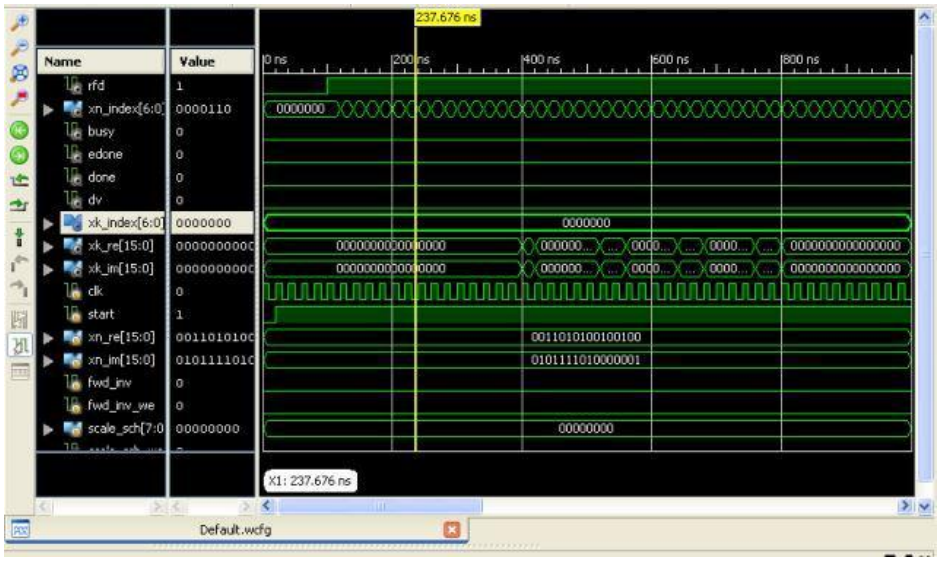


Fig.10 simulation Results of FFT

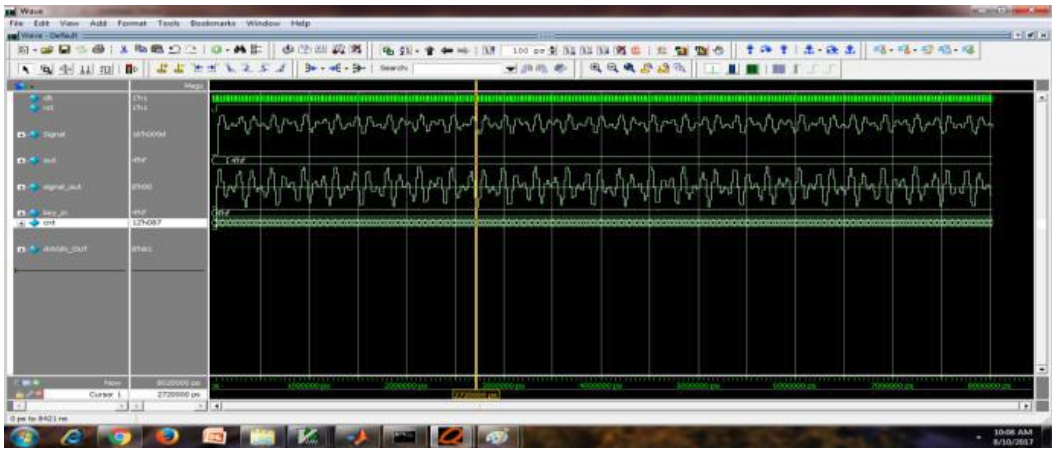


Fig. 11 Simulation Results of Spilt Goertzel Algorthim without Resource Sharing Approach

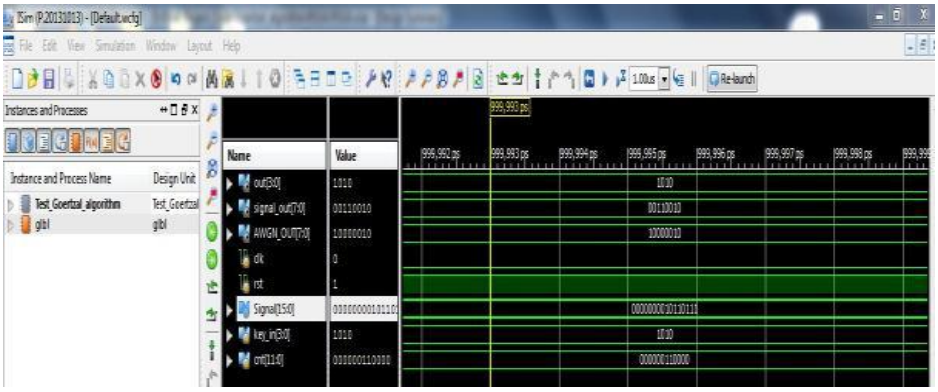


Fig.12 Simulation Results of Spilt Goertzel Algorthim with Resource Sharing Approach.

The Module, RTL Schematic, Device Utilization Summary are shown below by screenshots for FFT

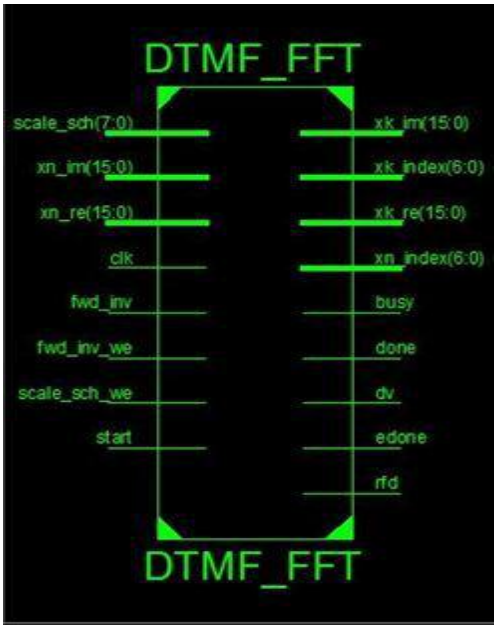


Fig.13 Module of FFT

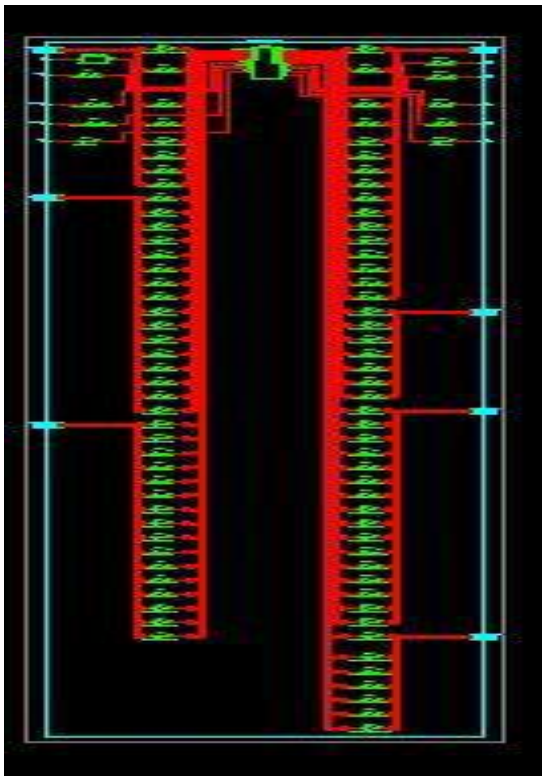


Fig.14 RTL Schematic of FFT

Table_1: Device utilization Summary of FFT

Device Utilization Summary(estimated values)			
Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	1991	35200	5%
Number Of Slice LUTs	1727	17600	9%
Number Of fully used	1527	2191	69%

LUT-FF pairs			
Number Of bonded IOBS	96	100	96%
Number Of Block RAM/FIFO	4	60	6%
Number Of BUFG/BUFG CTRLS	1	32	3%
Number Of DSP 48E1S	9	80	11%

The below figures represent Module, RTL Schematic, Device Utilization Summary for Spilt Goertzel Algorthim without Resource Sharing Approach.

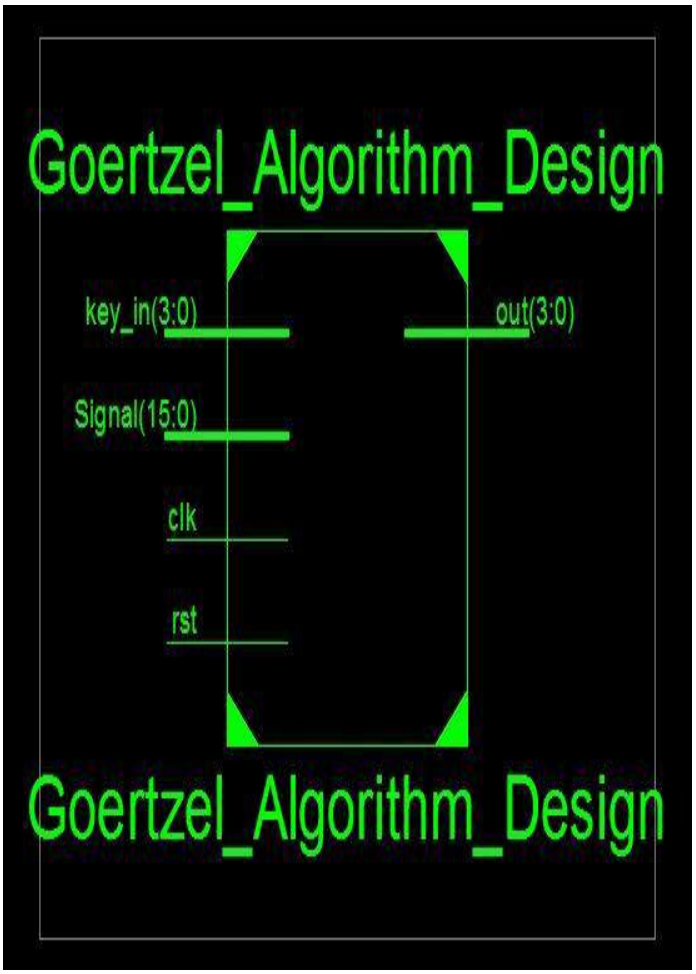


Fig. 15 Spilt Goertzel Algorthim without Resource Sharing Approach. Module

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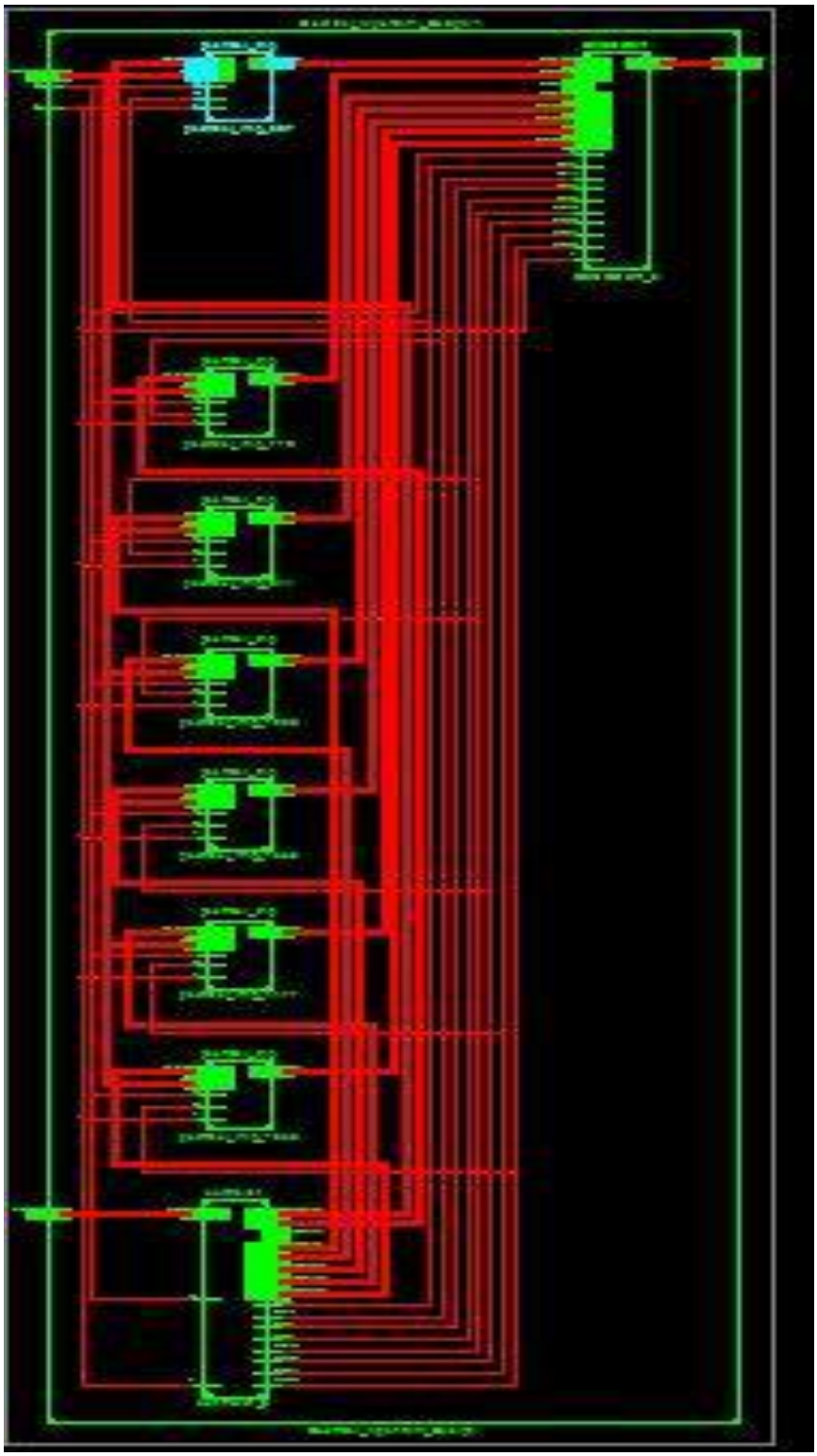

Fig.16 RTL Schematic of Spilt Goertzel Algorthim without Resource Sharing Approach.

Table_2: Device Utilization Summary of Spilt Goertzel Algorthim without Resource Sharing Approach.

Device Utilization Summary(estimated values)			
Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	1991	35200	5%
Number Of Slice LUTs	1727	17600	9%
Number Of fully used LUT-FF pairs	1527	2191	69%
Number Of bonded IOBS	96	100	96%
Number Of Block RAM/FIFO	4	60	6%
Number Of BUFG/BUFGCTRLS	1	32	3%
Number Of DSP 48E1S	9	80	11%

The below figures represent Module, RTL Schematic, Device Utilization Summary for Spilt Goertzel Algorthim with Resource Sharing Approach.

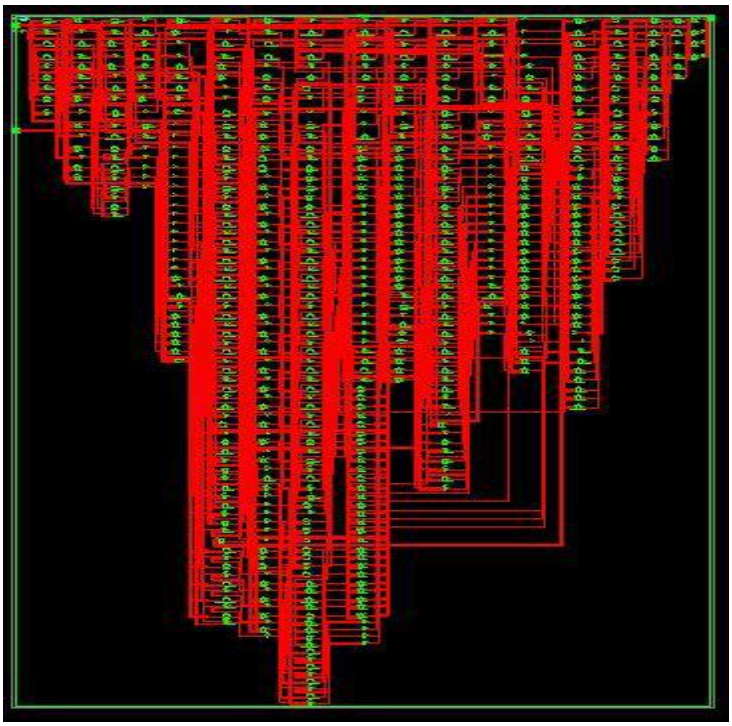

Fig. 17 RTL Schematic of Spilt Goertzel Algorthim with Resource Sharing Approach.

Table _3: Device Utilization Summary for Spilt Goertzel Algorthim with Resource Sharing Approach.

The below figure represents the Power Distribution for Spilt Goertzel Algorthim without Resource Sharing Approach., Spilt Goertzel

Logic Utilization	Used	Available	Utilization
Number Of Slice Registers	1	35200	0%
Number Of Slice LUTs	78	17600	0%
Number Of fully used LUT-FF pairs	12	79	15%
Number Of bonded IOBS	26	100	26%
Number Of BUFG/BUFGCTRLS	1	32	3%
Number Of DSP 48E1S	6	80	7%

Algorthim with RSA.

Table_5: Power results for Spilt Goertzel Algorthim with Resource Sharing Approach.

Device	
Family	Zynq - 7000
Part	Xc7z010
Package	Clg400
Temp Grade	Commercial
process	Typical
Speed Grade	-3

On-chip	Power(w)	Used	Available	Utilization (%)
Clocks	0	1	----	------
Logic	0	63	17600	0
Signals	0	650	-----	------
DSPS	0	21	80	26
IOS	0	26	230	11
Leakage	0.01			
Total	0.01			

Thermal Properties	Effective TJA(c/w)	Max Ambient(c)	Junction Temp(c)
	5.5	84.5	25.5

Supply Power(w)	Total	Dynamic	Quiescent
	0.100	0.00	0.100

Table_4: Power results for Spilt Goertzel Algorthim without Resource Sharing Approach.

Device	
Family	Zynq - 7000
Part	Xc7z010
Package	Clg400
Temp Grade	Commercial
process	Typical
Speed Grade	-3

On-chip	Power(w)	Used	Available	Utilization (%)
Clocks	0	1	----	------
Logic	0	61	17600	0
Signals	0	259	-----	------
DSPS	0	6	80	8
IOS	0	26	230	11
Leakage	0.01			
Total	0.01			

Thermal Properties	Effective TJA(c/w)	Max Ambient(c)	Junction Temp(c)
	5.5	84.5	25.5

Supply Power(w)	Total	Dynamic	Quiescent
	0.100	0.00	0.100

VI. CONCLUSION

In this task, we identify DTMF based FPGA usage utilizing Spilt Goertzel Calculation with improved Asset Sharing Methodology. In the primary stage, by utilizing Xilinx FFT center we recognized DTMF recognition. The territory, timing and power comes about are dissected. The hindrance of the DFT system is that it requires every symphonious to be ascertained independently, which requires significantly more preparing power, hardware& memory. In the second stage the split Goertzel calculation without Asset Sharing Methodology examination is completed. In the following stage the split Goertzel calculation with Asset Sharing Methodology is contemplated and appropriate state Machine based booking will be conveyed with restricted assets to actualize split Goertzel calculation without Asset Sharing Methodology. To recognize DTMF identification another sort of ZYBO board ZYNQ 7000 arrangement FPGA is utilized. In FFT Add up to territory expended i.e; add up to doors utilized 2369, memory utilization 445818 kilo bytes and speed is 1.5ns. In FFT it devours more zone, control, speed. In Split Goertzel Algorthim without Asset Sharing Methodology; Add up to territory expended i.e; add up to entryways utilized 33, memory utilization 445818 kilo bytes and speed is 4.123ns. In Split Goertzel Algorthim with Asset Sharing Methodology; Add up to territory expended i.e; add up to doors utilized 20, memory utilization 445818 kilo bytes and speed is 4.123ns.In Part Goertzel Algorthim with Asset sharing Methodology can recognize the approaching recurrence inside a ±1.5% balance go. This calculation does not check for flood issues. With the goal that it expends less territory, power& memory.

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