International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue14
November 2017

Design of Register File Using Reversible Logic

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Abstract: *Register file is the central perspective in PC memory unit. Eight bits (one memory unit) brings about a solitary enroll and 32 of such enlist make up an enlist record. In this paper we have displayed the outline of an entire enroll document utilizing reversible rationale plan. It comprises of decoder, multiplexer, memory unit, read and compose units. This has been confirmed utilizing Verilog HDL. Notwithstanding that, we have executed the enroll record in the outline of Content Addressable Memory (CAM) as an application.*

I. INTRODUCTION

Reversible registering is a model of figuring where the computational procedure to some degree is reversible, i.e., time-invertible. Reversible registering is for the most part considered a flighty type of figuring. A register files is a variety of processor enlists in a focal handling unit (CPU). Present day incorporated circuit-based enroll documents are normally actualized by method for quick static RAMs with numerous ports. Such RAMs are recognized by having devoted perused and compose ports, though standard multi ported SRAMs will generally read and compose through similar ports.

In current situation, the reversible rationale configuration drawing in more enthusiasm because of its low power utilization. Reversible rationale is vital in low-control circuit outline. As per Landauer, the vitality of each piece is equivalent to kT*ln2 (where 'k' is the Boltzman steady and 'T' is the temperature in Kelvin). [1]With the loss of each piece, kT*ln2 of vitality is lost. So as to spare this vitality, Reversible rationale entryways are executed. It has same number of information and yield entryways and every one of the data sources bits can be recouped, accordingly sparing energy. There are different reversible doors accessible, yet we have fundamentally utilized Feynman Gate, Fredkin entryway, Toffoli door . A reversible rationale door is a n-input n-yield rationale gadget with coordinated mapping. To actualize reversible calculation, gauge its cost, and to judge its cutoff points, it is formalized it as far as door level circuits. Reversible registering will likewise prompt change in control proficiency. Power proficiency will on a very basic level influence the speed of circuits, for example, nano circuits and along these lines the speed of most figuring applications. Part I is prologue to the reversible rationale outline.

II. LITERATURE SURVRY.

Content-addressable memory (cam) circuits and architectures: A tutorial and survey.

We survey recent developments in the design of large-capacity content-addressable memory (CAM). A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high-speed table lookup. The main CAM-design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. In this paper, we review CAM-design techniques at the circuit level and at the architectural level. At the circuit level, we review low-power match-line sensing techniques and search-line driving approaches. At the architectural level we review three methods for reducing power consumption.

Design of testable reversible sequential circuits.

In this paper, we propose the design of two vectors testable sequential circuits based on conservative logic gates. The proposed sequential circuits based on conservative logic gates outperform the sequential circuits implemented in classical gates in terms of testability. Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1's, and all 0's. The designs of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops are presented. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the need for any type of scan-path access to internal memory cells. The reversible design of the DET flip-flop is proposed for the first time in the literature. We also showed the application of the proposed approach toward 100% fault coverage for single missing/additional cell defect in the quantum-dot cellular automata (QCA) layout of the Fredkin gate. We are also presenting a new conservative logic gate called multiplexer conservative QCA gate (MX-cqca) that is not reversible in nature but has similar properties as the Fredkin gate of working as 2:1 multiplexer. The proposed MX-cqca gate surpasses the Fredkin gate in terms of complexity (the number of majority voters), speed, and area.

Theory, synthesis, and application of adiabatic and reversible logic circuits for security applications.

Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Adiabatic logic is a design methodology for reversible logic in CMOS where the current flow through the circuit is controlled such that the energy dissipation due to switching and capacitor dissipation is minimized. Production of cost-effective Secure Integrated Chips, such as Smart Cards, requires hardware designers to consider tradeoffs in size, security, and power consumption. In order to design successful security-centric designs, the low-level hardware must contain built-in protection mechanisms to supplement cryptographic algorithms such as AES and Triple DES by preventing side channel attacks, such as Differential Power Analysis (DPA). Dynamic logic obfuscates the output waveforms and the circuit operation, reducing the effectiveness of the DPA attack. In this dissertation, I address theory, synthesis, and application of adiabatic and reversible logic circuits for security applications. First, we present a mathematical proof to demonstrate that reversible logic can be used to design sequential computing structures. Next, a novel algorithm for synthesis of adiabatic circuits in CMOS is presented. This approach is unique because it correlates the offsets in the permutation matrix to the transistors required for synthesis, instead of determining an equivalent circuit and substituting a previously synthesized circuit from a library. Using the ESPRESSO heuristic for minimization of Boolean functions method on each output node in parallel, we optimize the synthesized circuit. It is demonstrated that the algorithm produces a 32.86% improvement over previously synthesized circuit benchmarks. For stronger mitigation of DPA attacks, we propose the implementation of Adiabatic Dynamic Differential Logic for applications in secure IC design. A Performance Adiabatic Dynamic Differential Logic (PADDL) is presented for an implementation in high frequency secure ICs. This method improves the differential power over previous dynamic and differential logic methods by up to 89.65. Then, we present an adiabatic S-box which significantly reduces energy imbalance compared to previous benchmarks. The design is capable of forward encryption and reverse decryption with minimal overhead, allowing for efficient hardware reuse.

III. REVERSIBLE CIRCUITS

Reversible rationale circuits have been first inspired in the 1960s by hypothetical contemplations of zero-vitality calculation and additionally pragmatic change of bit-control changes in cryptography and PC designs. Since the 1980s, reversible circuits have pulled in enthusiasm as parts of quantum calculations, and all the more as of late in photonic and nano processing innovations where some exchanging gadgets offer no flag gain. Surveys of reversible circuits, their development and enhancement and in addition late research challenges are accessible.

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Feynman / CNOT Gate: The Reversible 2*2 gate with Quantum Cost of one, having mapping input (A, B) to output (P = A, Q= A^B) .

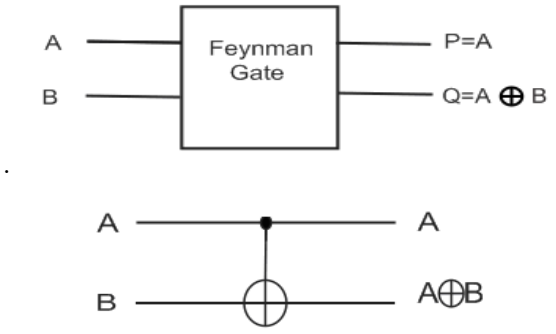

Fig.1. Reversible Feynman/CNOT gate ,Quantum equivalent of Feynman gate

Fredkin Gate:

The Fredkin gate (additionally CSWAP entryway) is a computational circuit reasonable for reversible registering, created by Ed Fredkin. It is all inclusive, which implies that any sensible or number juggling operation can be built completely of Fredkin entryways. The Fredkin door is the three-piece entryway that swaps the last two bits if the primary piece is 1.

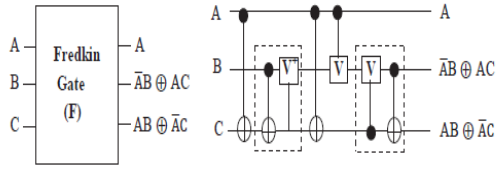

Fig .2. Fredkin Gate, Graphical representation

It has the helpful property that the quantities of 1s are saved all through, which in the billiard ball demonstrate implies a similar number of balls are yield as information. This relates pleasantly to the protection of mass in material science, and demonstrates that the model isn't inefficient.

ToffoliGate:

In software engineering, the Toffoli entryway (additionally CCNOT door), designed by TommasoToffoli, and is a general reversible rationale entryway, which implies that any reversible circuit can be built from Toffoli doors. It is otherwise called the "controlled controlled-not" door, which depicts its activity.

Shockingly, there are reversible capacities that can't be processed utilizing quite recently those doors. At the end of the day, the set comprising of NOT and XOR doors isn't all inclusive. On the off chance that we need to process a self-assertive capacity utilizing reversible entryways, we require another door. One probability is the Toffoli entryway, proposed in 1980 by Toffoli.

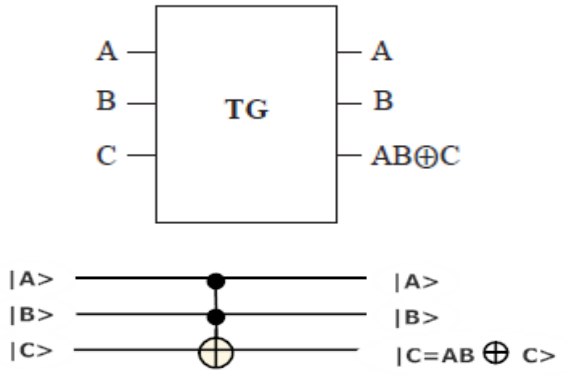

Fig.3. Toffoli Gate , Graphical Representation

The Toffoli door is general; this implies for any Boolean capacity f(x1, x2, ..., xm), there is a circuit comprising of Toffoli entryways which takes x1, x2, ..., xm and some additional bits set to 0 or 1 and yields x1, x2, ..., xm, f(x1, x2, ..., xm), and some additional bits (called trash). Basically, this implies one can utilize Toffoli doors to construct frameworks that will play out any coveted Boolean capacity calculation in a reversible way.

IV. DESIGN OF REGISTER FILE

The center component in PC memory is Register File. As said before, each enroll record contains 32

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registers and each enlist is made of n byte. Here, we have demonstrated an enlist having 1 byte: 8 bits.

The general working is as per the following:

The control flag is given to the primary contributions of two Feynman door and second info are relegated 1(constant). The yields of Feynman door 1 are READ 1 and WRITE . READ 1 goes about as an empower/choice flag for first multiplexer .Similarly, the principal yield from Feynman entryway 2 goes about as select flag for second multiplexer, yielding READ DATA 2. WRITE signal is associated with the AND doors to empower Write operation on to the memory cell. The Multiplexer when empowered peruses the composed information from the chose enlist. The Register record piece outline is appeared in the Fig. 4

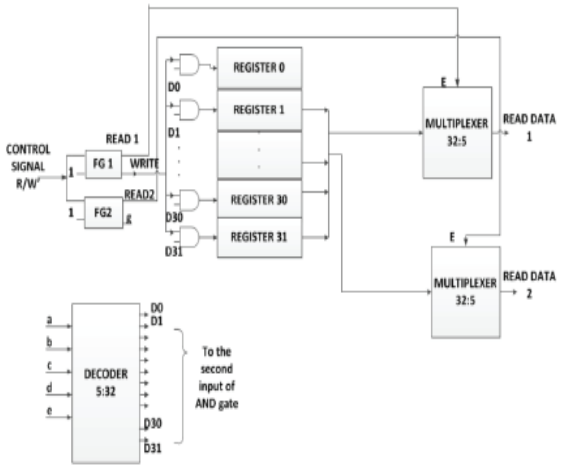

Fig. 4. Register File Block Diagram

Operation involved

The processor interfaces with the memory unit through two unique operations, in particular: Read and Write. The clarification for every operation is given beneath.

1) Read operation: When the control flag is high , the READ 1/READ2 flag acts as the select line for the Multiplexer. Once the multiplexer is empowered , the information which put away in the relating register is picked and influenced accessible on READ DATA 1/To peruse DATA 2 line. The Fig. 5 gives the diagrammatic way to deal with read operation.

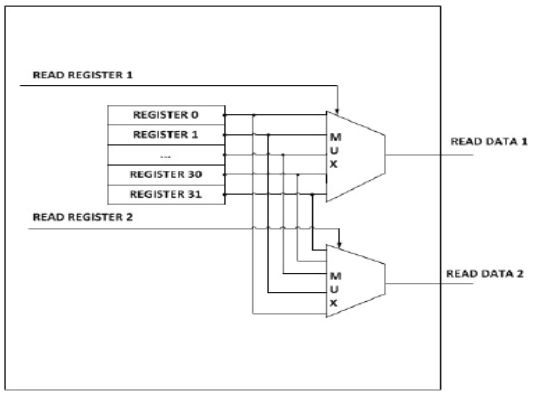

Fig. 5. Read operation [12]

1) Write operation: When control flag is low , the WRITE flag is enabled(READ 1 and READ 2 is impaired) . The WRITE empower the AND door. One of the contribution to AND entryway is the information from the decoder. Enroll number is bolstered to a 5:32 decoder . Each yield of AND door goes about as code in enlist record and the 32 bit enroll information is specifically sustained into the enlist document. Fig. 6 demonstrates the Write operation outline.

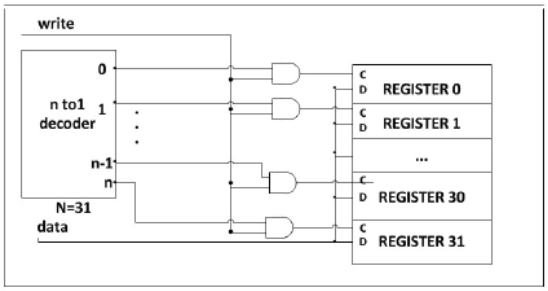

Fig. 6. Write operation [12]

Design of individual components used in the Block Diagram

1) Multiplexer (Enocders) utilizing MFRG door (32:1): Multiplexer, a combinational circuit, is utilized as information selector. It has many sources of info and one yield. Contingent on the select esteem, relating information line will be accessible at the output. We have proposed a 32:1 multiplexer utilizing altered Fredkin door which has a diminished quantum cost and power and have a fundamental part in read impact of enroll document .we have 2 perused yield which requires two 32:1 multiplexer . For multiplexer piece we alter the Frekdin door. The info vector, Iv= (A ,B,C). [3]

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This plan comprises of 5 phases. In first stage A will be select line and B and C are two information inputs. The main yield of each door which will be the select line to next MFRG of same stage. The second yield is sustained as second info for the succeeding stage MFRG doors. The third yield will be a waste yield. This rehashes for each stage. In the fifth stage, second yield will be the required multiplexed yield.

The yield of these two 32:1 multiplexer will be READ DATA 1 and READ DATA 2. The outcomes are recreated in Xilinx ISE by utilizing Verilog HDL dialect. The outline is appeared in the Fig.7

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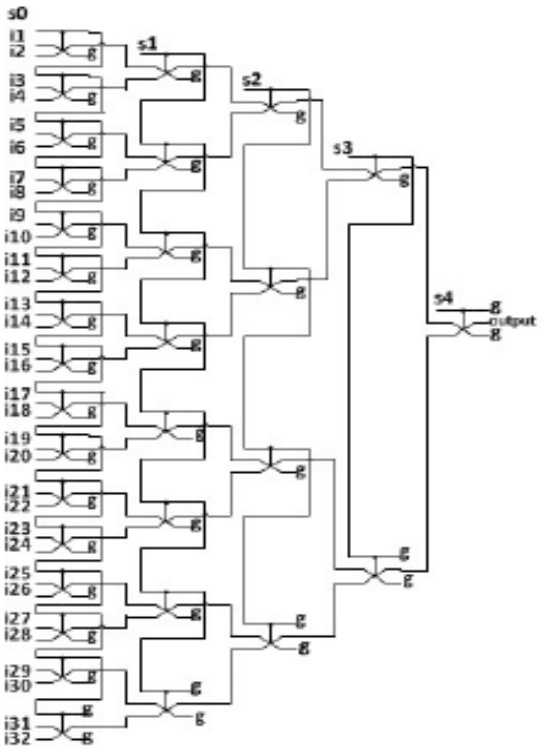

Fig. 7. Encoder

*1)**Decoder for a Register File:***Decoder, likewise a combinational circuit, has n inputs and 2^n yields. As, the name says, it disentangles the coded inputs. [8]

The proposed configuration as appeared in Fig. 8 is a 5 to 32 decoder, manufactured utilizing one Feynman door and thirty Fredkin entryways.

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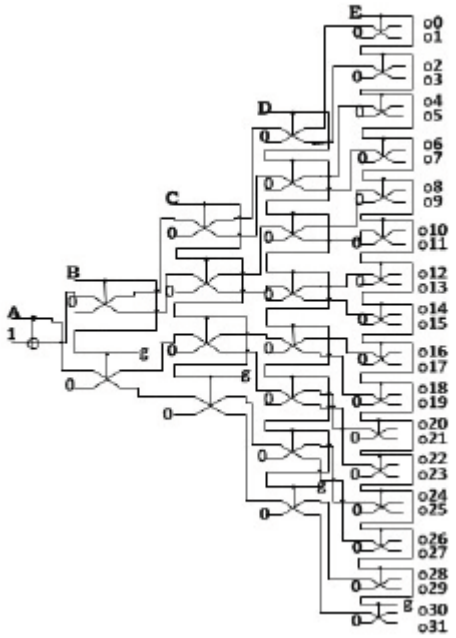

an and0 are offered contribution to the Feynman door to deliver an and a. At each stage , new sources of info are presented. Each stage has2n,n=0,1,2,3,4 number of entryways. 'a'and '¯a' nourished as the contribution to the following two Fredkin entryway alongside input ' b' and ancilla0.

For the following stage, 4 contribution from these two Fredkin entryways (second and third yield of each Fredkin door) are given to the second information door of the Fredkin and the 0 is nourished as contribution to the third information door of the Fredkin. This is rehashed for the next two stages as shown in the figure. It has 4 garbage values and 31 ancilla. The yield toward the end fourth stage are, ó¯ ¯b c¯ d¯e¯ , a b c de , a b c d e ... abcde , abcde, abcde from 0 to 31.

3) AND entryway utilizing Toffoli door: Toffoli door is 3*3 reversible rationale door. The main information is compose flag and decoder each yield is given as second contribution for each entryway. The third information is a steady 0. The third yield gives the ANDed yield of the initial two data sources. This is nourished as a contribution to every memory cell of an enlist document. The first and second yields are rubbish yields.

4) Memory Cell: The arrangement of the memory cell is as showed up in the Fig. 9 One Fredkin entryway and one Feynman gateway are used to plot one D-snare [4] [6]. Yield from the AND door isassociated with the main contribution of the Fredkin entryway. Information tobe put away is associated with the second contribution of this entryway. Initial two yield entryway are waste esteem. The third entryway is given to the Feynman door , to deliver criticism Q. This criticism is associated with the third contribution of the Fredkin door. There are 8 such D-locks [11] in arrangement to shape an enlist.

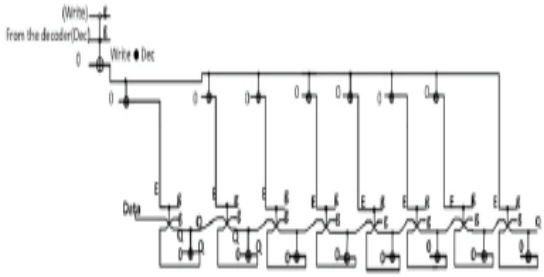

Fig. 9. 8 bit Register Block Diagram

There are 16 ancilla and 18 trash esteems. The quantity of entryways, junk esteems, number of ancilla, quantum cost ,quantum deferral and profundity of every segment planned above is arranged in the Table I.

TABLE I PERFORMANCE PARAMETER OF ALL THE COMPONENTS

PROPERTY	Multiplexer	Decoder	AND Gate	8 bit memory cell.
Garbage values	36	4	2	18
Number of Gates	31	33	1	16
Number of ancilla	0	31	1	16
Quantum cost	124	121	5	55
Quantum delay	25Δ	24Δ	5Δ	15Δ
Quantum depth	5	5	1	3

V. APPLICATION OF REGISTER FILE IN CONTENT ADDRESSABLE MEMORY

CAM - Content addressable memory is a unique sort of PC memory utilized as a part of fast looking application .It is otherwise called cooperative memory or acquainted stockpiling A. General working: The outline of the CAM is given in the Fig.8 It comprise of a Look up table (LUT), encoder, decoder and Register record (memory) [5]. At the point when the client gives an inquiry word (input), its address is sought in the Look Up Table to check whether the hunt word is put away in it. On the off chance that the hunt word is

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discovered, the data is sent to the encoder and in the end to the decoder. The decoder, unravels the data and returns the address of word put away in the memory. This decoder yield is encouraged to the enroll record which gives the area of the pursuit word (yield).

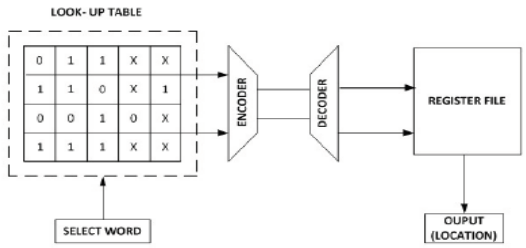

Fig. 10. CAM Block Diagram

The outline of every part in detail is introduced underneath: The Look up table comprise of the customary CAM cells which utilizes NOR doors. Here a 5x4 cell cluster is masterminded(4 words with each containing 5 bit). The match line is chosen, if a match is found and encoder gives the address area in the coordinated line. The query table is as appeared in Fig 11

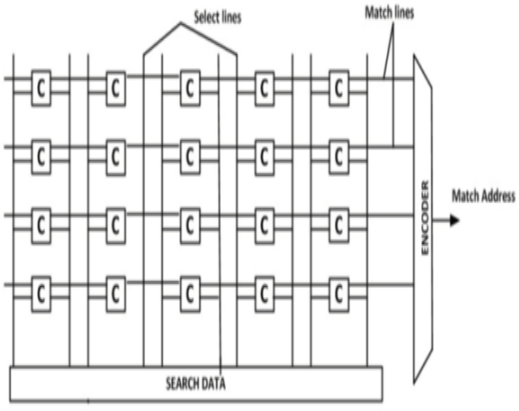

Fig. 11. 5x4 LUT

B. Design of Encoder and Decoder

The plan of the encoder as appeared in fig and decoder appeared in figure.

ENCODER: The plan is appeared in Fig 10 utilizes 3 doors. Its quantum cost is 27. The deferral of the circuit is 10¨, while the profundity is 2.It doesn't have any ancilla. DECODER: The circuit is as appeared in Fig. 11 It has 3 entryways, 1 yield is a waste esteem. Quantum cost, quantum postponement and quantum profundity is 22, 9¨ and 2 individually.

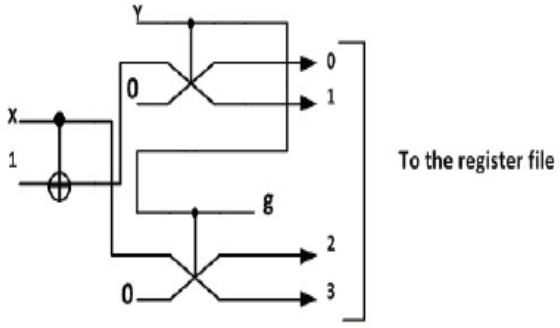

Fig. 12. Decoder used in CAM

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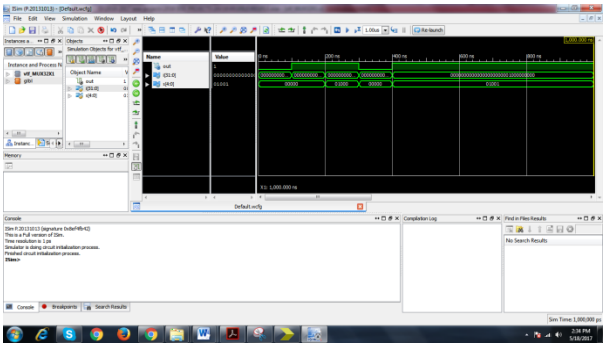
VI. RESULTS

Simulated outputs for proposed Reversible Multiplexer(Encoder).



RTL schematic of Internal block of proposed Reversible Multiplexer(Encoder).

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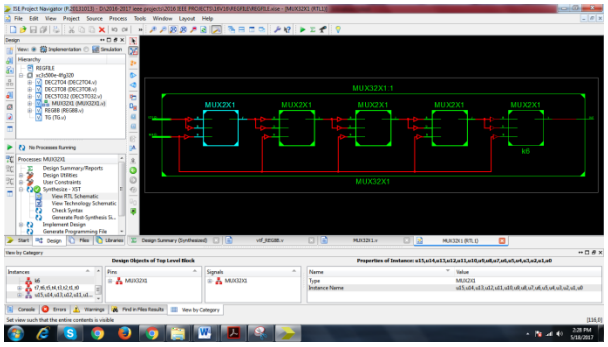
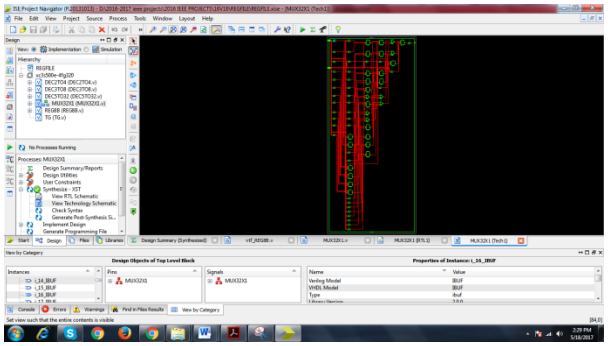


Technology schematic of Internal block of proposed Reversible Multiplexer(Encoder).



Design Summary.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	12	4656	0%
Number of 4 input LUTs	22	9312	0%
Number of bonded IOBs	38	232	16%

CONCLUSION

This paper proposed the total plan of Register File which utilizes D-Latch as the memory unit. This is beneficial in light of the fact that, it is non concurrent. Once the control flag is sent by the control unit of the processor, the information is composed and perused into/from the memory without requiring extra clock timing compel. This enlist document is utilized as an application in the plan of the CAM.

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