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Design A Semiconductor Nanowire Development With Performance Limits

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ABSTRACT: *Semiconductor nano wires are the unique materials that explore the phenomena of nanoscale. Basically, nano wires are extensively used in the properties of electronic, mechanical and electrochemical. By using the top down techniques we can yield the device performance in an excellent way. In this first basic nanowire field-effect transistor structures are introduced and these are obtained from the results of both p-channel and n-channel homogenous composition nanowires. Next one is about the description of nanowire heterostructures; it consists of certain limiting factors that can demonstrate the performance of nanowire transistor. Third one is to fabricate the devices and circuits in the organization of nanowires. Fourth one is to introduce the concept of crossbar nanowire circuits. This circuit gives the results for both the transistors and non volatile circuit devices. It not only discusses about the result but also describes the unique approaches of multiplexing and de multiplexing. These unique approaches are enabled by the coded nanowire. Coming to fifth one, in this we discuss about the application of the silicon thin flim narrow wire array transistors. Basically, silicon thin flims are fabricated on the foreign substrates like glass and stainless steel. These arrays are of low cost and describe the results for high frequency ring oscillator and transparent device arrays. At last we discuss about the 3-D heterogeneous integration, it is a unique approach which enables the multi functional nano wires in the bottom up approach.*

I.INTRODUCTION

Semiconductor nanowires are extensively used from past two decades. Basically, one dimensional nano structures likes wires, tubes, rods are used from past decades and it consists of electronic, thermal, mechanical and magnetic properties. Advanced materials of nano structures are introduced last ten years ago. Coming to the present generation field novel synthetic routes and fundamental characterization are emphasized. Now we are going to focus on the development of the applications like electronic, photonic, mechanical, biological, and energy-conversion. To develop this nanowire structure we use bottom up mechanism. In this bottom up synthetic routes, we use both gas phase and solution phase chemistry. These are enabled with new material systems. In CMOS devices nano wires are most extensively used and also Number of key factors are used in this nanowire research. First these semiconductor nanowires are prepared from the large scale integrated systems. Second one is when we Compared with the top down nanofabricated devices with bottom up synthesized devices, the bottom up nano wire materials gives well controlled size and high carrier mobility. It not only controls the size but also reduces scattering in the both radial and axial nanowire hetero structures. At last the thicknesses of the nano wires are controlled below 10nm. Basically, in MOSFETS it is difficult to implement the gate length. So, to solve this NWFETS are introduced on the silicon on insulator (SOI) MOSFET. Now the surface potential in the FET channel is described by the 1-D modified poisson ratio. In this poisson ratio the length L is larger than the five to ten times the wavelength. This equation minimizes the short channel effects. At last to obtain the good electricity integrity gate length should be reduced. Coming to the NWFETS, t_{si} is the diameter of the nanowire which reduces to nanometers to obtain conventional lithography process. The below figure (1) shows the schematic view of the NWFETs.

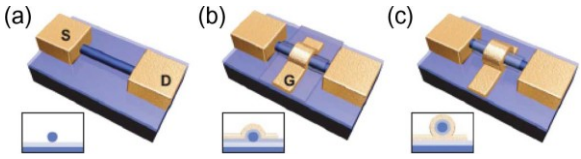

Fig. 1. Schematic of NWFETS with (a) back gate, (b) semi cylindrical top gate, and (c) cylindrical gate-all-around configurations. The nanowire is dark blue, gate-dielectric is light purple, and source (S), drain (D), and top-gate (G) electrodes are gold. Insets show device cross section at midpoint between source and drain.

Basically, these are the straight forward implementation of gate structures. They enable the

free standing nano wire structures. For high performance operation the drive current should be increased. A well known method to produce the nanowires is nanocluster catalyzed vapor–liquid–solid (VLS) growth process. In this we use nanoclustor to define the growth of both nucleations And subsequent nanowire growth. Coming to the vaphor phase materials, they provide the chemical vapor deposition (CVD), chemical beam epitaxy (CBE), laser ablation, or thermal evaporation reactor. As we discussed earlier that nano wire growth mechanism is used to produce nano wires but it is not widely used instead of this we use the nano cluster catalyzed VLSI growth approach. So this process gives the way to find the ability of the nano wires and tune the diameter. This makes the nanowires more flexible and it controls the nanowire dimensions, crystal structure, composition, growth pattern and structural complexity.

II. HOMOGENEOUS NANOWIRE-BASED DEVICES

In this we are going to study about the homogenous structures of nano wires. In this we not only discuss about the structure but also we discuss about the composition and silicon nano wires. Here the silicon in semiconductor industry gives the control of structures in a high level way and the doping level in this process are demonstrated in the silicon nano wire growth studies. In this we not only use the silicon material but also germanium, InAs, GaN, and metal oxides. Let us discuss this in detail manner.

A. SiNWs, Early Days

The development of silicon nano wires came into the process in the year 1998. By using laser ablation method the SiNWs diameters are arranged between < 20 nm and lengths > 1 μm. In this the growth of nano wires are obtained from the nano scale clusters. Because of this nano scale clusters the growth is increased. The order of this silicon nano wires is of 0.1 μm. Silicon nano wires have two attractive properties they are electrical and optical. The silicon nano wires are grown from the vapour liquid solid reactions. SiNW building blocks give high performance and low cost processing. In this we use electro less etching techniques for well controlled features. Basically the both VLS and VSS techniques are used to prepare the single crystal substrates which consist of better control of growth direction. By using the VLS and VSS techniques we can trap the electrons and holes.

To achieve the high performance in silicon nanowires uniform doping should be done. The doping methods consist of thermal diffusion and ion implementation and in-situ implementation. The physical properties of silicon nano wires employ the building blocks to make the process more effective. Coming to the energy gap of silicon nano wires are tuned to increase with the decrease of diameter of silicon nanowires. High carrier mobility is essentially used to increase the performance. Generally, SiNWs have high surface to volume ratio. Some of the devices are configured using the p- n diodes and bipolar transistors.

B. CVD Growth of SiNWs

To control the doping level of SiNWs we use the CVD based nanowires. In these electrical properties SiNWs gives the realization of high performance p and n channel SiNWs FETs. This entire process is shown in below figure (2). In this we use device geometry where a SiNW is deposited on the sio_2 substrate.

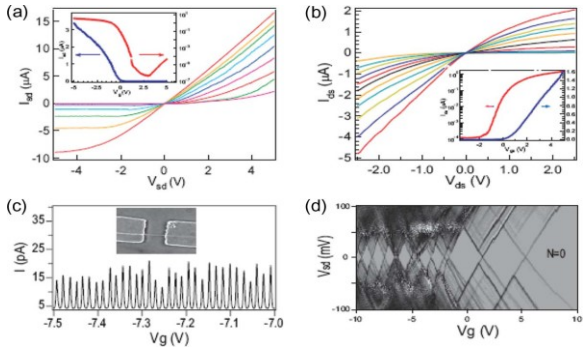

Fig. 2. (a)– (b) Transistor characteristics of p- and n-type nanowires. Insets show transfer characteristics of the back-gated devices. (c) CB oscillations observed at 4.2 K in molecular-scale diameter SiNW; inset shows SEM image of the *L* 400 nm device. (d) $\partial I/\partial Vsd - Vsd - Vg$ for a *L* 50 nm device at 4.2 K, where carriers are completely depleted ($N = 0$) for $Vg > 5.5$ V. Adapted from [13], [31], and [27].

In this the metal electrodes are fabricated from the photolithography process. In this process the both drain and source electrodes serve as an FET structure. Here the improved version of doping level gives about the desired doping level and uniform device performance. The metal contacts are most widely used in the NWFETs. It is not only used in the NWFETs but also used in the devices of schottky barrier devices. If it is positive metal then schottky barrier gives the effect of metal work function and Fermi level pinning by surface states. The effect of contrast resistance is observed in both p and n type SiNWs. Sometimes the schottky barrier contacts acts

as the tunnel barriers to allow the properties of SiNWs devices. From figure 2(a) we can observe the transistor characteristics of p and n type nanowires and figure 2(b) shows the transfer characteristics of back gated devices. From figure 2(c) we can observe the number of oscillations at 4.2 K in molecular scale diameter. At last figure 2(d) shows the carrier depletion.

C. Germanium Nanowires (GeNWs)

Instead of silicon we use germanium in this mechanism. Germanium nano wires consist of high electrons and holes motilities. This mechanism is analyzed by using the nanoclustor catalyzed VLS mechanism. Now this mechanism is used in CVD process under low temperatures and initial nucleation step at 520 degrees. Compared to the silicon nano wires FETS these germanium nanowires have low contact effects. Depend on the surface doping the complementary p and n type germanium nanowire devices are demonstrated. By suing Zhang et al prototype gate all around devices are also demonstrated. But here the demonstration process is done by the using the atomic layer deposition and magnetron sputtering. Compared to the black gated Ge-NW devices the gate around devices gives the excellent performance.

III. HETEROSTRUCTURE DEVICES

The homogenous narrow wire devices consists two measurements one is low temperature measurements and room temperature measurements. Here to improve the contacts and ohmic behavior we use the particular formation of NiSi/Si contacts. The heavily doped semiconductors contacts consist of narrow channels which are lightly doped. Coming to the hetero structure narrow wire devices are lightly doped transparent ohmic contacts. Compared to the homogenous narrow wire devices this hetero structure devices gives better performance.

A. Heterostructure Nanowire Growth

In this hetero structure nano wire growth consists of bottom up nano wire system. This system controls the growth of hetero structures and coming to the superlattice heterostructure it consists of lithographic process. The below figure (3) shows the growth of nano wires. From this figure (3) we can observe that the vapour decomposes at the surface of nano cluster site. Now in this there will be growth in crystalline semiconductors. If the reactants are changed in this growth then the change will be obtained in axial hetertostructure and radial heterostructure growth.

IV. INTEGARTION TECHNIQUES

To transfer the growth of nano wires we use effective integration techniques. In these integration techniques we use large numbers of nanowires. This nano wires are used in complex integrated circuits. Basically there are two requirements in this integration techniques one is nano wires are assembled into higher integrated circuits which controls the entire operation and second requirement is to access the nano wire devices on to the multiple Length scales and also it gives the interconnection between micro and macro scopic subsystems.

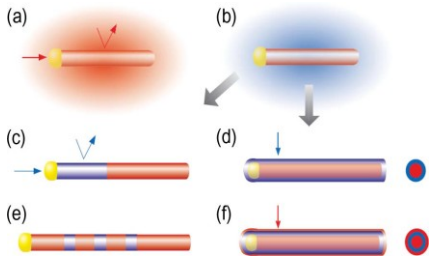

Fig. 3. Nanowire heterostructure growth. (a) Preferential reactant incorporation at the nanocluster catalyst leads to 1-D axial growth. (b) Change in the reactant leads to either (c) axial heterostructure growth or (d) radial heterostructure growth depending on whether the reactant is preferentially incorporated (c) at the catalyst or (d) uniformly on the nanowire surface. Alternating reactants will produce (e) axial superlattices or (f) core-multishell structures.

To obtain parallel operation in nano wire arrays the first requirement is used. During assembly process an external force is employed in this system. Coming to the size of nano wires it is employed by the fluid channel. Here in some of systems we use cross structured nano wires. This cross structured nano wires are used in orthogonal directions. One of the integration techniques is Langmuir–Blodgett (LB) technique. In this technique the compressed layer is transferred into single step crystal substrate. Now this transferred layer is spaced at certain measurement by using micrometer scale. This is about Langmuir Blodgett technique coming to the dry transfer technique, in this nano wire integration is realized at direct growth of selected sites. Here there will be growth in orientation but delay occurs in to the end to end register. The main purpose of integration in nano wires to speed up the process.

V. NANOWIRE CIRCUITS

There are number of ciruits used in nano wires but in this process we use cross bar circuits of nanowires. To overcome the high performance in nano wires we use planar silicon elements. To use this planar silicon elements number of nanoowries should be connected to a single nano wire position. The main advantage of this cross bar circuits is that they play uniqueness role in the opeartion. Large number of devices are connected together to attain effective integration in circuits. During operation it uses and or logic functions. Bascically this one dimensional nanano wire structure is also known as cross bar circuits. In this active devics consists of set of crossed nanowires which offers high density. In this the interconnection is between individual device and functional device. Defect tolerant computing schemes are used in cross bar circuits. The below figure (4) shows the cross bar nanowire structure. By using LB technique crossed narrow wire devices are interconnected to each other. this about the cross bar circuits regarding to nano wires.

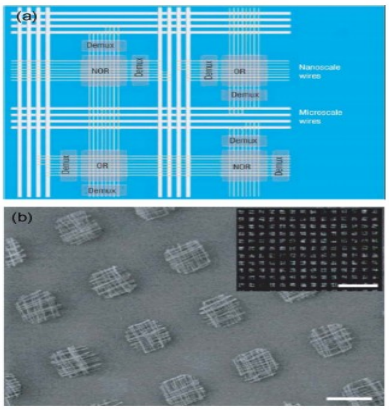

Fig. 4. (a) Crossbar nanowire architecture for computing. (b) SEM image of patterned crossed nanowire arrays produced by LB method; scale bar is 10 µm. Inset shows larger area optical image of the nanowire crossbar array; scale bar is 100 µm.

V. CONCLUSION

First the entire process of nanowires is based on the NWFETs hich enable the perfoemance of the circuit. Some of the key factors are used in narrow wire devices to get limits of performance. Basically semiconductor nanowires are at high yield and consist of electronic properties which are applicable to material compositions. Semiconductor nano wires are most widely used in the integrated systems. Coming to the bottom up nano wire field effect devices, they control the dimensions of performance obtained in the circuit. By using turn down process this can be enable the performance in nano wires. In CMOS technology semiconductor nano wires are most widely used to speed up the operation. Many techniques have been provided to increase the speed and to get maximium performance. At last by using this nano wire technology the devices becomes more flexible.

VI.REFERENCES

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