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New Modular Multi Level Full-Bridge Inverter for Renewable Sources

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Abstract - *In this paper a multi-level inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss harmonic distortion and electromagnetic interference caused by the switching operation of power electronic devices. Here a dual buck configuration with full bridge inverter is used for the MLI implementation. Moreover, its control circuit is more complicated. Thus both the performance and complexity should be considered in designing the multilevel inverter. However interest in the multilevel inverter has been aroused due to its advantages of better power efficiency lower switching harmonics and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. the operation and design of the Boost Converter is described in a very precise manner. Also the simulation of the Boost Converter in MATLAB and the corresponding output waveforms are done.*

Key Words: Multi-level, full-bridge, filter inductor, boost converter, power grid.

1. INTRODUCTION

The conventional single-phase inverter topologies for grid connection include half-bridge and full bridge. The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter.

The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies or the full-bridge inverter are bipolar modulation and unipolar modulation. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced. Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus both the performance and complexity should be considered in designing the multilevel inverter. However interest in the multilevel inverter has been aroused due to its advantages of better power efficiency lower switching harmonics and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters.

Circuit Configuration

The circuit configuration of the multi-level inverter applied to a photovoltaic power generation system is shown in fig 2.1. As can be seen, it is configured by a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches SW1 and SW2. The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the five-level inverter. The dc–dc converter is a boost converter and it performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This five-level inverter is configured by two dc capacitors, a dual buck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The two dc capacitors perform as energy buffers between the dc–dc converter and the five-level inverter. The output of the dual-buck converter is connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the full bridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual-buck converter.

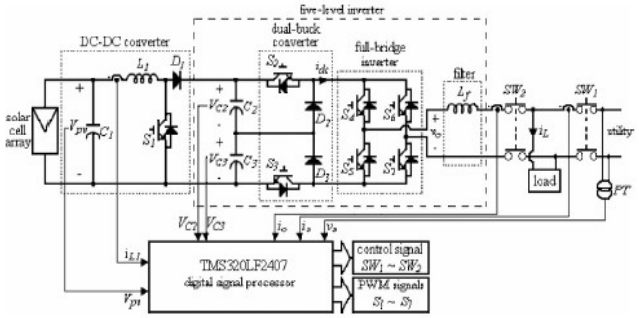

Fig:1 multi-level inverter configuration

The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs) uninterruptible power supplies (UPS), static var compensators, active filters, flexible ac transmission systems (FACTS), and voltage compensators, which are only a few applications. For sinusoidal ac outputs the magnitude frequency and phase should be controllable. According to the type of ac output waveform these topologies can be considered as voltage source inverters (VSIs) where the independently controlled ac output is a voltage waveform.

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The quality of the inverter output waveform can be expressed by using the Fourier analysis data to calculate the total harmonic distortion (THD). The total harmonic distortion is the square root of the sum of the squares of the harmonic voltages divided by the fundamental voltage

$$\text{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+\cdots+V_n^2}}{V_1}$$

2. TYPES OF INVERTERS:

Generally inverters are of two types:
1. VOLTAGE SOURCE INVERTER
2. CURRENT SOURCE INVERTER

TYPES OF VSI:

In these we discuss two main types. They are half bridge and full bridge inverter

HALF-BRIDGE VSI:

The power topology of a half-bridge VSI where two large capacitors are required to provide a neutral point N such that each capacitor maintains a constant voltage=2. Because the current harmonics injected by the operation of the inverter are low-order harmonics a set of large capacitors (C. and Cÿ) is required. It is clear that both switches S. and Sÿ cannot be on simultaneously because short circuit across the dc link voltage source vi would be produced. There are two defined (states 1 and 2) and one undefined (state 3) switch state as shown in Table 2.1. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.

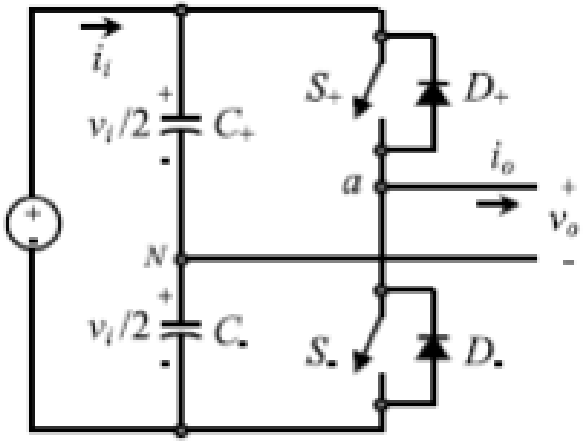

Fig 2: single phase half bridge VSI

Selective Harmonic Elimination:

The main objective is to obtain a sinusoidal ac output voltage waveform where the fundamental component can be adjusted arbitrarily within a range and the intrinsic harmonics selectively eliminated. This is achieved by mathematically generating the exact instant of the turn-on and turn-off of the power valves.

$$\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)=(2+\pi\hat{v}/v_i)/4$$
$$\cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3)=1/2$$
$$\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)=1/2$$

Inverters convert low frequency main AC power to a higher frequency for use in induction heating. To do this AC power is first rectified to provide DC power. The inverter then changes the DC power to high frequency AC power.

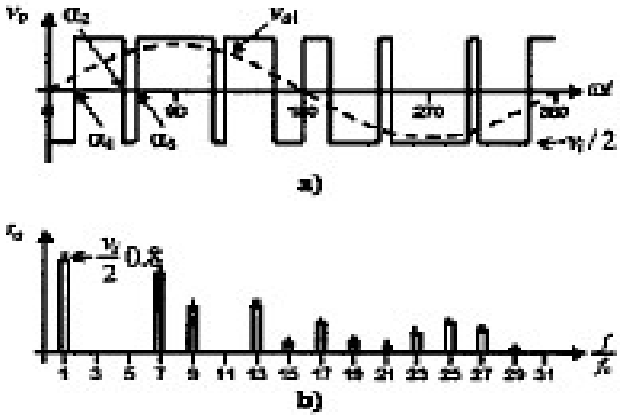

Fig 3: waveforms showing operation of selective harmonic elimination technique

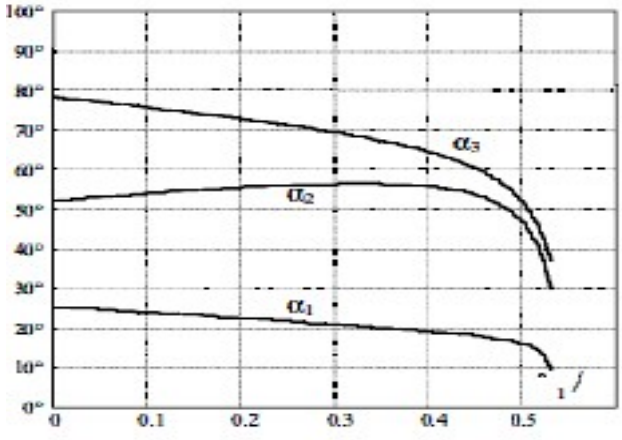

Fig 4: graphical representation of angles

Fundamental magnitude control (N ÿ 1. 3) the equations to be solved are

$$\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)-\cos(1\alpha_4)=(2+\pi\hat{v}/v_i)/4$$
$$\cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3)-\cos(3\alpha_4)=1/2$$
$$\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)=1/2$$
$$\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)=1/2$$

The power topology of a full - bridge VSI. This inverter is similar to the half-bridge inverter however a second leg provides the neutral point to the load. As expected both switches S1. And S1ÿ (or S2. and S2ÿ) cannot be on simultaneously because a short circuit across the dc link voltage source Vi would be produced.

The undefined condition should be avoided so as to be always capable of defining the ac output voltage. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition the modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant. It can be observed that the ac output voltage can take values up to the dc link value vi which is twice that obtained with half-bridge VSI topologies.

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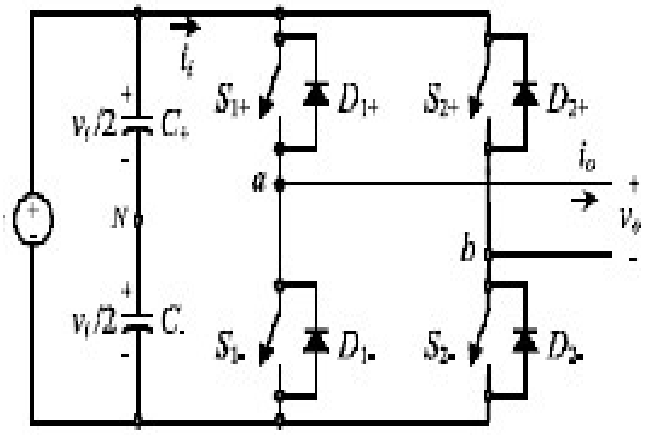

Fig 5: full bridge inverter

3. MULTILEVEL CONVERTER:

The conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types

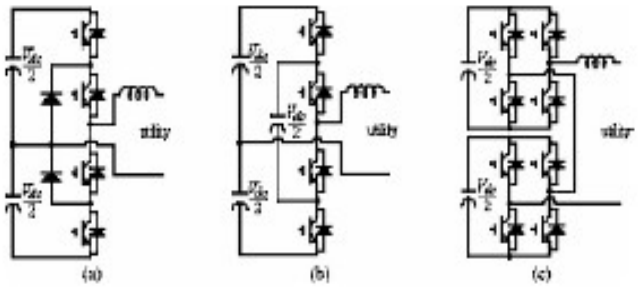

Fig 6: Circuit configuration of conventional single - phase multilevel inverter. (a) Diode clamped. (b) Flying capacitor. (c) Cascade H- Bridge

Diode-Clamped Multilevel Converter:

Figure 6(a) shows the basic configuration of a diode-clamped multilevel inverter. As can be seen it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The voltage difference of each level is *V*dc/2 (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter the voltages of these two dc capacitors must be controlled to be equal. The control for balancing these two dc capacitors is very important in controlling the diode-clamped multilevel inverter and it is very hard under the light load. If the five-level output voltage is expected extra two diodes and four power electronic switches are required.

Flying Capacitor Multilevel Converter

Figure 6(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be

Cascade H- Bridge Multilevel Converter

Figure 6(c) shows the circuit configuration of the basic cascade H-bridge multilevel inverter. As can be seen it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is $\frac{V_{dc}}{2}$, and the output voltage of each full-bridge inverter can be controlled to be $\frac{V_{dc}}{2}$, 0 and

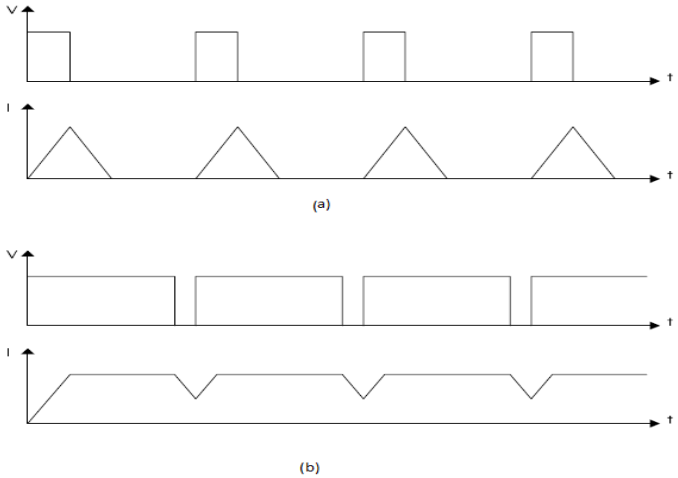

Fig 7: (a) low frequency PWM if (a) D < rise time (b) D > rise time

At high frequencies V turns on and off very quickly, regardless of D such that the current does not have time to decrease very far before the voltage is turned back on. The resulting current through the solenoid is therefore considered to be constant. By adjusting the D the amount of output current can be controlled. With a small D the current will not have much time to rise before the high frequency PWM voltage takes effect and the current stays constant. With a large D the current will be able to rise higher before it becomes constant.

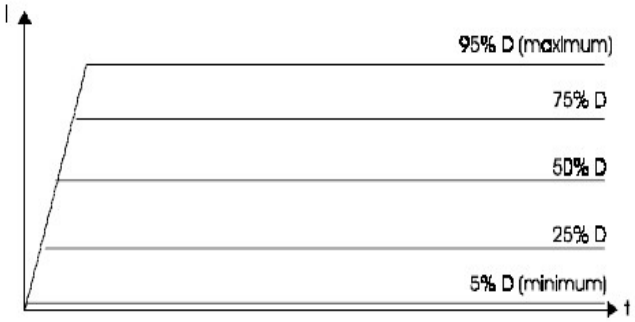

Fig 8: output current by adjusting D

n is any integer (1,2,3,..) and p is the number of pulses in the circuit and the magnitude decreases as the ration of 1/h (1/3, 1/5, 1/7, 1/9,...). Table 4 shows examples of such.

RATIO Iscc / I load	Harmonic Range	Limit as % of Fundamental
Less than 20	Odd numbers less than 11	4.0 %
Between 20 and 50	Odd numbers less than 11	7.0 %
Greater than 1000	Odd numbers greater than 35	1.4%

Table 1: Current Harmonic Limits as per IEEE 519-1992

For voltage harmonics the voltage level of the system is used to determine the limits. At the higher voltages more customers will be effective hence the lower limits.The European Community has also developed susceptibility and emission limits for

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harmonics. Formerly known as the 555-2 standard for appliances of less than 16 A a more encompassing set of standards under IEC 1000-4-7 are now in effect.

Bus Voltage	Voltage Harmonic Limit as % of Fundamental
69Kv and below	Individual harmonic = 3.0%
69Kv and below	THD= 5.0%
161kv and above	Individual harmonic = 1.0%
161kv and above	THD = 1.0%

Table 2: Voltage Harmonic Limits as per IEEE 519-1992

Fig 9: harmonics across waveform

Despite the use of good quality test meter instrumentation high current flow can often remain undetected or under estimated by as much 40%. This severe underestimation causes overly high running temperatures of equipment and nuisance tripping. This is simply because the average reading test meters commonly used by maintenance technicians are not designed to accurately measure distorted currents and can only provide indication of the condition of the supply at the time of checking. Power quality conditions change continuously and only instruments offering true RMS measurement of distorted waveforms and neutral currents can provide the correct measurements to accurately determine the ratings of cables bus bars and circuit breakers.
There is much discussion over the practical harmonic range of a measurement instrument however study of the harmonic profiles of typically installed equipment can guide the system designer to the practical solution. A typical harmonic profile graph will show a logarithmic decay as the harmonic frequency increases. It is necessary to establish the upper level at which the harmonic content is negligible.

4. PULSE WIDTH MODULATION (PWM):

Pulse Width Modulation (PWM) is the most effective means to achieve constant voltage battery charging by switching the solar system controller's power devices. When in PWM regulation the current from the solar array tapers according to the battery's condition and recharging needs consider a waveform such as this: it is a voltage switching between 0v and 12v. It is fairly obvious that, since the voltage is at 12v for exactly as long as it is at 0v then a 'suitable device' connected to its output will see the average voltage and think it is being fed 6v - exactly half of 12v. So by varying the width of the positive pulse - we can vary the 'average' voltage.

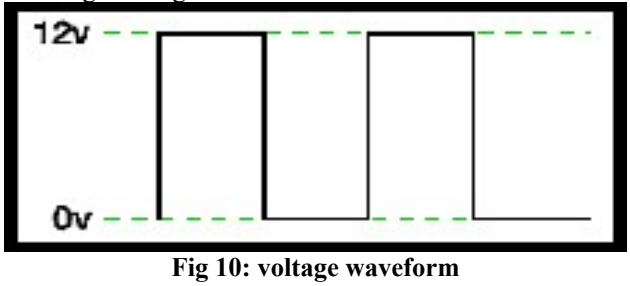

Fig 10: voltage waveform

Similarly if the switches keep the voltage at 12 for 3 times as long as at 0v the average will be 3/4 of 12v - or 9v as shown below and if the output pulse of 12v lasts only 25% of the overall time then the average is

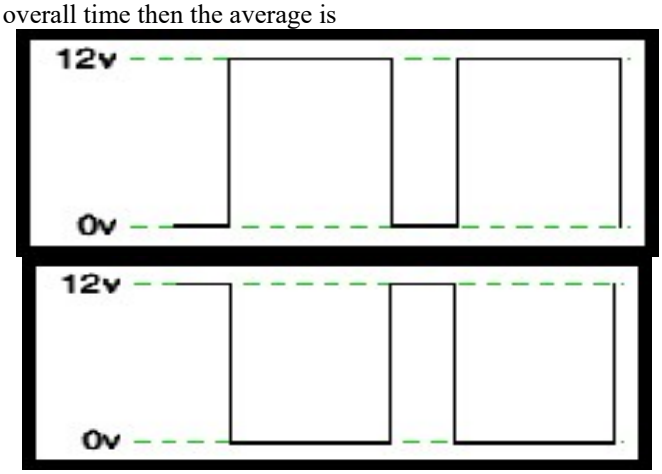

Fig 11: variation in voltage

By varying - or 'modulating' - the time that the output is at 12v (i.e. the width of the positive pulse) we can alter the average voltage. So we are doing 'pulse width modulation'. I said earlier that the output had to feed 'a suitable device'. A radio would not work from this: the radio would see 12v then 0v and would probably not work properly. However a device such as a motor will respond to the average so PWM is a natural for motor control.

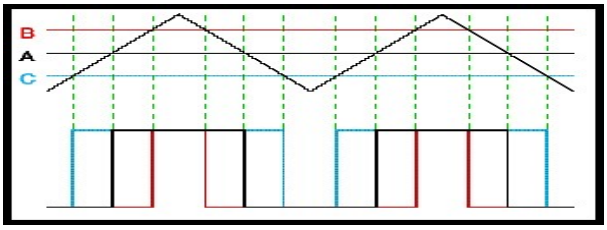

Fig 12: generation of PWM waveform

When the demand speed it in the middle (A) you get a 50:50 output as in black. Half the time the output is high and half the time it is low. Fortunately there is an IC (Integrated circuit) called a comparator: these come usually 4 sections in a single package. One can be used as the oscillator to produce the triangular waveform and another to do the comparing so a complete oscillator and modulator can be done with half an IC and maybe 7 other bits.

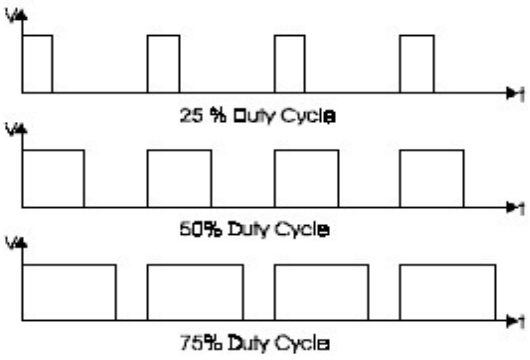

Fig 13: PWM signal with different duty cycle

A solenoid is a length of wire wound in a coil. Because of this configuration, the solenoid has in addition to its resistance R a certain inductance L. When a voltage V is applied across an inductive element the current I produced in that element does not

jump up to its constant value but gradually rises to its maximum over a period of time called the rise time. Conversely it does not disappear instantaneously even if V is removed abruptly but decreases back to zero in the same amount of time as the rise time.

The switching operations of the replaced power electronic switches are complementary to those of power electronic switches *S*2 and *S*4 respectively. Accordingly the five-level inverter can supply active power and reactive power simultaneously

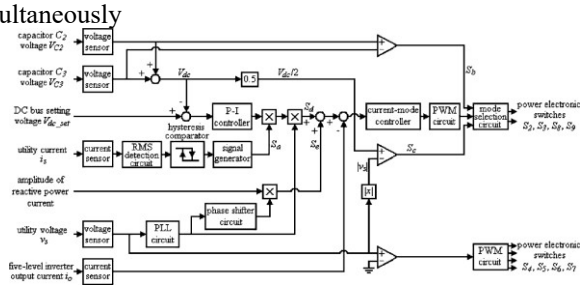

Fig 14: Control block diagram of five-level inverter with the function of supplying reactive power.

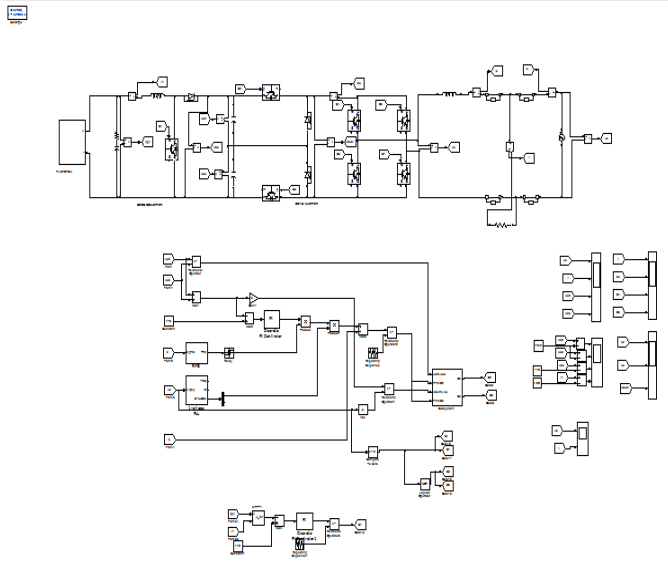

Fig 15: Indicates the Existing Simulation Model / Simulink of Five Level Inverter

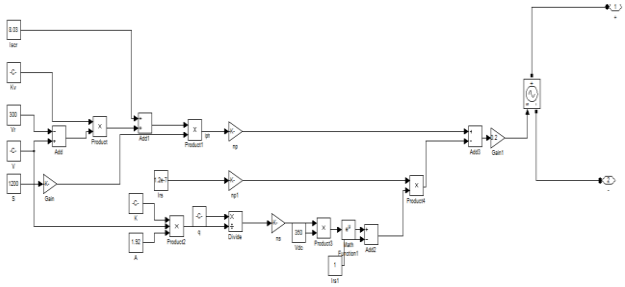

Fig 16: Indicates the Simulation Model / Simulink of a DC PV Panel

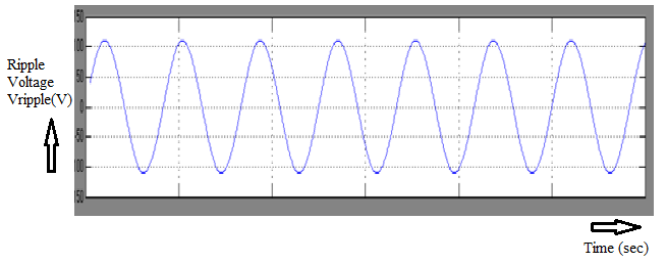

Fig 17:Indicates the Output Ripple of DC Capacitor C2 (Vc2)

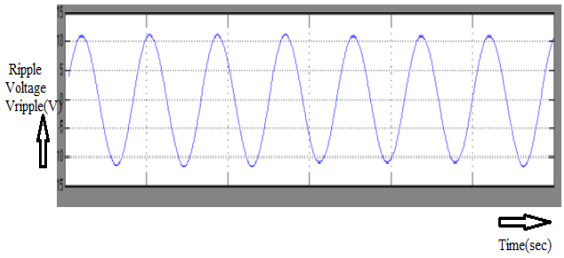

Fig 18: Indicates the Output Ripple of DC Capacitor C3(Vc3)

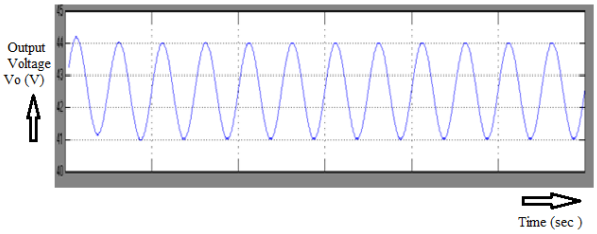

Fig 19:Indicates the Output Voltage of Solar Array

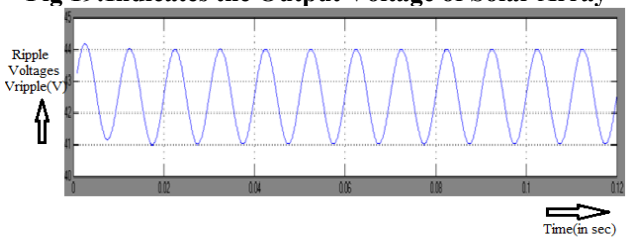

Fig 20: indicates the inductor current of DC DC Converter

5. CONCLUSION

A photovoltaic power generation system with a multi-level inverter is developed. The multi-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation.

The Simulation results verify that the developed photovoltaic power generation system and the multi-level inverter achieve the expected performance.

In contrast if D is larger than the rise time I will never fall back to zero so it will be continuous and have a DC average value. The current will not be constant however but will have a ripple.

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