High performance and high efficiency DET flip flop by using Clock gating techniques

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Abstract:

Dual edge triggered (DET) flip-flops achieve the same data rate as single edge triggered (SET) flip-flops at half the clock frequency, which can lead to reduced power dissipation of synchronous logic circuits. The cost of this reduction is higher circuit complexity of DET flip-flops which usually have more transistors and more internal nodes than SET flip-flops. In this paper, a novel Clock gating flip-flop (FF) design for high speed applications is presented. . Both total transistor count and the number of clocked transistors are significantly reduced to improve power consumption and speed in the flip-flop.

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Introduction:

Today's technologies make possible powerful computing devices with multi-media capabilities. Consumer's attitudes are gearing towards better accessibility and mobility. Their desire has caused a demand for an ever-increasing number of portable applications requiring low-power and high throughput. For example, notebook and handheld computers are now made with competitive computational capabilities as those found in desktop machines. Equally demanding are personal communication applications in a pocket-sized device. In these applications, not only voice, but data as well as video are transmitted via wireless links. It is important that these high computational capabilities are placed in a low-power, portable environment. The weight and size of these portable devices is determined by the amount of power required. The battery lifetime for such products is crucial; hence, a well planned low-energy design strategy must be in place .As the density of the integrated circuits and size of the chips and systems continue to grow, it becomes more and more difficult to provide adequate cooling for the systems .In addition to heat removal, there are also economic and environmental issues for low power development. In the United States, computer equipment accounts for about 2-3% 1 Introduction 2 of national electricity consumption. This figure is expected to increase as there is tremendous increase in household computer applications, Web phones, handheld computers, and internal terminals. These economic and environmental reasons have compelled the requirement for energy efficient computers. The 20th century has brought an extension to existing 2- valued logic called as n-valued logic (>2). Those logical calculi having more than two truth values are Multi valued logics some of which are the 3-valued logic, the finite valued with more than 3 values and the infinite valued like fuzzy logic . This paper emphasizes on the three-valued logic, which has three valued switching (i.e. true, false and intermediate). It is logically stated as base-3 counting system and is referred as ternary logic in this paper. In 1964, it was proven that for implementation of switching circuits, natural base (e = 2.71828) is the most efficient radix. Ternary system evolved because of the several advantages over binary such as information

content transmitted over a given set of lines is increased, memory requirement for a given length of data is lowered, interconnections required to implement logic functions are reduced thereby reduction in chip area thus making VLSI implementations energy efficient and cost effective at the same time. Also, certain serial and serial-parallel operations are carried out at faster speeds. Numerous applications like digital signal processing, fuzzy logic, artificial intelligence, memories, communications, robotics, digital control systems and many more, have confirmed its applications. The design of multipliers in today's advanced technology takes up any one or combination of the following design targets such as high speed, regularity of layout and hence less area in one multiplier, low power consumption thus making them adequate for a number of high speed, lower power and compact VLSI implementations. Three valued logic (3VL) based multiplier design offers the added advantage of circuit complexity being reduced in terms of both device count and inter connections. It is a very slow operation which also depends on the word size to be executed where large number of partial products (PPs) needs to be computed to produce the final result. So they should be fast enough to give the output in the required cycle time. Recently, because of the rapid growth of battery-powered, high-performance and portable electronic devices, the power consumption of VLSI chip has gained extraordinary consideration. It is known that the power consumption determines the device's battery life as well as the time between two successive recharges of a device so what assumes importance is the reduction of power dissipation in such devices. Various techniques for reducing the power consumption are applied externally or internally in digital multipliers. Techniques which deal with the input data characteristics are external techniques, whereas those concerned with the logic, architecture and circuit designs of the multiplier are internal ones.

C-ELEMENT:

A C-element, introduced in, is normally a three-terminal device with two inputs and one output. When all of its inputs are the same, the output switches to the value of the inputs. When the inputs are not the same, the previous output value is preserved. This device acts as a latch which can be set and reset with appropriate combinations of signal levels at the input.
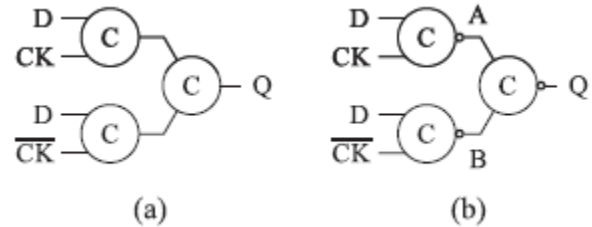

FIG: 1(a) non inverting (b) inverting using C-ELEMENTS.

DUAL EDGE TRIGGERED FLIP-FLOP:

In a synchronous system, operations and data sequences take place with a fixed and predetermined time relationship. The timing of computations is controlled by flip-flops and latches together with a global clock. Flip-flops and latches are clocked storage elements, which store values applied to their inputs. They are classed according to their behavior during the clock phases. A latch is level sensitive. It is transparent and propagates its input to the output during one clock phase (clock low or high), while holding its value during the other clock phase. A flip-flop is edge triggered. It captures its input and propagates it to the output at a clock edge (rising or falling), while keeps the output constant at any other time. The design of this clocked storage an element is highly depended on the clocking strategy and circuit topology .This research focuses on synchronous system with edge-triggered clocking strategy, henceforth, only flip-flop is discussed. In particular, dual edge-triggered flip-flops are introduced and explored.
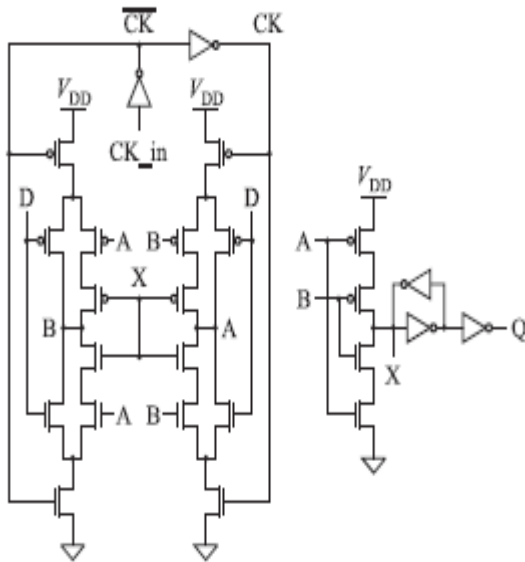
A. Floating-Node FN_C Flip-Flop:

Fig.2 floating-node FN_C

In the IP_C flip-flop, signal levels at A and B toggle after every clock transition regardless of D and Q, which leads to higher power dissipation due to clock signal transitions. The transistor-level and gate-level schematic diagrams of the improved FN_C flip-flop that solves this issue. In the case of the LG_C, IP_C, and FN_C flip-flops, for the output C-element to work correctly, the requirements for the flip-flop's input stage are as follows: In between the clock edges, at least one of A and B has to be kept at Q to avoid flipping at the output, and once the clock toggles, both nodes have to be at D for the output to switch to D. As long as one of A and B is kept at Q, the signal level at the other node is irrelevant for the correct operation of the output stage. With implementations of C-elements, one of A and B that is not kept at Q can be at any permitted voltage level without affecting the output. The LG_C flip-flop satisfies these requirements by employing two independent latches at A and B, one of which is always redundant (which one depends on D and CK). The implicit-pulsed IP_C flip-flop ensures

correct operation through the cross-connection of the weak inner this article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination. Simulated signal levels of the FN_C flip-flop implemented in the GF28HPP technology. The figure illustrates the behavior of the FN_C flip-flop. C-elements. This cross-coupling ensures that nodes A and Bare at opposite signal levels and that one of them is at Q. The improved floating-node FN_C flip-flop design does not cater for the node not at Q in between clock transitions and does not reinforce its signal level. This behavior is implemented through the feedback of X, which Q follows, into the inner cross-coupled weak C-elements. If the signal combination of D and CK is such that the Q level at one of A or B is maintained by strong transistors of an inputC-element, the other node is left floating. This does not compromise the overall static behavior of the circuit, since as it was mentioned above, the signal level at the floating node cannot affect the output as long as the other node is at Q. Compared to the IP_C flip-flop, this flip-flop's power dissipation due to clock signal transitions is reduced without increasing power dissipation due to input switching. The FN_C's simulated signal levels for one clock transition. The flip-flop was designed in the 28 nm GF28HPP CMOS technology. Initially in the simulation, Q is "0,"CK is "1," and D is "0." Since D is equal to CK, B is kept at"1" with strong transistors of its input C-element, which ensures that X (and Q that follows X) stays at "0." As a result, node A is floating. Due to the switching of parasitic capacitances, the voltage level at node A is slightly higher than the VDD voltage of 0.85 V. Before the next clock edge, input D switches to "1."Since D is now equal to CK, A switches to "0." Now CK, A, and X are "0," which keeps node B at "1" through the weak transistor branch connected to its input C-element. The next clock edge comes when CK switches to "0" and CK switches to"1." Since CK is now equal to D,

node B switches to "0." Both A and B are now at "0," which causes the output C-element to switch Q to "1." Node A is floating again and B is kept at "0," which ensures that Q stays at "1" in the new cycle. In this example, the combinations of D and CK are such that only node A is seen floating. If either D or CK were inverted, node B would have been the floating node. Because of the switching of parasitic capacitances before floating node events, floating voltage levels at A and B can stay above the VDD voltage of 0.85 V or below 0 V. Analog simulations indicate that the increase above VDD and the decrease. Transistor-level schematic diagram of the conditional-toggle CT_CDET flip-flop. Simulated signal levels of the CT_C flip-flop implemented in the 28nm GF 28HPP technology. below 0 V do not exceed 10% of the nominal VDD and that no significant dynamic current is flowing through the transistors' channels during this time. Thus, floating node events do not affect circuit reliability.
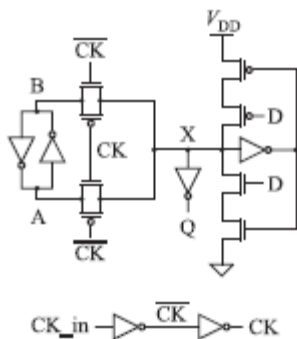
D. Conditional-Toggle CT_C and CTF_C Flip-Flops:

Fig 3.Schematic diagram of the conditional-toggle CT_CDET flip-flop.

The novel conditional-toggle CT_C DET flip-flop design. The CT_C flip-flop circuit uses only20 transistors including transistors for the input, output, and clock buffering. The flip-flop consists of a dynamic C-element at the output

and a latch that provides static behavior to the circuit. The distinguishing feature of the CT_C flip-flop is that the state of its latch does not change when the flip-flop's output switches after a clock transition, which leads to low switching energy dissipation. The circuit for the output C-element is based on the weak-feedback implementation but with the feedback inverter eliminated. The inputs to it are input D and the signal that mirrors Q in between clock transitions. When D is equal to Q, the C-element keeps its inverted output X at the level of Q. When D is not equal to Q, the Q level at X is kept by the latch. The latch part of the circuit is responsible for toggling the signal level at X after clock transitions and for keeping it at Q in between clock transitions when D is not equal to Q. The latch part consists of two inverters connected back to-back and a bidirectional 2-to-1 multiplexer with its output connected to node X. The operation of the CT_C flip-flop is illustrated using simulated voltage traces. The clock signal makes the multiplexer alternate between the two ends of the latch A and B after every clock transition. In between clock transitions, the end of the latch that is connected to X is at Q. After a clock transition, the multiplexer switches to the opposite end of the latch, which makes the signal levels at X and Q toggles if D was not equal to Q before the clock edge. If D is equal to Q when the clock edge arrives, it is the latch that toggles its stored value and not node X, because the C-element forces node X to the level of D. Toggling at the output is not done by changing the value stored by the latch but rather by multiplexing to the inverse of it, which achieves low switching activity within the flip-flop. The latch toggles its stored value after a clock edge only when D is equal to Q. Implementation of the CT_C flip-flop presents trade-offs between power dissipation at high and low switching activities and circuit delay. Strong inverters in the latch make the output switching faster with little impact on the switching energy. However, the stronger these inverters are, the

more energy It takes to change the state of the latch, i.e., the higher the power dissipation at low switching activity becomes. Fig. 15 shows the CTF_C flip-flop, a modification of the CT_C flip-flop, that relaxes these trade-offs.

During operation one of A or B nodes is at D while the other is at D. In the CTF_C flip-flop, the strengths of signal levels at these nodes depend not only on transistor sizing but also on D:Which ever node is at D is kept strongly while the other node is kept weakly with always-on transistors. If at a clock transition D is not equal to Q, node X is multiplexed to a strong D that quickly changes X to D and Q to D. When D is equal to Q, logic level at node X is kept strongly at D by the C-element. The next clock transition multiplexes node X to a weak D which the C-element overpowers quickly and at a low energy cost. Thus, CTF_C achieves faster switching compared to CT_C and reduces energy dissipation of idle cycles.
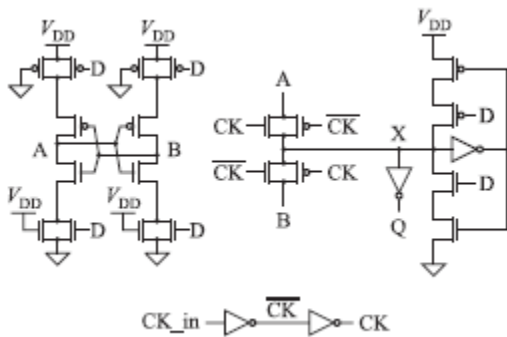

Fig.4 Schematic diagram of the improved conditional-toggle CTF_C DET flip-flop.

A. Clock Gating Technique:

Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal regardless of whether or not they will toggle in the next cycle. Clock enabling signals are usually introduced by designers during the system and clock design phases, where the inter-dependencies of the various functions are well understood. In contrast, it is very difficult to define such signals in the gate level, especially in control logic, since the inter-dependencies among the states of various flip-flops depend on automatically synthesized logic. There is a big gap between block disabling that is driven from the HDL definitions, and what can be achieved with data knowledge regarding the flip-flops activities and how they are correlated with each other. The clock gating technique has been developed to avoid unnecessary power consumptions, like the power wasted by timing components during the time when the system is idle. Specifically for flip-flops, clock gating means disabling the clock signal when the input data does not alter the stored data. It can be applied from the system level where the entire functional unit can be selectively set into sleep mode, or from the sequential/combinational circuit level where some parts of the circuit are in sleep mode while the rest of the block are operating. But Clock gating does not come for free. Extra logic and interconnects are required to generate the clock enabling signals, and the resulting area and power overhead must be considered [5]. In the extreme case, each clock input of a flip-flop can be disabled individually, yielding maximum clock separation. This, however, results in high overhead. Thus, the clock disabling circuit is shared by a group of several flip-flops in an attempt to reduce the overhead.

B. How to implement Clock Gating?

When there is no activity at a register "data" input, there is no need to clock the register and hence the "clock" can be gated to switch it off [5]. If the clock feeds a bank of registers, an "enable" signal can be used to gate the clock, which is called the "clock gating enable".
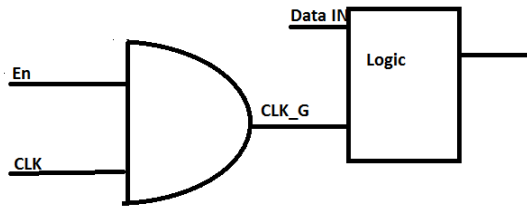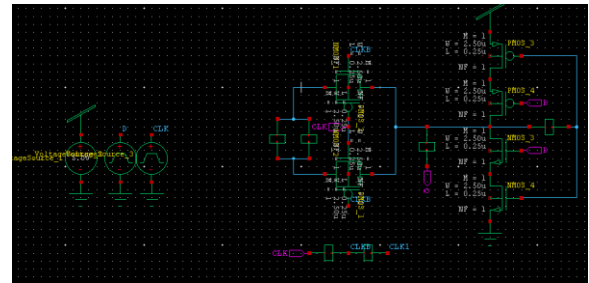
Fig: 5 Clock gating circuit
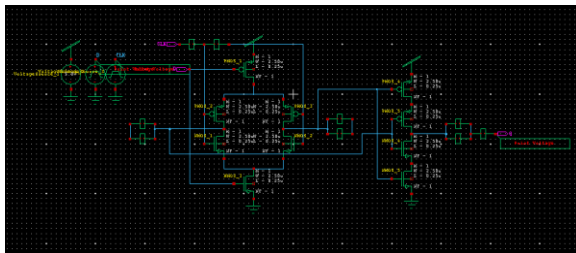

Fig9 :CTC_DET FF

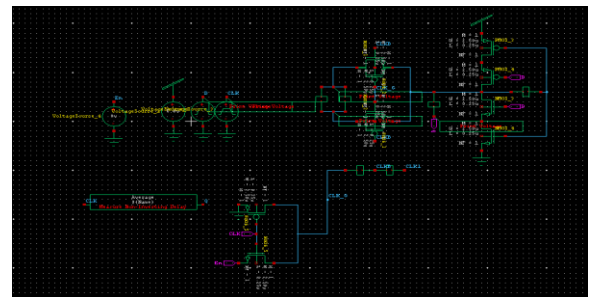## Result analysis:

Fig:6 LG_DET FF

Fig:10 Clock gating technique based DET flipflop
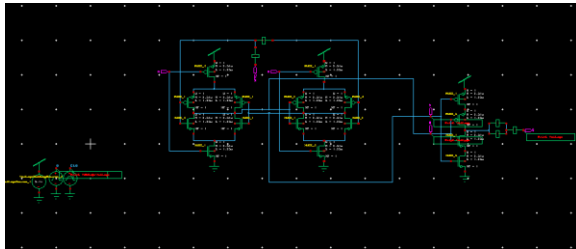
Fig:7 IP_DET FF
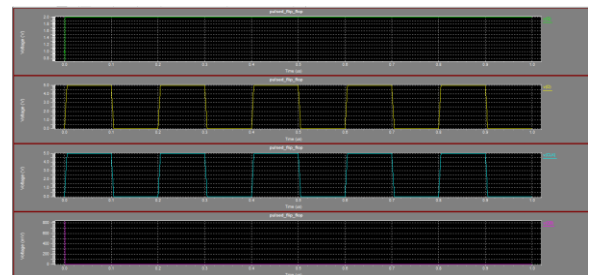
Fig:11 Waveform for flipflop
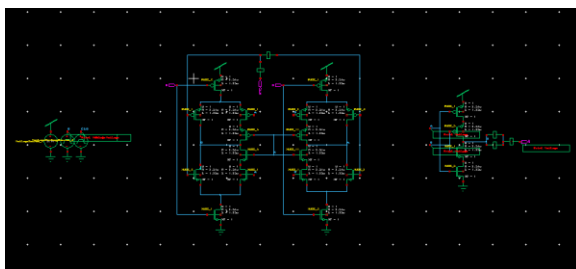
Tabulation:

Fig:8 FN_DET FF

Type	Power consumption	Delay
LG_DET	4.547539e-003 watts	1.0000e-007
Implicit pulsed	2.399687e-004 watts	5.2500e-008
FN DET	2.473412e-004 watts	5.2500e-008
CTC_DET	6.207332e-005 watts	9.9754e-008

Clock gating technique	2.449398e-006 watts	5.2500e-008

Conclusion:

In this paper, a novel low-power pulse triggered flip-flop (ff) design is presented. If optimization is applied it is possible to achieve much higher speeds .it is then concluded that the proposed novel implicit pulsed-data close to output appears to be the most suitable storage element in high-speed, low-power VLSI applications. The pulse trigged, consume less power and delay compare with existing.

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