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Fault Tolerant Parallel Filters Based on ErrorCorrection Code

Y Latha
(Assistant Professor)
Stanley College of Engineering and Technology for Women
ylatha@stanley.edu.in

Abstract:*In today's world, there is a great need for the design of low power and area efficient high-performance DSP system. FIR filter is considered to be the fundamental device in the broad application of wireless as well as the video and image processing system. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC This new scheme allows more efficient protection when the number of parallel filters is large. Finally, both the effectiveness in protecting against errors and the cost are evaluated for an FPGA implementation.*

IINTRODUCTION

Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Today filters are widely used in number of applications which based on automotive, medical, and space where reliability of components in digital electronic circuits is critical. Filters of some sort are essential in the operation of most electronic circuits.

Error Detection and Correction

In information theory and coding theory with applications in computer science and telecommunication, error detection and correction or error control are techniques that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data in many cases.

1) Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver.

2) Error correction is the detection of errors and reconstruction of the original, error-free data.

Filtering is also a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. It is therefore in the interest of anyone involved in electronic circuit design to have the ability to develop filter circuits capable of meeting a given set of specifications. In signal processing, a digital filter is a device or process that removes some unwanted component or feature from a signal.

II EXISTING SYSTEM

In existing concurrent error detection and correction technique to detect and correct single errors occurring in pairs of parallel filters that have either the same input data or the same impulse response. The technique uses a primary implementation comprised of two independent filters and a redundant implementation that shares input data between both filters so as to detect and correct errors. The area cost of the proposed scheme is shown to be slightly more than double that of the unprotected filter, whereas the conventional triple modular redundancy solution requires an area three times that of the

unprotected filter. However, it is increasingly common to find systems in which several filters operate in parallel.

This is the case in filter banks and in many modern communication systems. For those systems, the protection of the filters can be addressed at a higher level by considering the parallel filters as the block to be protected. This idea was where two parallel filters with the same response thatprocessed different input signals were considered. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was obtained.

In fault tolerance based system based on Error Correction Codes (ECCs) using VHDL is designed, implemented, and tested.

It proposes that with the help of ECCs i.e. Error Correction Codes there will be more protected Parallel filter circuit has been possible. The filter they have used for error detection and correction are mainly finite-impulse response (FIR) filters. They have been used Hamming Codes for fault correction in which they takes a block of k bits and produces a block of n bits by adding n−k parity check bits. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. In this scheme, they have used redundant module in which the data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by re-computing the parity check bits and comparing the results with the values stored. In this way using hamming codes error can be detected and corrected within the circuit.

III PROPOSED SYSTEM

A simple ECC takes a block of k bits and produces a block of n bits by adding n−k parity check bits. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. As an example, let us consider a simple Hamming code [14] with k = 4 and n = 7. In this case, the three parity check bits p1, p2, p3 are computed as a function of the data bits d1, d2, d3, d4 as follows:

$$p1 = d1 \oplus d2 \oplus d3$$

$$p2 = d1 \oplus d2 \oplus d4$$

$$p3 = d1 \oplus d3 \oplus d4.$$

In the Parity, the error is detected and corrected by using,

$$yc1\,[n] = z1\,[n] - y2\,[n] - y3\,[n]$$

The data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by re-computing the parity check bits and comparing the results with the values stored. In the example considered, an error on d1 will cause errors on the three parity checks; an error on d2 only in p1 and p2; an error on d3 in p1 and p3; and finally an error on d4 in p2 and p3. Therefore, the data bit in error can be located and the error can be corrected.

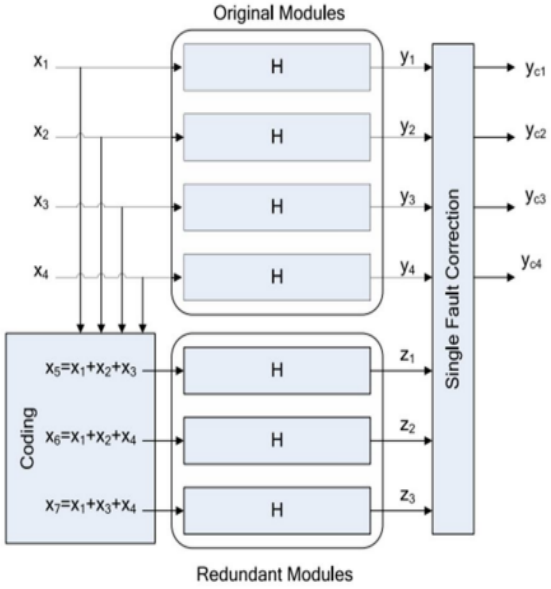

Fig.1 block diagram of proposed work

This is done by recomputing the parity check bits and comparing the results with the values stored. In the example considered, an error on d1 will cause errors on the three parity checks; an error on d2 only in p1 and p2; an error on d3 in p1 and p3; and finally, an error on d4 in p2 and p3. Therefore, the data bit in error can be located and the error can be corrected. This is commonly formulated in

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terms of the generating G and parity check H matrixes. For the Hamming code considered

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}.$$

TABLE I
ERROR LOCATION IN THE HAMMING CODE

$s_1 s_2 s_3$	Error Bit Position	Action
0 0 0	No error	None
1 1 1	d_1	correct d_1
1 1 0	d_2	correct d_2
1 0 1	d_3	correct d_3
0 1 1	d_4	correct d_4
1 0 0	p_1	correct p_1
0 1 0	p_2	correct p_2
0 0 1	p_3	correct p_3

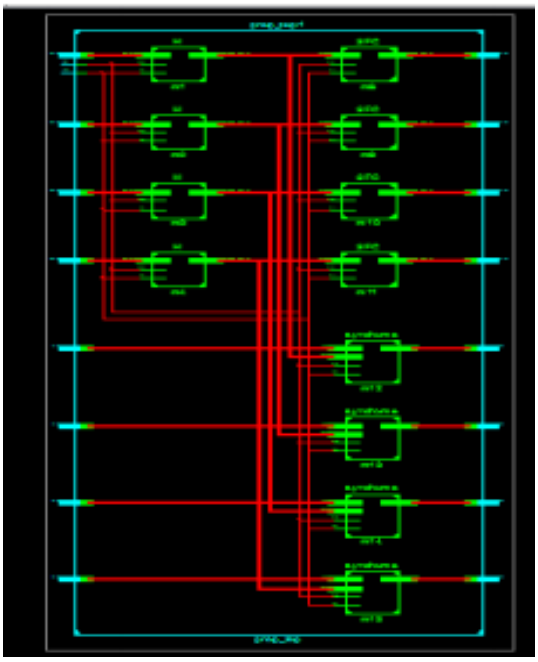
In our case, we can define the check matrix and calculate

s = y HT

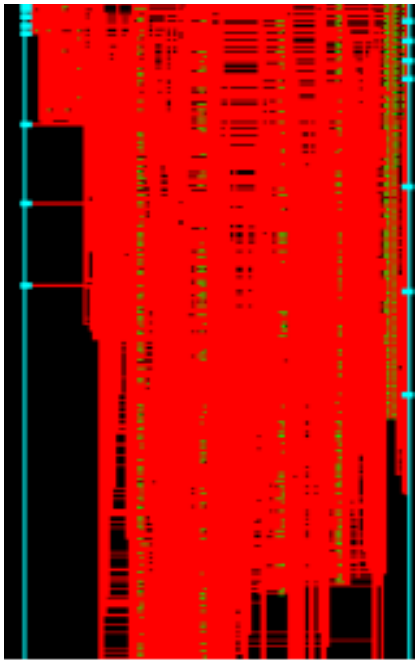
to detect errors. Then, the vector s is also used to identify the filter in error. In our case, a nonzero value in vector s is equivalent to 1 in the traditional Hamming code. A zero value in the check corresponds to a 0 in the traditional Hamming code. It is important to note that due to different finite precision effects in the original and check filter implementations, the comparisons in can show small differences. Those differences will depend on the quantization effects in the filter implementations that have been widely studied for different filter structures. The interested reader is referred to for further details. Therefore, a threshold must be used in the comparisons so that values smaller than the threshold are classified as 0.

IV RESULTS

RTL schematic



Technology schematic:



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Timing report:

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Timing Summary:
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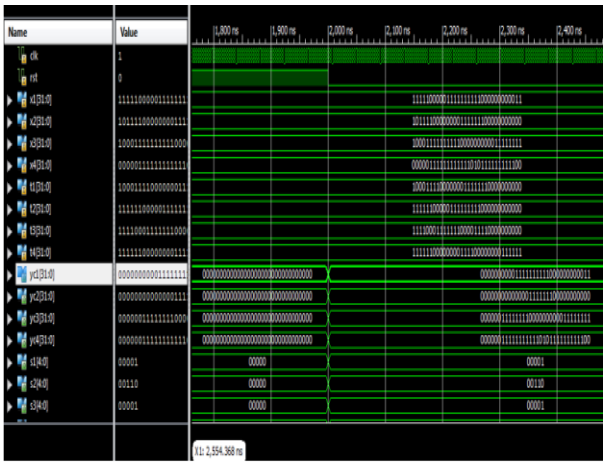
Speed Grade: -5

   Minimum period: 6.972ns (Maximum Frequency: 143.440MHz)
   Minimum input arrival time before clock: 7.022ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found
```

Simulation results



V CONCLUSION

In this project, we have presented a scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The proposed scheme can also be applied to the FIR filters. The technique is evaluated using a only two redundant filter to achieve the high error correction in ECC which also reduces the area, delay and power than previous. This will be of interest when the number of parallel filters is small as the cost of the proposed scheme is larger in that case.

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