

Design Of Islanding Detection Using Phase-Locked Loops In Three-Phasegrid-Interface Power

K Gopi

ABSTRACT:Phase locked loop and synchronization techniques are one of the most important issues for operating grid-interfaced converters in practical applications, which involve Distributed Power Generation Systems, Flexible AC Transmission Systems (FACTS), and High Voltage Direct Current (HVDC) Transmission, and so on. This paper proposes a systematic PLL modeling and design approach to evaluate different frequency-based islanding detection methods. Two different types of PLL-based islanding detection solution are discussed, accounting for a majority of the existing methods. The first method is to modify the PLL to constantly move the stable equilibrium point. The second method is to modify the PLL small-signal characteristics to achieve a monotonic instability behavior under the islanded conditions. The design procedures of these methods are presented using the proposed PLL modeling approach.

KEYWORDS-Converter stability, distributed generation (DG), islanding detection, phase-locked loop (PLL).

I. INTRODUCTION

Distributed generation for renewable energy sources is penetrating the electric power system due to the rising cost of traditional energy sources and the environmentally friendly features of renewable energy. Over 60 countries around the world have set targets for renewable energy supply [1]. The types of renewable energy include solar, wind, hydrogen, biomass, geothermal, hydropower, and biodiesel. Many of these renewable energy sources are designed to supply energy into the electric power system. Each power electronics interface should provide quality power to the electric grid for the loads. This means the harmonics should be low, the inverter should be turned off if the voltage or frequency goes out of range, and the inverter should be able to detect when the centralized generator is no longer connected; this case is called unintentional islanding. An island may occur for many reasons;

such as, a disconnection for servicing, human error, an act of nature, or one of the circuit breakers in the power system trips as shown in Fig. 4 with distributed generation (DG). Under the island condition, the distributed resource (DR) is required to disconnect within 2 seconds according to IEEE 1547[2]-[3]. A distributed resource should disconnect from the electric grid for many reasons: to prevent the electric power grid from reconnecting with the distributed resource out of phase causing a large spike in voltage damaging the loads, a line worker could get hurt, and the utility is liable for power lines even when distributed resources use them to transmit power.

Besides the detection of abnormal grid conditions, the standard also requires that a DG unit has to detect the unintentional islanding condition and de-energize the area electric power system (EPS) within 2 s. When this condition occurs, the system voltage and frequency normally shift out of the normal range and an over or under voltage (OUV) or frequency (OUF) protection method can be directly used to detect the islanding event. However, the detection time might be longer than 2 s if the voltage or frequency shifts too slowly or does not shift at all under certain local loading conditions. Therefore, a sensitive but reliable islanding-detection algorithm has to be implemented in any DG units to ensure the fulfillment of unintentional islanding-detection requirements. In addition to detecting the grid faults, islanding-detection algorithms play another key role in ac microgrid and nanogrid systems. Through the detection of islanding event, these methods allow the control system to precisely decide an appropriate operational mode accordingly. Many islanding-detection algorithms have been proposed in the literature. In general, the islanding detection can adopt either passive or active methods [4]-[7]. Passive methods are simple but susceptible to nondetection zones (NDZ) and incompatible to certain grid codes, such as low- or zero-voltage ride-through (LVRT or ZVRT) requirements. Active methods introduce continuous

perturbations and may distort the converter's output in the case of current perturbation. The performance of active detection methods varies from the operation conditions, and a large perturbation could lead to power quality and system instability concerns. Frequency-based islanding-detection methods are gaining popularity recently as the method itself does not violate the LVRT requirement.

Therefore, it is necessary and also our intention to investigate the inherent mechanism and the converter output frequency dynamic behaviors using a systematic approach, which can be eventually applied to multiple-inverter conditions. This paper is dedicated to the modeling and design procedures for frequency-based islanding detection.

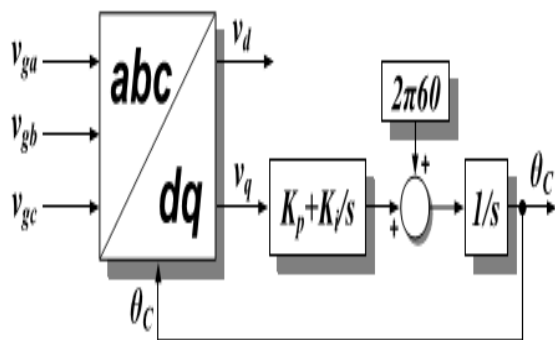


Fig. 1. Synchronous reference frame PLL linear model.

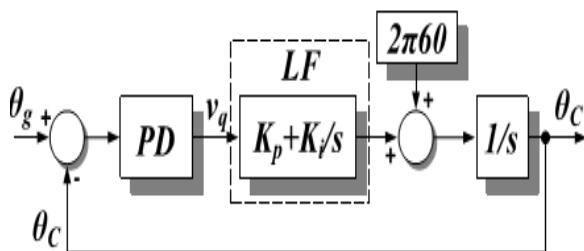


Fig. 2. Typical PLL linear model.

Two types of PLL-based islanding detection methods will be discussed and compared with the typical PLL. Figs. 1 and 2 show the typical SRF PLL structure and its linear model. The closed-loop response is shown in (1), where the phase-

detector gain k_{PD} equals the input ac voltage amplitude V_g .

II. ISLANDING DETECTION BASED ON PLL LARGE-SIGNAL STABILITY

Fig. 3 shows a three-phase power converter system where Z_L and Z_g are the paralleled RLC local load and grid impedances, respectively. The islanding event occurs when the point-of-common-coupling (PCC) switch opens. I_c is the injection current amplitude of the inverter. The modeling of PLL frequency behavior at the islanded condition was presented in [5]. In most cases, the islanding events would be effectively detected by directly monitoring the PLL output frequency. However, for the paralleled RLC load with 60 Hz resonant frequency, the PLL output frequency will stay at the resonant frequency and the system cannot detect the islanding event. Therefore, the PLL or internal control loops are usually modified to detect islanding under such a loading condition.

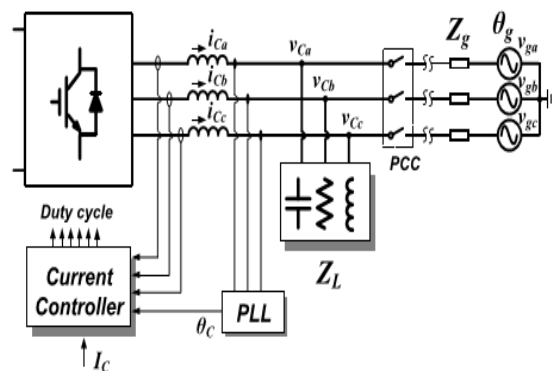


Fig. 3. Three-phase grid-interface power converter system.

The nonlinear PLL model under the islanded condition is shown in Fig. 4. Under the islanded condition, the PLL still tracks the inverter terminal voltage produced by the inverter's current flowing to Z_L . Therefore, there is a self-synchronization loop shown in the model.

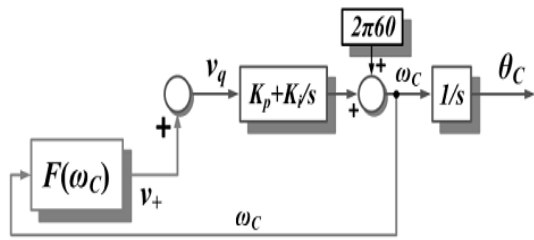


Fig. 4.SRF PLL model under the islanded condition.

This nonlinear PLL model can be linearized around the linefrequency to obtain the small-signal model [5], as shown in Fig. 5. $I_c R_L$ is considered as k_{PD} .

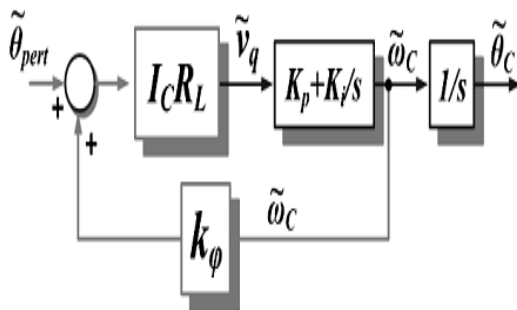


Fig.5.Linearized small-signal PLL model under islanded condition.

If the equilibrium point changes, the PLL output will automatically react to this change. Therefore, many islanding-detection methods are proposed to actively perturb the equilibrium point. Fig. 6 shows an example of PLL-based islanding detection using such a way. An additional large-signal feedback loop is introduced and multiplied by a gain k_{pt} (a 0.5 or 1 Hz small triangular signal between 0 and k_{max}). This additional feedback loop constantly shifts the equivalent resonant frequency. Thus, the PLL output frequency will keep moving all the time.

As shown in Fig. 7, the output frequency will follow the input injection signal k_{pt} . Eventually, the average value ω_{av} of the PLL output will stay lower than 60 Hz to ensure $F = 0$.

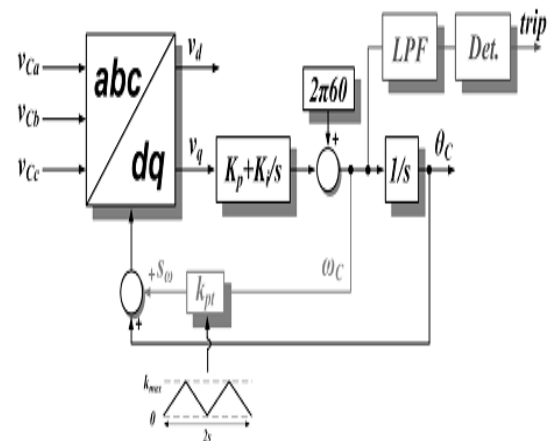


Fig. 6.Modified PLL with a large-signal feedback for islanding detection.

According to Fig. 7, the PLL output ω_c can be directly monitored to detect the islanding condition, and a low-pass filter (LFP) is used to eliminate the high-frequency noise.

The islanding-detection protection signal is set when ω_c is lower than the ω_{th} or the variation range of ω_c is beyond the threshold. The only design parameter is k_{pt} , because it is a very low frequency signal, much lower than the PLL bandwidth. The output of the PLL can be assumed to be at the steady state all the time.

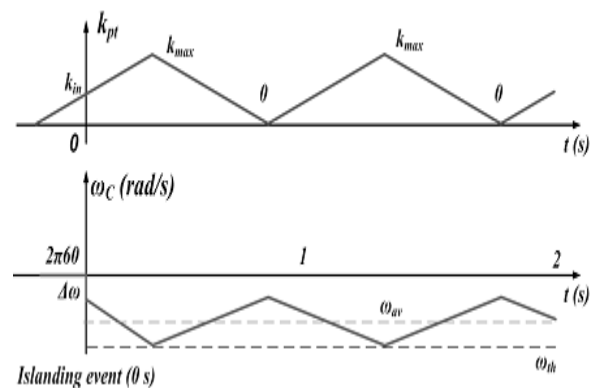


Fig. 7. First PLL output behavior when the islanding condition occurs.

The change of the grid synchronization performance owing to the additional feedback loop can be investigated by exploring the PLL model at the stiff grid-tied mode, as shown in Fig. 9.

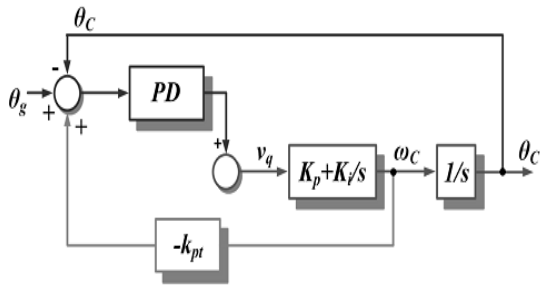


Fig. 9. Modified PLL model under the stiff grid-connected condition.

III. ISLANDING DETECTION BASED ON PLL SMALL-SIGNAL STABILITY

The PLL cannot detect the paralleled RLC load, because the PLL is stable according to (5). Therefore, the equilibrium point itself can be modified to be unstable. With this idea, the PLL can be modified as shown in Fig. 15. An additional small-signal feedback term is introduced with a constant gain N . Then, the equivalent small-signal PLL model around the equilibrium point at the islanded condition is shown in Fig. 16

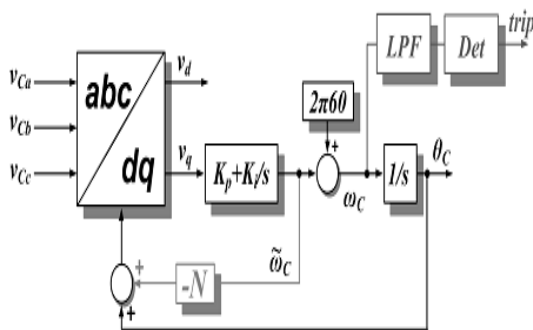


Fig. 15. Modified PLL with a small-signal feedback for islanding detection.

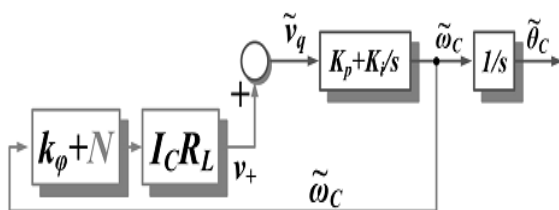
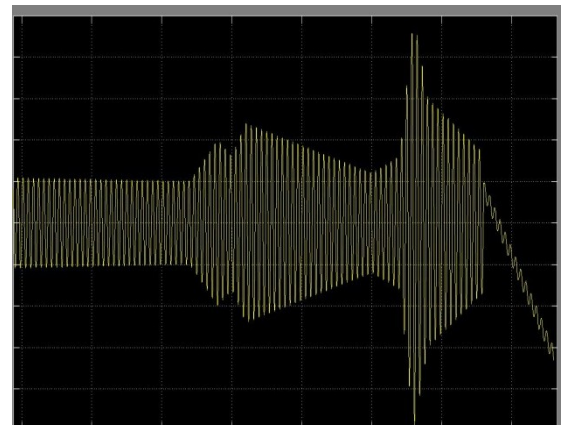
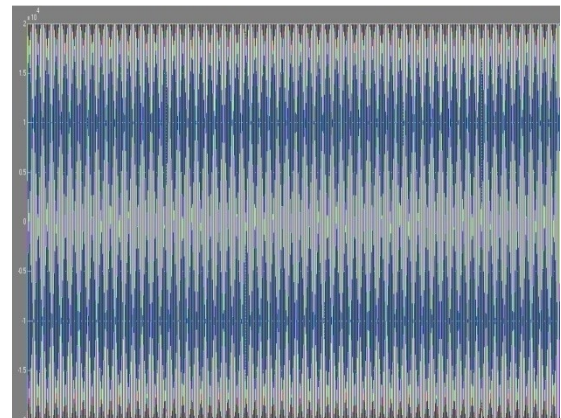
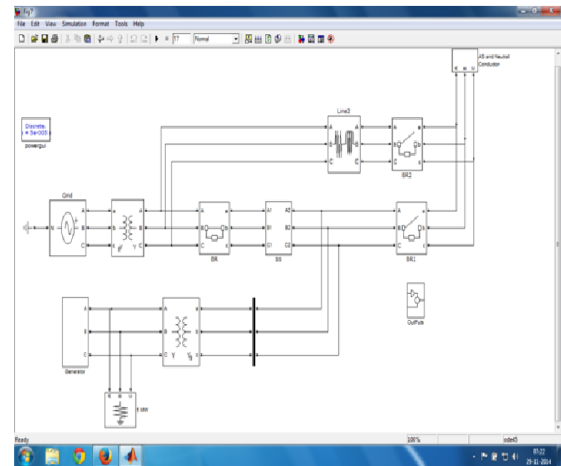
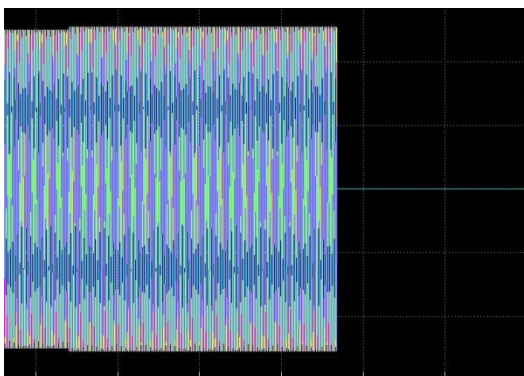
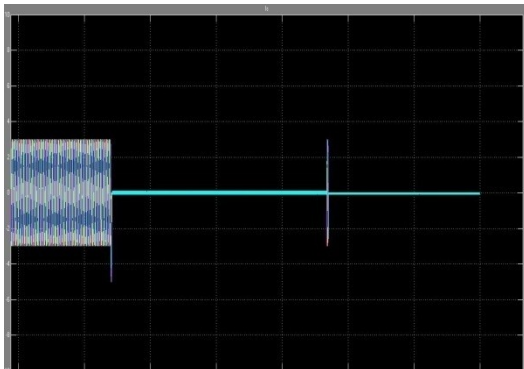
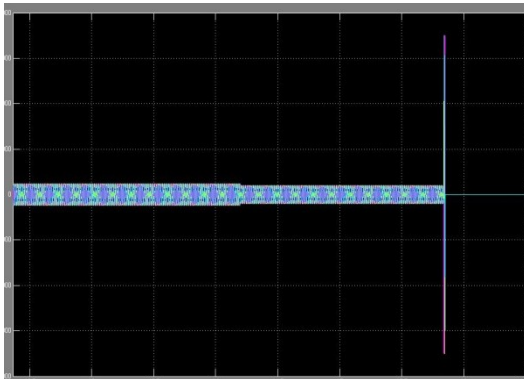
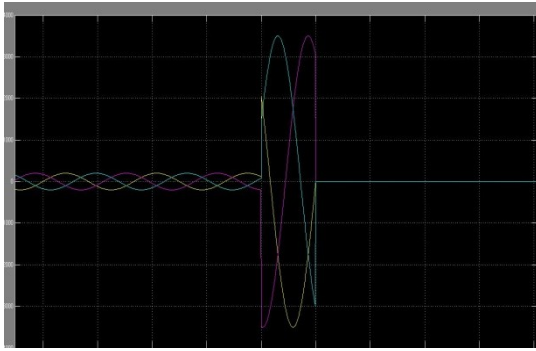


Fig. 16. Small-signal model of the modified PLL for islanding detection.

IV. SIMULATION RESULTS

The PLL behavior is verified in a 2.5 kW two-level three-phase PWM converter system shown below





V. CONCLUSION

The proposed PLL model can be used to analyze and explain the underlying theory for both large-signal-perturbation-based and small-signal positive-feedback-based-islanding-detection solutions. For the large-signal perturbation-based method, the PLL keeps tracking the constantly moving equilibrium point. The change of PLL's grid synchronization performance is very limited and is robust in grid-tied conditions. The detection speed is inherently slow due to the slow PLL bandwidth, thereby requiring a low-frequency, for example, 1 Hz, signal injection. For the small-signal instability-based method, the proposed small-signal PLL model shows that the additional small-signal loop gain design is determined by the local load power quality factor and its resonant frequency to ensure islanding-detection performance.

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BIODATA

Author

AUTHOR:



K GOPI Was Born In Nalgonda, Telegana State , India In1990.He Received The B.Tech Degree In Electrical And Electronics Engineering From The Jawaharlala Nehru Technological Univer City, Hyderabad,India In 2012.completdhis Master Degree From The Same Univercity