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A Closed Loop Fault Tolerant Series Resonant Dc-Dc Converter

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Abstract: *In this project we are implementing the Series-Resonant dc-dc converter (SRC) which is widely utilized in the power supply from the telecommunications, wireless power transfer for electrical vehicle and high voltage power supplies. Here we are developing the fuzzy controller for the better performance. Fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. Therefore in the reconfiguration method of the SRC which is performance for the cases of failure in one semiconductor, which is used to decreases the requirement of the redundancy. According to the proposed scheme the full bridge will be depend upon the SRC which can be reconfigured in the half bridge topology in order to converter the operation without the failure of one switch. According to the demerits of the technique, the output voltage a drop which is half of the original value. Moreover a novel reconfiguration rectifier which is depends upon the voltage doubler methodology which is proposed technique which is used to keep the output voltage constant after the faults. By utilizing the simulation results we can verify the proposed system which confirms the effectiveness of the proposed approach.*

Keywords: DC-DC converter, Fuzzy controller, Full bridge, Half bridge, Series resonant converter.

I NTRODUCTION

The series-resonant dc-dc converter (SRC) has been very used in wireless power transfer application for electrical vehicle [1]–[4], battery charger [5], [6], renewable energy system [7]–[10] and high voltage power supply for specific application, such as traveling-wave tube (TWT) for satellite application [11]. Recently, this topology became very popular in Solid-State Transformer (SST) [12]–[14], mainly because of its characteristic of output voltage regulation in open loop. The SRC has been used for traction application [12], [13], where an efficiency of around 98% was achieved. In SST, telecommunication or even in renewable energy system applications, the continuity of operation is of paramount importance. For that reason, a highly reliable system (preferable with redundancies) is required.

The fault tolerant feature contributes to increase the availability of system and several fault tolerance methods have been proposed in literature [15]– [18]. Most of these methods includes a significant amount of extra hardware (such as semiconductors/leg redundancy [15], [17] or series connection of fuses/switches to isolate the fault [15], [16], [18]), increasing the cost and compromising the efficiency of the system. In this context, this paper proposes a fault tolerance solution with minimum of additional hardware and no impact on efficiency for the SRC converter, using the advantage of inherent fault tolerant capability of this topology. Independently from the mechanism, there are two possible failures types for the semiconductor: open-circuit (OC) or short-circuit (SC). According to the reasons that implies a OC failure are: bond-wire lift off or rupture and failure on the gate drive.

Meanwhile, the SC failure might be a result of an overvoltage, static or dynamic latch up, second breakdown or energy shock. Since most of the failures resultin a SC condition this work focuses on a SRC resilient to SC failure. The proposed reconfiguration scheme consists in reconfiguring the full-bridge SRC (FB-SRC) in a half-bridge SRC (HB-SRC) converter. Nevertheless, the output voltage generated by the HB-SRC is half of the output generated by the FB-SRC, considering the same parameters. Therefore, a novel re-configurable rectifier based on the voltage-doubler topology is proposed in order to keep the same output voltage.

III. O PERATION PRINCIPLE OF THE SR CONVERTER

A. Full-Bridge SRC

The topology of the SRC based on full-bridge configuration (FB-SRC) is shown in Fig. 1 (a). To simplify the description, an unidirectional topology is considered in this analysis and a diode bridge rectifier is used in the secondary side. To support the analysis, the variables resonant frequency (fo), resonant angular frequency (w0) and characteristic impedance of the resonant network (Z) are defined by (1), in terms of the resonant inductor (L r) and capacitor (Cr) of the tank circuit

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, \omega_0 = 2\pi f_0, Z = \sqrt{\frac{L_r}{C_r}} \qquad (1)$$

Fig. 1 (c) shows the main waveforms for the FB-SRC operating at the resonant frequency (f s = fo) and below the resonant frequency (f s < fo), where f s is the switching frequency. For operation below the resonant frequency, the current i Lr reaches zero before half of the

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switching period, and it remains zero until the primary bridge applies negative output voltage, i.e. v p = Vi . Since the commutations happen when i Lr = 0, all semiconductors switch at zero-current-switching (ZCS), avoiding therefore switching losses. The converter parameters must satisfy the following conditions [21]:

$$\gamma = \frac{\omega_0}{2f_s} > \pi \quad (2)$$

$$f_s < f_0 \quad (3)$$

$$I_0 < 8 f_s C_r V_0 \quad (4)$$

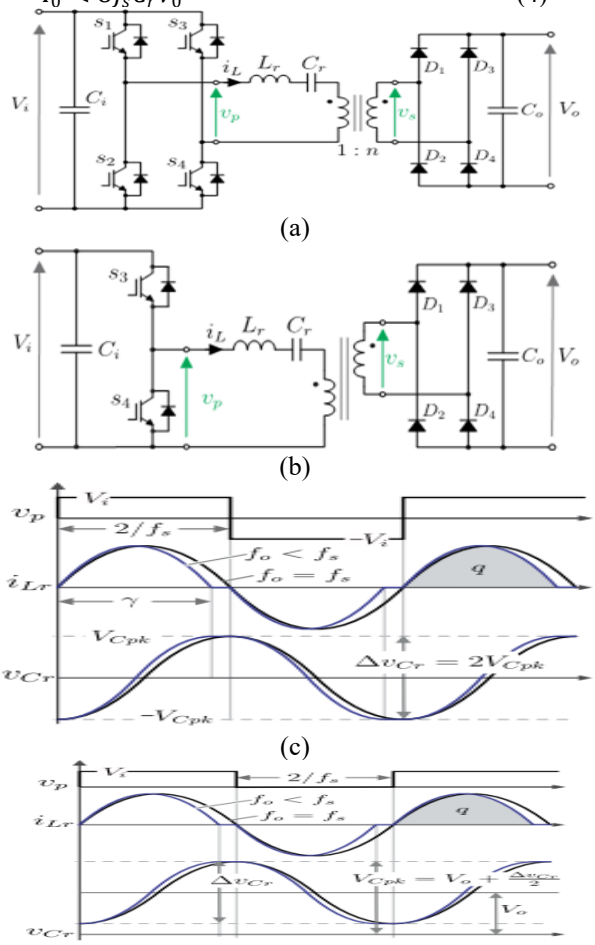

Figure 1. Series Resonant dc-dc converter: (a) topology of the FB-SRC, (b) Topology of the HB-SRC, (c) main waveforms of the FB-SRC and (d) main waveforms of the HB-SRC

where, g is the angular length of one half switching period and Io is the load current. From these conditions is possible to design L r and Cr , considering the operation range of the converter. The relation between the amount of charge stored in the capacitor (Dq) and its voltage (v Cr) is given by (5). During the period 0 < t < T 0 (where T 0 is the resonant period), the capacitor voltage starts from V Cpk and reaches V Cpk (see Fig. 1 (c)), thus Dv Cr = 2V Cpk . Likewise, the charge that flows through the capacitor during this period is defined as q, as shown in Fig. 1 (c). This relation is described in (6)

$$\Delta q = C_r \Delta v_{C_r} \quad (5)$$

$$q = 2.C_r.V_{C_{pk}} \quad (6)$$

The instantaneous average value of the input current (i i) is calculated by (7). As highlighted in this equation, the integral of the current during the time interval 0 to T s =2 is the charge accumulated in the capacitor (see Fig. 1 (c)). Thus, the relation presented in (8) is found

$$I_i = \langle i_1(t) \rangle_{T_s} = \frac{2}{T_s} \underbrace{\int_0^{T_s/2} i_1(t)dt}_{q} \quad (7)$$

$$I_i = 2 f_s q \quad (8)$$

Replacing (8) in (6), (9) is obtained, and it can be rearranged to obtain the peak voltage on the capacitor in function of the load (represented in this equation by the input current Ii), switching frequency and capacitance value, as presented in (10).

$$\frac{I_i}{2 f_s q} = 2.C_r.V_{C_{pk}} \quad (9)$$

$$V_{C_{pk}} = \frac{I_i}{8 f C_{r_s}} \quad (10)$$

The output voltage of the converter is given by (11).

$$V_0 = n V_i \quad (11)$$

B. Half-Bridge SRC

Besides the circuit shown in Fig. 1 (a), the series-resonant dc-dc converter can be also implemented based on the halfbridge topology (HB-SRC), as shown in Fig. 1 (b). This circuit became well-known in literature as LLC converter, due to the configuration of the tank circuit, considering the magnetizing inductance of the transformer, and it has been widely used in telecommunications power supply applications.

The operation of the HB-SRC is very similar to the one of the FB-SRC converter, previously described. As can be seen in Fig. 1 (c) and (d), the FB-SRC synthesizes an ac voltage v p on the tank circuit input, with negative and positive values (Vi , Vi), while the HB-SRC generates a rectangular waveform voltage v p with zero and positive values (0, Vi). As a consequence, the output rectified voltage on the secondary side of the HB-SRC is given by (13), which is half of the value, when compared to the FB-SRC output voltage (see eq. (11)) for the same parameters (Vi and n). The main waveforms for the HB-SRC are shown in Fig. 1 (d).

$$V_{C_p} = \frac{I_i}{8 f_s C_r} + V_o \quad (12)$$

$$V_o = \frac{n V_i}{2} \quad (13)$$

IV. P ROPOSED FAULT TOLERANT CONVERTER

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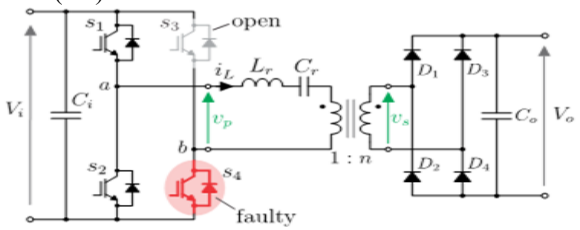
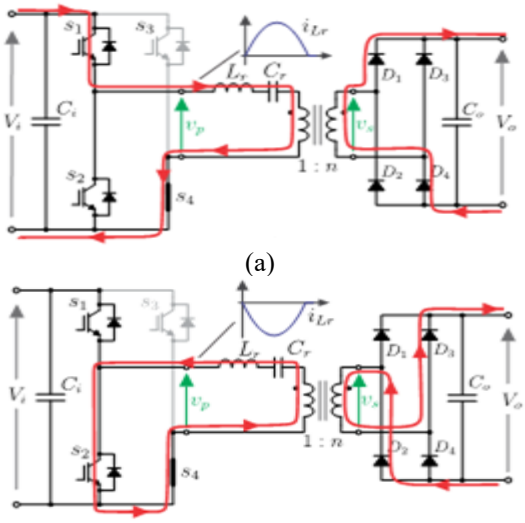
As already mentioned, depending on the semiconductors failure mechanisms, the device will assume two possible states: open-circuit (OC) or short-circuit (SC) .



IGBT's states before and after failure

	Normal	Failure
s_1	$d = 0.5$	$d = 0.5$
s_2	$\overline{s_1}$	$\overline{s_1}$
s_3	$d = 0.5$	open
s_4	$\overline{s_3}$	short circuit

Figure 2. FB-SRC under faulty condition: SC failure on the semiconductors4



(a)

(b)

Figure 3. Operation of the FB-SRC as a HB-SRC after the reconfiguration.
States operation of the SRC after the fault: (a) positive iL current (first state),
(b) negative iL current (second state).

A. Reconfiguration Scheme: Operation and Control Level

The proposed reconfiguration scheme for the SRC consists in configuring the FB-SRC in a HB-SRC after the fault, i.e. SC of a semiconductor. The detailed analysis is carried out in this section for the FB-SRC shown in Fig. 2. Initially, as an example, it is assumed that the switch s4 is damaged in SC (see Fig. 2), hence the switch s3 must remain open, avoiding short-circuit of the input voltage source.

Since the switch s4 is short-circuited, the point b (highlighted in Fig. 2) is directly connected to the primary side ground and the damaged device is used as a circuit path, resulting in the same circuit of the Fig. 1 (b). Meanwhile, the healthy leg (composed of s1 and s2) operates normally. Fig. 3 shows the operation states of the SRC after the fault, i.e. after the reconfiguration, where it can be seen that the damaged switch s4 being used as a circuit path. Fig. 4 shows the main waveforms of the FB-SRC when a fault happens. As the HB-SRC provides only half of the output voltage compared to the FB-SRC, the output voltage of the converter after the fault will be half of its original value, which is not desired. Thereafter, to overcome this problem and keep the output voltage constant after the fault, a modification to the circuit of the secondary side rectifier is proposed and a novel re-configurable rectifier is obtained.

B. Fault-Tolerant SRC:

Topology and Hardware Level Fig. 5 (a) shows the topology of the standard full-bridge rectifier (FBR), which is the most used in the secondary side of the SRC [11], [3]- [10]. In this configuration, the output is given by: v o = v s pk . Fig. 5(b) shows the topology of the voltage-doubler rectifier (VDR), which is also popular in the literature, however it has not so far been applied to the SRC. In this configuration, the rectified output voltage is given by: v o = 2v s pk .

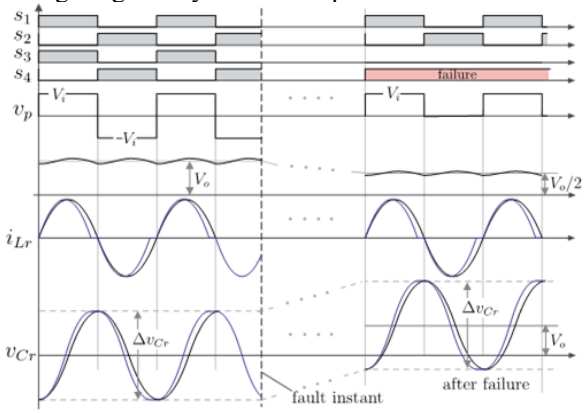


Figure 4. Main waveforms of the FB-SRC when a fault happens: main
voltages and currents before and after the fault

constant, a re-configurable rectifier circuit presented in Fig. 5 (c) is proposed. The proposed rectifier has two split capacitors and an additional switch (Sf) that allows to connect one side of the high frequency transformer secondary winding directly to the middle point of the capacitors, becoming a VDR. The operation in normal and faulty conditions is depicted in Fig. 5 (d) and Fig. 5 (e), respectively.

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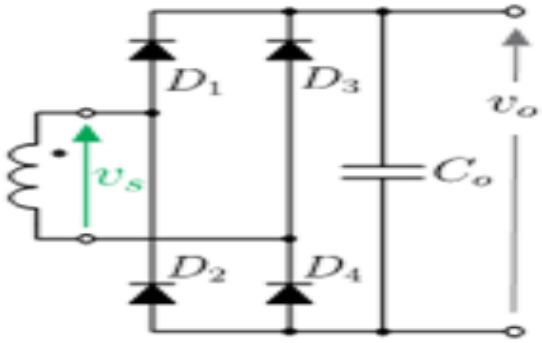
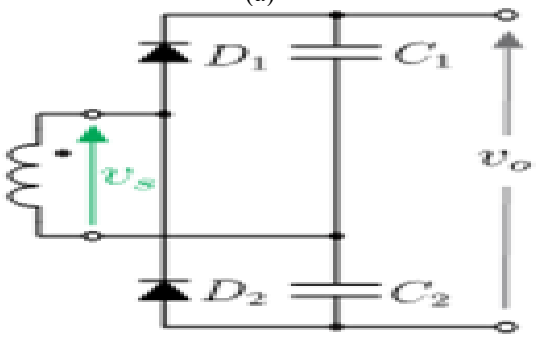
In normal operation, the switch S f is open, and the rectifier operates as a standard FBR. In fault case, the switch S f is on, and then the leg composed of the diodes D3 and D4 is bypassed. The bottom side of the secondary winding is connected to the middle point of the capacitors C1 and C2 , as depicted in Fig. 2 (e). Finally, Fig. 6 shows the complete proposed fault-tolerant seriesresonant dc-dc converter (FT-SRC). The main waveforms for the proposed FT-SRC before and after a failure are depicted in Fig. 7.

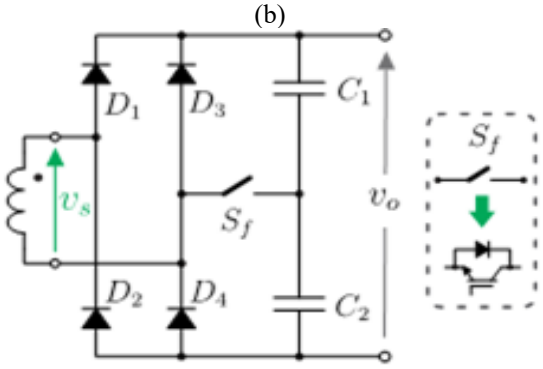
The effect of the reconfiguration is only observed on the voltage v Cr , that has an expected offset of Vo, and on the the current i Lr , that must be twice the previous value to process the same amount of power than before.



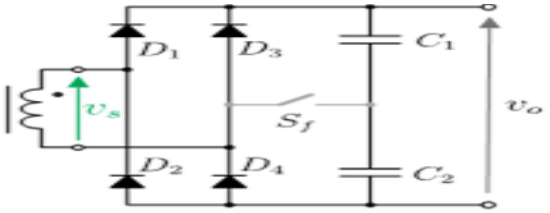
(a)



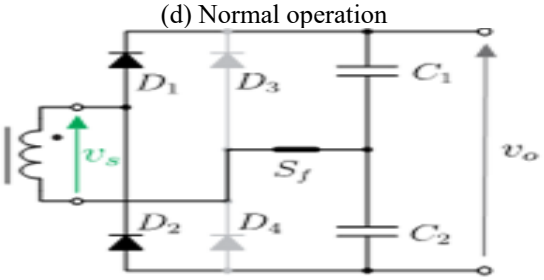
(b)



(c)



(d) Normal operation



(e) Faults operation

Figure 5. Possibles rectifier topologies and proposed topology: (a) fullbridge rectifier (FBR), (b) voltage-doubler rectifier (VDR) and (c) proposed reconfigurable rectifier. Operation of the proposed rectifier: (d) operation as a FBR, (e) operation as a VDR.

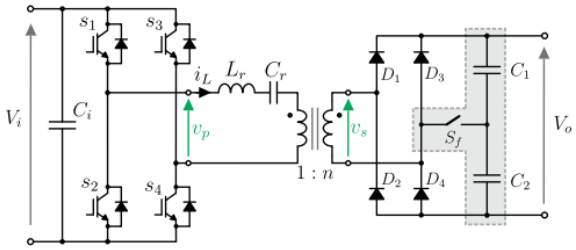


Figure 6. Proposed fault-tolerant SRC topology.

protection by gate voltage limiting, current mirror method [23] and gate voltage sensing [20] are very promised. All this indicated methods require the sensing of device collector voltage and/or current and therefore they are considerably simple to be implemented. Fig. 8 shows the protection method based on the de-saturation detection interfaced with the logic system, used to diagnosis the faulty leg.

In case of fault of the switch s4, the collector voltage of s3 (v ceS3) increases from the low saturation value to the dc link, while the gate signal is still high.

CLOSED-LOOP SYSTEM TRANSFER FUNCTION

The Transfer Function of any electrical or electronic control system is the mathematical relationship between the systems input and its output, and hence describes the behaviour of the system. Note also that the ratio of the output of a particular device to its input represents its gain. Then we can correctly say that the output is always the transfer function of the system times the input. Consider the closed-loop system below.

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Typical Closed-loop System Representation

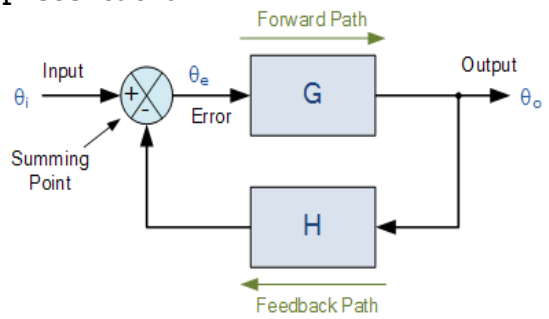

Fig 7.Bolck diagram of closed loop system

Where: block G represents the open-loop gains of the controller or system and is the forward path, and block H represents the gain of the sensor, transducer or measurement system in the feedback path.

To find the transfer function of the closed-loop system above, we must first calculate the output signal θo in terms of the input signal θi. To do so, we can easily write the equations of the given block-diagram as follows.

The output from the system is equal to: Output = G x Error

Note that the error signal, θe is also the input to the feed-forward block: G

The output from the summing point is equal to: Error = Input - H x Output

If H = 1 (unity feedback) then:

The output from the summing point will be: Error (θe) = Input - Output

Eliminating the error term, then:

The output is equal to: Output = G x (Input - H x Output)

Therefore: G x Input = Output + G x H x Output

Rearranging the above gives us the closed-loop transfer function f: $\frac{\text{output}}{\text{Input}} = \frac{G}{1+GH}$ (16)

Advantages of Closed Loop Control System

1.Closed loop control systems are more accurate even in the presence of non-linearity.

2.Highly accurate as any error arising is corrected due to presence of feedback signal.

3.Bandwidth range is large.

4.Facilitates automation.

5.The sensitivity of system may be made small to make system more stable.

6.This system is less affected by noise.

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

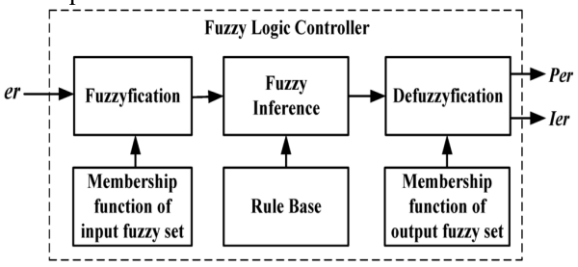

Fig.8.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

TABLE I: Fuzzy Rules

e / ė	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (12)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (13)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used

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and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. To achieve this, the membership functions of FC are: error, change in error and output
The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (14)$$

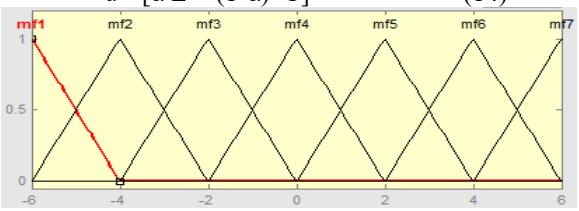

Fig 9 input error as membership functions

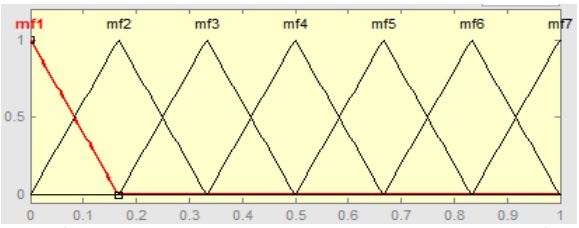

Fig 10 change as error membership functions

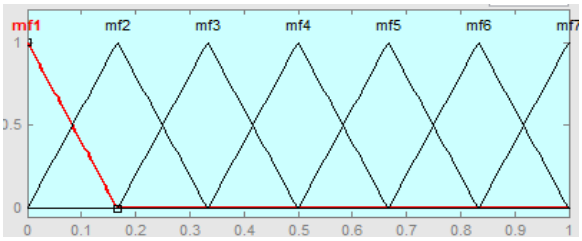

Fig.11 output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

V. SIMULATION RESULTS

In order to verify the performance of proposed FT-SRC converter and to attest the theoretical analysis presented in this paper in simulation results were obtained. Fig. 9 shows photo of the main waveforms for the converter operating in steady-state at nominal condition.

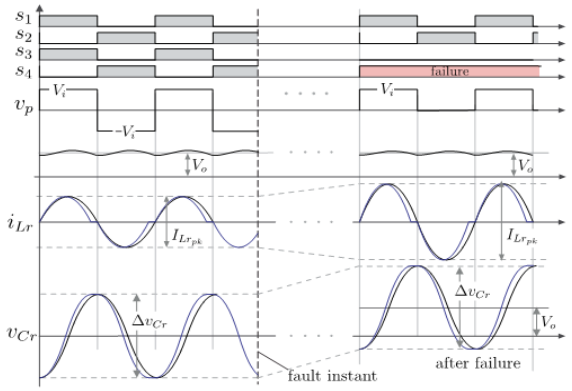

Figure12. Main waveforms of the proposed FT-SRC when a fault happens:
main voltages and currents before and after the fault

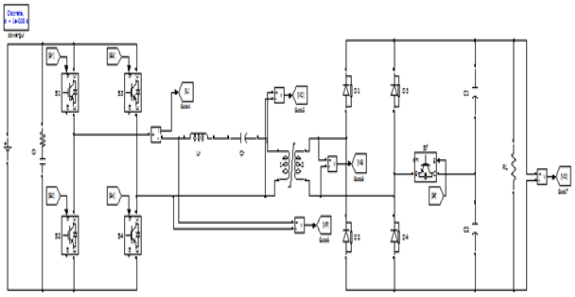

Figure 13.Simulation circuit closed loop SRC

The results were obtained for the converter operating

Table II
Specification of The SRC Parameter

Input voltage	$V_i = 700$ V
Output voltage	$V_o = 600$ V
Nominal output power	$P_o = 10$ kW
Switching frequency	$f_s = 20$ kHz
Transformer turn ratio	$n = 1.45$

Table III
Main Parameters of The Tank Circuit

Resonant capacitance	$C_r = 0.68\mu F$
Resonant Inductor	$L_r = 79\mu H$
Tank resonant angular frequency	$\omega_0 = 1.364 \cdot 10^5$ rad/s
Resonant frequency	$f_o = 21.7$ kHz
Angular length of half switching period	$\gamma = 0.577$

steady-state (before and after the fault) and also dynamically during the fault and they are discussed herein.

The test was performed with input and output voltage of 200 V and 300 V, respectively, and the results for this condition are presented in Fig. 10. The dynamic response of the FB-SRC during the fault of the switch s2 is depicted in Fig. 10 (a), in which is observed the the

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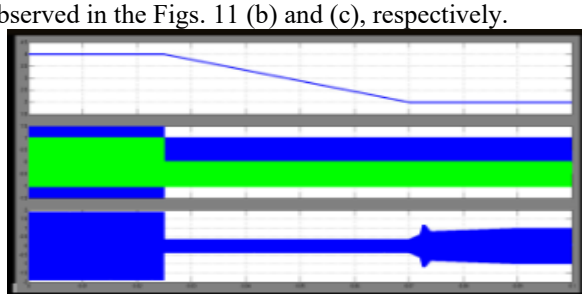
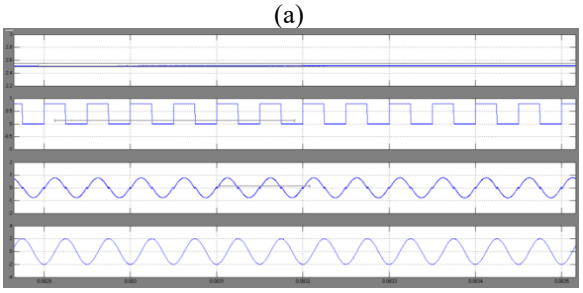
converter remains operational after the fault, proving its inherent ability to handle the fault, as described in Section III. The inductor current is also reduced, because the test was performed with constant resistance as load and therefore reduction on the output voltage implies in reduction on power. The detailed waveforms before and after the fault can observed in the Figs. 10 (b) and (c), respectively.

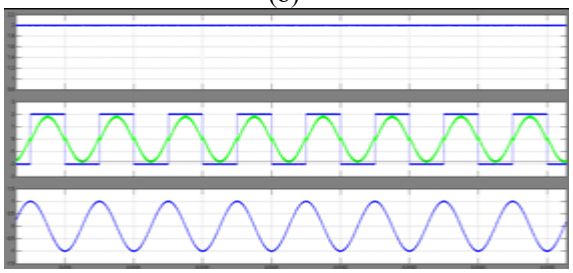
The dynamic behavior during the fault on switch s2 of the proposed FT-SRC is shown in Fig. 11 (a) and as can be seen in this figure, the converter remains operational after the fault and it provides a constant output voltage (500 V) even after the fault, attesting the effectiveness of the proposed rectifier and the converter. The detailed waveforms before and after the fault can observed in the Figs. 11 (b) and (c), respectively.



(a)



(b)



(c)

Figure 14. simulation results of the FB-SRC (without the reconfigurable rectifier on the secondary side) under a fault on the switch s2: (a) dynamic behavior of the converter during the fault, (b) steady-state operation before the fault and (c) steady-state operation after the fault.

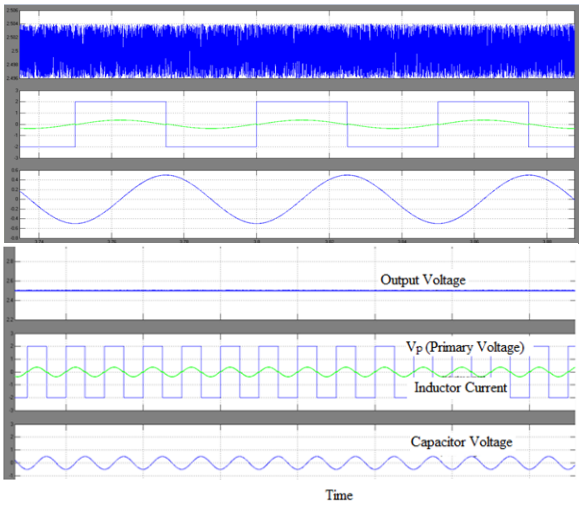


Figure 15. From the above fig basic wave sorts of the close hover with cushy controller FB-SRC the outline plotted on Y-center yield voltage, inductor present, fundamental voltage, capacitor voltage and on X-center time .

VI. CONCLUSION

In this project we are implementing the proposed faults tolerant series resonant dc-dc converter with the combination of the fuzzy controller. Therefore the basic operation of the SRC will be depend upon the full bridge and half bridge topologies. In this paper we are developing the fuzzy logic controller for the better performance comparing the other controller .therefore semiconductor short circuit fault will be evaluated for the full bridge series resonant converter and with the reconfiguration technique in which the FB-SRC will be operate with the HB-SRC will be presented. Therefore according to the reconfiguration scheme, the output voltage will be decreases .The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. After utilizing the fuzzy we can overcome the problem of the rectifier which van be reconfigured in the voltage doublers rectifier and it keep the output voltage constant which is proposed in this paper. There are main merits of the proposed converter are: post fault operation, simple implementation, reduced number of additional components and no efficiency deterioration. By using simulation results we can analysis the effectiveness and advantages of the proposed fault tolerant series resonant dc-dc converter.

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