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Vedic Multiplier based Fault Tolerant FFTs through Verilog HDL

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Abstract: *Algorithmic-Based Fault Tolerance (ABFT) technique is used to exploit the algorithmic properties to detect and correct errors. One example is Fast Fourier transforms (FFTs) that is used in spectral analysis in the communication. There are several protection schemes to detect and correct errors in FFTs. Among those, most likely the utilization of the Parseval or add of squares check is that the most generally glorious. The Parseval or sum of square check is the most widely known. It is most common to find several blocks operating in parallel in the modern communication systems. Recently, a method that exploits this truth to implement fault tolerance on parallel filters has been projected. During this temporary, this system is 1st applied to guard FFTs. Then, 2 improved protection schemes that mix the utilization of error correction codes and Parseval checks are projected and evaluated. This project outspread with FFT using Vedic multiplier. Simulation results are observed using Xilinx.*

Keywords-Error correction codes, Fast Fourier transform, sum of square, Vedic multiplier.

I.INTRODUCTION

Filters are typically used in electronic systems to emphasize signals in bound frequency ranges and reject signals in alternative frequency ranges. In circuit theory, a filter is associate electrical network that alters the amplitude and/or section characteristics of a symbol with relevance frequency. Ideally, a filter won't add new frequencies to the input signal, nor can it modification the part frequencies of that signal, however it'll modification the relative amplitudes of the numerous frequency elements and/or their section relationships. Now -a-days filter area unit wide used in range of applications that supported automotive, medical, and house wherever reliableness of elements in digital electronic circuits is essential. Filters of some type area unit essential in the operation of most electronic circuits. There area unit several totally different bases of classifying filters and these overlap in several different ways; there is no straightforward hierarchal classification. Because the behavioral properties of signal changes the techniques of filtering it'll be take issue. Being specific with filter, the digital filters have large applications in digital signal process. Filtering is additionally a category of signal process, the process feature of filters being the complete or partial suppression of some facet of the signal. it's thus within the interest of anyone concerned in electronic circuit style to possess the flexibility to develop filter circuits capable of meeting a given set of specifications. In signal process, a digital filter is a device or process that removes some unwanted element or feature from an indication. Digital filters are used for 2 general purposes; separation of signals that are combined, and restoration of signals that are distorted in some approach. Most often, this suggests removing some frequencies and not others so as to suppress interfering signals and scale back background signal.

This parallel operation is exploited for fault tolerance. In fact, dependableness may be a major challenge for electronic system. Specifically, soft errors are a very important issue, and lots of techniques are planned over the years to mitigate them. a number of these techniques modify the low-level style and implementation of the integrated circuits to stop soft errors from occurring. Different techniques work on the next abstraction level by adding redundancy which will observe and proper errors. The protection of digital filters has been wide studied. for instance, fault-tolerant implementations supported the utilization of residue variety systems or arithmetic codes are planned. The utilization of reduced exactness replication or word-level protection has been additionally studied another choice to perform error correction is to use 2 completely different filter implementations in parallel. All those techniques concentrate on the protection of one filter.

Error coding is employed for fault tolerant computing in computer memory, magnetic and optical information storage media, satellite and part communications, network communications, cellular phone networks, and almost any other type of digital communication. Error writing uses mathematical formulas to code information bits at the source into longer bit words for transmission. The "code word" will then be decoded at the destination to retrieve the information. the additional bits

within the code word offer redundancy that, in line with the writing theme used, will allow the destination to use the decryption method to determine if the communication medium introduced errors and in some cases correct them in order that the info needn't be retransmitted. Totally different error writing schemes are chosen depending on the kinds of errors expected, the communication medium's expected error rate, and whether or not or not information retransmission is feasible. Quicker processors and higher communications technology create a lot of complex coding schemes, with higher error police work and correcting capabilities, attainable for smaller embedded systems, allowing a lot of strong communications. However, tradeoffs between information measure and writing overhead, writing complexness and allowable writing delay between transmissions, should be thought of for every application.

A Concept of Fault Tolerance

A number of techniques is used to defend a circuit from errors. Those vary from modifications within the producing method of the circuits to reduce the amount of errors to adding redundancy at the logic or system level to make sure that errors don't have an effect on the system practicality. Digital Filters square measure one among the foremost normally used signal process circuits and a number of other techniques are projected to guard them from errors. There square measure range of ways accustomed establish faults and also the actions necessary to correct the faults at intervals circuit. Digital filters square measure wide used in signal process and communication systems. There square measure completely different fault tolerance approaches to typical process circuits and also the DSP circuits. In some cases, the dependableness of these systems is vital, and fault tolerant filter implementations square measure required. Over the years, several techniques that exploit the filters structure and properties to attain fault tolerance are projected. All together the techniques mentioned to this point, the protection of one filter is taken into account.

Transient errors can often upset more than one bit producing multi-bit errors with a very high probability of error occurrence in neighboring memory cells. Bit interleaving is one technique to remedy multi-bit errors in neighboring memory cells as physically adjacent bits in memory array are assigned to different logical words. The single-error-correction, double-error-detection, and double-adjacent-error-correction (SEC-DED-DAEC) codes have previously been presented to correct adjacent double bit errors. The required number of check bits for the SECDED-DAEC codes is the same as that for the SEC-DED codes. In addition, the area and timing overheads for encoder and decoder of the SEC-DED-DAEC codes are similar to those of the SEC-DED codes. Consequently, adjacent double bit errors can be remedied with very little additional cost using the SECDED-DAEC codes. The SEC-DED-DAEC codes may be an attractive alternative to bit interleaving in providing greater flexibility for optimizing the memory layout. Furthermore, the SEC-DED-DAEC code can be used in conjunction with bit interleaving and this method can efficiently deal with adjacent multi-bit errors. The FFTs in parallel increases the scope of applying error correction codes together. Generating parity together for parallel FFTs also helps in minimizing the complexity in some ECC. By assuming that there can only be a single error on the system in the case of radiation-induced soft errors and may be two in worst case. The proposed new technique is based on the combination of Partial Summation combined with parity FFT for multiple error correction.

II. LITERATURE SURVEY

[1]Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic-based fault tolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT. One example is fast Fourier transforms (FFTs) that are a key building block in many systems. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, probably the use of the Parseval or sum of squares check is the most widely known. In modern communication systems, it is increasingly common to find several blocks operating in parallel. Recently, a technique that exploits this fact to implement fault tolerance on parallel filters has been proposed. In this brief, this technique is first applied to protect FFTs. Then, two improved protection schemes that combine the use of error correction codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection.

[2]In this paper, fault tolerance based system based on Error Correction Codes (ECCs) using Verilog is designed, implemented, and tested. It proposes that with the help of ECCs i.e. Error Correction Codes there will be more protected Parallel filter circuit has been possible. The filter they have used for error detection and correction are mainly finite-impulse response (FIR) filters. They have been used Hamming Codes for fault correction in which they takes a block of k bits and produces a block of n bits by adding n−k parity check bits. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. In this scheme they have used redundant module in which the data and parity check bits are store d and can be recovered later even if there is an error in one of the bits. This is done by re -computing the parity check bits and comparing the results with the values stored. In this way using hamming codes error can be detected and corrected within the circuit.

[3] In this paper, Triple Modular Redundancy (TMR) and Hamming Codes have been used to protect different circuits against Single Event Upsets (SEUs). In this paper, the use of a Novel Hamming approach on FIR Filters is studied and implemented in order to provide low complexity, reduce delay and area efficient protection techniques for higher bits data. A novel Hamming code is proposed in this paper, to increase the efficiency of higher data bits. In this paper, they have proposed technique used to demonstrate, how the lot of overhead due to interspersing the redundancy bits, their subsequent removal, pad to pad delay in the decoder and consumption of total area of FIR filter for higher bits are reduced. These are based on the novel hamming code implementation in the FIR filter instead of conventional hamming code used to protect FIR filter. In this scheme Hamming code used for transmission of 7-bit data item.

[4] In this paper, the design of a FIR filter with self checking capabilities based on the residue checking is analyzed. Usually the set of residues used to check the consistency of the results of the FIR filter are based of theoretic considerations about the dynamic range available with a chosen set of residues, the arithmetic characteristics of the errors caused by a fault and on the characteristic of the filter implementation. This analysis is often difficult to perform and to obtain acceptable fault coverage the set of chosen residues is overestimated. Obtained result and therefore requires that Instead, in this paper they have showed how using an exhaustive fault injection campaigns allows to efficiently select the best set of residues. Experimental results coming from fault injection campaigns on a 16 taps FIR filter demonstrated that by observing the occurred errors and the detection modules corresponding to different residue has been possible to reduce the number of detection module, while paying a small reduction of the percentage of SEUs that can be detected. Binary logic dominates the hardware implementation of DSP systems

[5] In this paper they have proposed architecture for the implementation of fault -tolerant computation within a high throughput multirate equalizer for an asymmetrical wireless LAN. The area overhead is minimized by exploiting the algebraic structure of the Modulus Replication Residue Number System (MRRNS). They had demonstrated that for our system the area cost to correct a fault in a single computational channel is 82.7%. Fault tolerance within MRRNS architecture is implemented through the addition of redundant channels. This paper has presented a detailed analysis of the cost of implementing single fault correction capability in a FIR filter using the MRRNS. The fault-tolerant architecture makes use of the algebraic properties of the MRRNS, and has been shown to provide significant area savings when compared with general techniques. This architecture also requires few additional components to be designed, as identical redundant channels are used, and the polynomial mapping stages are simply expanded from the original components.

III. ERROR TOLERANT TECHNIQUES FOR PARALLEL FFTS

Error Correction based on Hamming Codes

The impulse response $h[n]$ completely defines a discrete time filter that performs the following operation on the incoming signal $x[n]$:

$$\boldsymbol{y[n]} = \sum_{l=0}^{\infty} \mathrm{x[n-l].h[l]} \ldots\ldots\ldots\ldots\ldots (1)$$

This property can be exploited in the case of parallel filters that operate on different incoming signals, as shown on Fig. 1. In this case, four filters with the same response process the incoming signals $x\,1[n]$, $x\,2[n]$, $x\,3[n]$, and $x\,4[n]$ to produce four outputs $y\,1[n]$, $y\,2[n]$, $y\,3[n]$, and

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y 4[n]. To detect and correct errors, each filter can be viewed as a bit in an ECC, and redundant filters can be added to form parity check bits. This is also illustrated in Fig. 1, where three redundant filters are used to form the parity check bits of a classical single error correction Hamming code. Those correspond to the outputs $z1[n]$, $z2[n]$, and $z3[n]$. Errors can be detected by checking if

$$Z_1[n]=y_1[n]+y_2[n]+y_3[n]$$
$$Z_2[n]=y_1[n]+y_2[n]+y_4[n]$$
$$Z_3[n]=y_1[n]+y_3[n]+y_4[n]$$

When some of those checks fail, an error is detected. The error can be corrected based on which specific checks failed. For example, an error on filter y 1 will cause errors on the checks of $z1$, $z2$, and $z3$.

TABLE I
ERROR LOCATION IN HAMMING CODE

$c_1c_2c_3$	Error Bit Position
000	No Error
111	Z_1
110	Z_2
101	Z_3
011	Z_4
100	Z_5
010	Z_6
001	Z_7

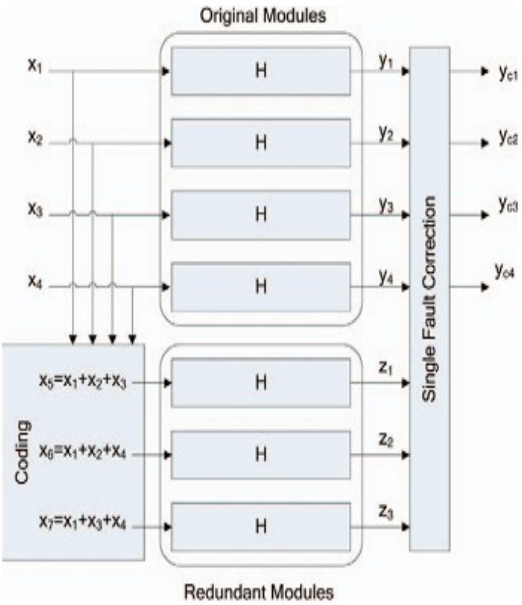

Fig. 1. ECC-based scheme for four filters and a Hamming code.

The proposed schemes have been evaluated using FPGA implementations to assess the protection overhead. The results show that by combining the use of ECCs and Parseval checks, the protection overhead can be reduced compared with the use of only ECCs.

Fault tolerant FFT based on Parseval's check

Parseval's technique is one amongst the techniques to detect errors parallel in multiple FFT. this is often achieved with sum of Squares (SOSs) check [5] supported Parseval's theorem. The error free FFT should have its sum of Squares of the input equaling the total of Squares of its frequency domain output. This correlation are often accustomed establish errors with minimum overhead. For parallel FFTs, the Parseval's check are often combined with the error correction codes to attenuate the realm overhead. Multiple error detection and correction is achieved through this mix. one amongst the straightforward ways in which is to come up with the redundant input for single FFT with all the four FFT inputs. To correct error the parity FFT output is XORed with fault free outputs of the FFTs. Compared to the previous schemes bestowed within the Fault Tolerant Parallel FFTs victimization Error Correction Codes and Parseval Checks [1], this technique reduced the whole variety of sum of Squares used. Another existing work done is by combining SOS checks with hamming codes rather than exploitation Parseval's check on an individual as shown in Fig2.

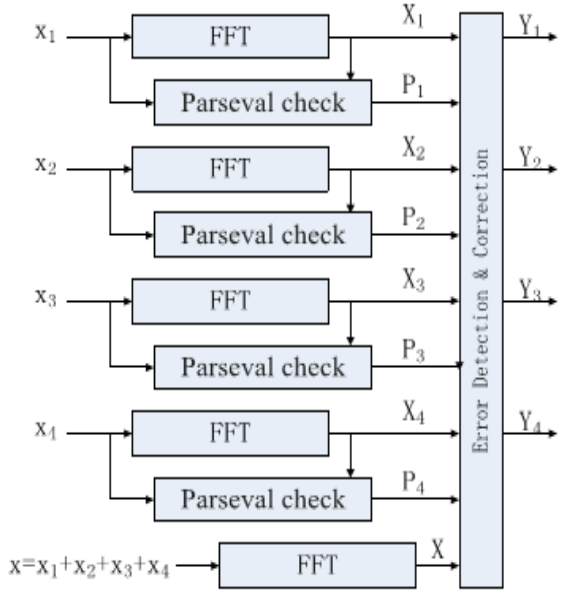

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Fig. 2. Parity-SOS (first technique) fault-tolerant parallel FFTs.

This method combines the feature of parity calculation of hamming codes and error detection process of Sum of Squares. Concurrent Error Detection (CED) schemes for the FFT are the Sum of Squares (SOS) check based on Pa theorem. The use of parseval check is exponentially reduced to the direct comparisons of FFTs inputs and outputs used to protect parallel FFTs.

IV. PROPOSED PROTECTION SCHEMES FOR PARALLEL FFTS

The place to begin for our work is that the protection theme based on the utilization of ECCs that was for digital filters. This theme is shown in Fig1. In this example, a straightforward single error correction playacting code is employed. The initial system consists of 4 FFT modules and 3 redundant modules is value-added to sight and correct errors. The inputs to the 3 redundant modules area unit linear combos of the inputs and that they area unit used to check linear combos of the outputs. For example, the input to the primary redundant module is

$$x_5=x_1+x_2+x_3$$

and since the DFT is a linear operation, its output z5 can be used to check that

$$z_5=z_1+z_2+z_3$$

This will be denoted as c1 check. The same reasoning applies to the other two redundant modules that will provide checks c2 and c3. Based on the differences observed on each of the checks, the module on which the error has occurred can be determined. The different patterns and the corresponding errors are summarized in Table I. Once the module in error is known, the error can be corrected by reconstructing its output using the remaining modules. For example, for an error affecting z1, this can be done as follows:

$$Z_{1c}[n]=z_5[n]-z_2[n]-z_3[n]$$

Similar correction equations can be used to correct errors on the other modules. More advanced ECCs can be used to correct errors on multiple modules if that is needed in a given application. For example, to protect four FFTs, three redudant FFTs are needed, but to protect eleven, the number of redundant FFTs in only four. This shows how the overhead decreases with the number of FFTs.

$$X_{1c}=X-X_2-X_3-X_4$$

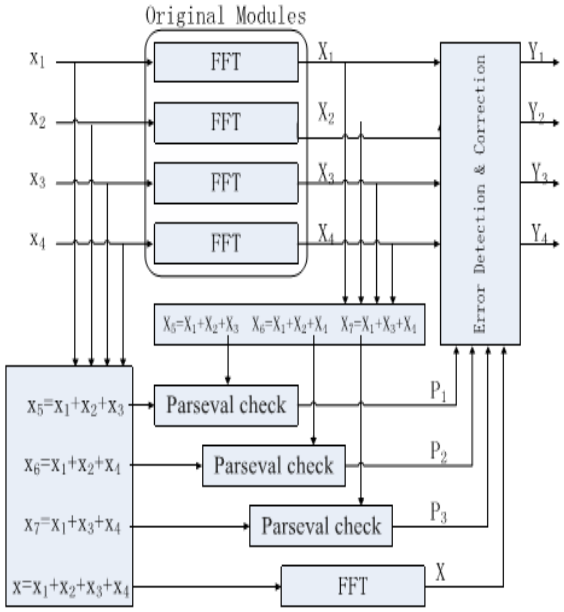

Fig. 3. Parity-SOS-ECC (second technique) fault-tolerant parallel FFTs.

Another possibility to combine the SOS check and the ECC approach is instead of using an SOS check per FFT, use an ECC for the SOS checks. Then as in the parity-SOS scheme, an additional parity FFT is used to correct the errors. This second technique is shown in Fig. 3. The main benefit over the first parity SOS scheme is to reduce the number of SOS checks needed. The error location process is the same as for the ECC scheme in Fig. 1 and correction is as in the parity-SOS scheme. In the following, this scheme will be referred to as parity-SOS-ECC (or second proposed technique).

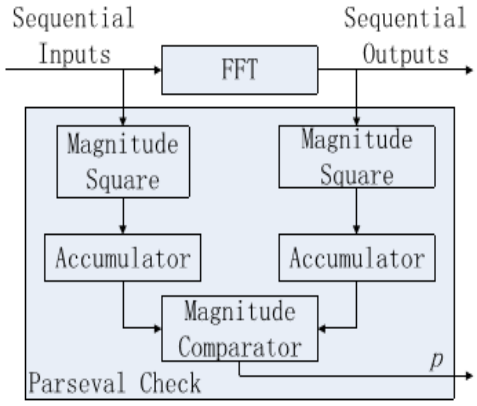

Fig. 4. Implementation of the SOS check

V. Vedic Sutra – Urdhwa Tiryakbhyam

In proposed system we tend to area unit measurement Input Adder Unit, currently it is replaced by

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sacred text multiplier factor. By doing this we are able to get less power consumption, high accuracy and reduced delay.

The sixteen sacred text Sutras apply to and canopy nearly each branch of arithmetic. They apply even to advanced issues involving an oversized variety of mathematical operations. Among these sutras, Urdhwa Tiryakbhyam Sanskrit literature is that the best for acting multiplication. The use of this Sanskrit literature will be extended to binary multiplication as well.This Sanskrit literature interprets to "Vertical and crosswise". It utilizes solely logical AND operation, 0.5 adders and full adders to perform multiplication wherever the partial merchandise area unit generated before actual multiplication. this protects a substantial quantity of time interval. What is more it's a sturdy methodology of multiplication. Consider 2 8-bit numbers, a (a8-a1) and b (b8-b1) wherever one to eight represents bits from the least important bit to the most important bit. the ultimate Product is represented by P (P16-P1). In Fig.5, the step by step methodology of multiplication of 2 8-bit numbers using Urdhwa Tiryakbhyam sutra is illustrated. The bits of the number and number area unit diagrammatic by dots and also the 2 approach are represents the logical AND operation between the bits that provides the partial product terms. In the typical style of Urdhwa Tiryakbhyam sutra based mostly number, solely full-adders and half-adders area unit used for addition of the partial products. But, the aptitude of full-adder is restricted to addition of solely three bits at a time.

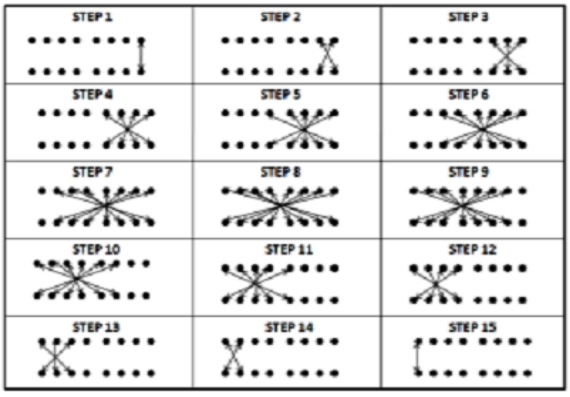


Fig.5. 8-bit binary multiplication using Urdhwa Tiryakbhyam Sutra

So, a large number of stages are required to get the final product. Higher order compressors discussed in next section can be employed to add more than 3 bits at a time (upto 7 bits) and hence can reduce the intermediate stages.

VI. RESULTS

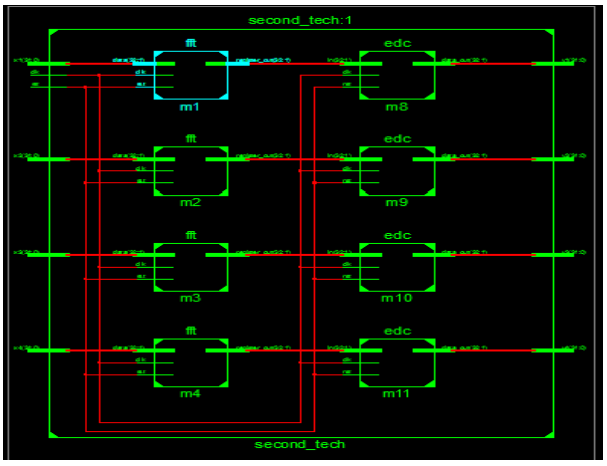
The written Verilog HDL Modules have successfully simulated and verified using synthesized using Xilinx ISE 13.2.

Proposed Result.

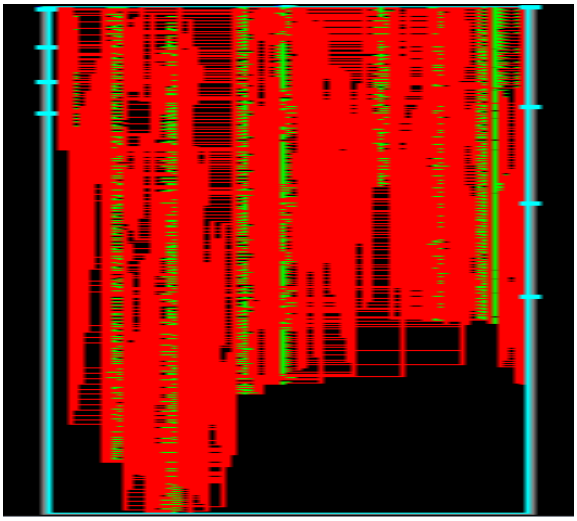
Simulation:

Synthesis Results:

RTL Schematic:



Technology Schematic:



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Design Summary:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	266	4656	5%
Number of Slice Flip Flops	228	9312	2%
Number of 4 input LUTs	429	9312	4%
Number of bonded IOBs	254	232	109%
Number of GCLKs	1	24	4%

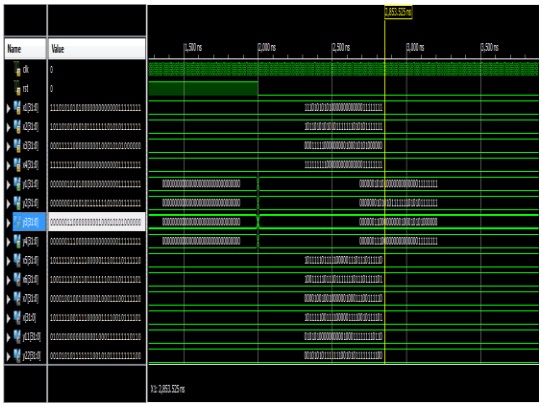
Timing Report:

```
Offset:             4.040ns (Levels of Logic = 1)
  Source:           m8/data_26 (FF)
  Destination:      y1<25> (PAD)
  Source Clock:     clk rising

  Data Path: m8/data_26 to y1<25>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              1   0.514   0.357  m8/data_26 (m8/data_26)
     OBUF:I->O                 3.169          y1_25_OBUF (y1<25>)
    ----------------------------------------
    Total                      4.040ns (3.683ns logic, 0.357ns route)
                                       (91.2% logic, 8.8% route)
```

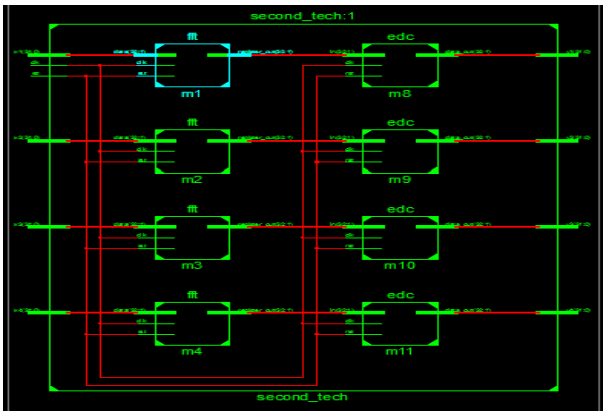
Extension Result:

Simulation:

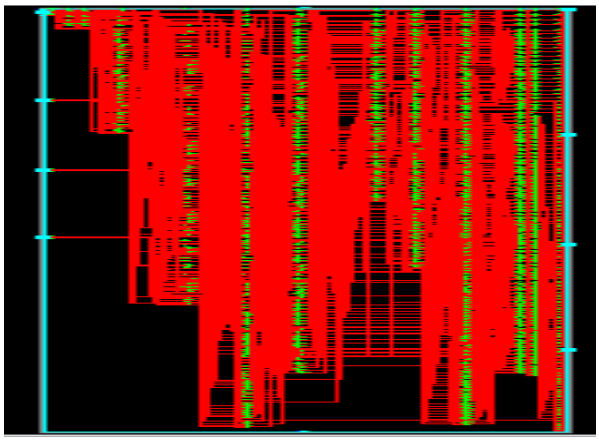


Synthesis Results:

RTL Schematic:



Technology Schematic:



Design Summary:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	225	4656	4%
Number of Slice Flip Flops	229	9312	2%
Number of 4 input LUTs	421	9312	4%
Number of bonded IOBs	234	232	100%
Number of GCLKs	1	24	4%

Timing Report:

```
Offset:             4.040ns (Levels of Logic = 1)
  Source:           m8/data_26 (FF)
  Destination:      y1<25> (PAD)
  Source Clock:     clk rising

  Data Path: m8/data_26 to y1<25>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              1   0.514   0.357  m8/data_26 (m8/data_26)
     OBUF:I->O                 3.169          y1_25_OBUF (y1<25>)
    ----------------------------------------
    Total                      4.040ns (3.683ns logic, 0.357ns route)
                                       (91.2% logic, 8.8% route)
```

VII. CONCLUSIONS

Detecting and correcting errors like important reliability are troublesome in signal process that will increase the utilization of fault tolerant implementation. In modern signal process circuits, it's common to search out many filters in operation in parallel. Proposed is a part economical technique to discover and correct single errors. The Parseval or sum of square check is the most widely known. It is most common to find several blocks operating in parallel in the modern communication systems. Recently, a method that exploits this truth to implement fault tolerance

on parallel filters has been projected. During this temporary, this system is 1st applied to guard FFTs. Then, 2 improved protection schemes that mix the utilization of error correction codes and Parseval checks are projected and evaluated. This project outspread with FFT using Vedic multiplier. For the further improvement of the multiplier efficiency ,we use Vedic multiplier i.e., Urdhwa Tiryakbhyam Sutra. By using this ,we can improve the functionality of the magnitude square block in the parseval check.

Future Scope: In Future, utilization of DCT instead of FFT will be carried out. Since SOS-ECC technique can detect and correct only single bit fault, this will be extended to multi bit faults by using the trellis code and hence area will be further reduced.

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