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Frequency Adaptive Repetitive Control of Grid Connected Inverter for Wind Power Generation Systems

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Abstract: *This paper is concerned with the current control of grid connected inverters based on a simple frequency adaptive repetitive controller. The main objective of VSPT is to obtain an integer number of samples per grid period. Which solves the main problem of RC, i.e., the loss of rejection to periodic disturbance due to grid frequency is adjusted with a variable sampling period filter phase-locked loop, which also adds robustness to the system due to its inherent tolerance to grid voltage distortion and un balances, and events such as frequency steps and faults. The control and synchronism subsystems are described, designed, and verified experimentally in a obtained prove the accuracy of the proposed control even under servant disturbances, typically in grids with high WPGS penetration, providing ancillary functions to enhance reliability and reduce operational cost.*

Keywords: Grid-Tie Current-Controlled Three-Phase Inverters; Power Quality; Repetitive Control;

I. INTRODUCTION

WIND power generation systems (WPGS) play a key role in the distributed power generation scenario worldwide [1]. Modern variable-speed WPGS square measure connected to the grid through a current-controlled three-phase voltage source inverter (CC-VSI), as shown in Fig. 1. Phase currents injected to the grid must abide by with strict power quality standards, such as, which demand a total harmonic distortion (THD) of the injected currents below 5%. Given the increasing penetration of WPGS, even more strict limits square measure expected to be needed in the close to future. Moreover, new grid codes are requiring further options. Known as adjunct functions, they enhance robustness, safety, and reliability of the grid through reactive power injection, fault ride-through capabilities, compensation of harmonic currents generated by nearby nonlinear hundreds, and mitigation of asymmetrical loads, among others. A key part of a WPGS is that the CC-VSI current management and synchronism subsystems, which square measure entirely accountable for meeting all the aforementioned needs. This is a complex task considering the multiple disturbance sources affecting the system [1]. In addition to grid voltage fluctuations, unbalances and harmonics, inverter nonlinearities (e.g., dead times, voltage drops of semiconductor switches, inductance variations, etc.) are major causes of current distortion.

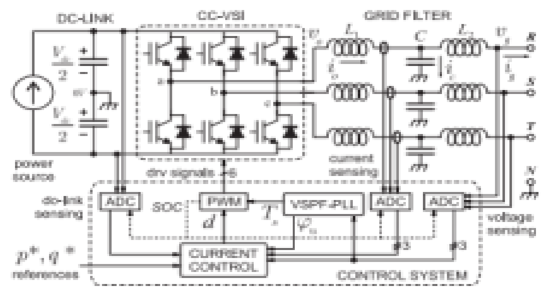

Fig. 1. Block diagram of the proposed control system within a CC-VSI for WPGS application.

The power source represents the energy supplied by the wind generator. This control adds are sonant pole in the open-loop transfer function at the grid fundamental frequency, fg, ensuring zero steady-state error at such frequency; grid phase/frequency information is implicit in the abc-dq transformation. However, inverter non linearities and unbalanced/distorted grid voltages generate errors not only at basic, but conjointly at harmonic frequencies of the grid. The limited open-loop information measure obtained with PI controllers results in low disturbance rejection capability and, hence, distorted line currents. A different methodology is to boost the steady state performance of a classic current controller (proportional (P), dead-beat predictive (DBP), state feedback (SFB), etc.) by attaching a repetitive controller. Repetitive control (RC), which is based on the inner model principle has been employed in uninterrupted power provides active power filters power factor correction converters and the output active/reactive power of distributed power generation systems .In the plug-in scheme, the classic controller closes an inner loop providing fast response to grid disturbances and reference changes, while the RC ensures zero steady-state error by placing resonant poles at fundamental and each harmonic frequency of the grid up to the Nyquist frequency. This paper proposes a different solution, which consists in changing fs adaptively thus fs = N fg, where N is a fixed whole {number |number} number [2].

II. CONTROL STRUCTURE AND PRINCIPLES

The WPGS control system can be observed, where the VSPF-PLL output governs the sampling/switching period value, $Ts = 1/fs$, which feeds the pulse width modulator (PWM). This in turn generates the start-of-conversion signal. For the analog-to-digital converters (ADCs). Thus, the whole system operates with a frequency *fs* that is an exact multiple of *fg*, $fs = N\,fg$. During normal operation, grid frequency drifts are small (e.g., ≤2%), so *fs* keeps close to its nominal value. As a consequence, the variation over time in the spectral content due to *fs* is negligible, hence switching losses are approximately the same and the grid filter design can be left unchanged. *A. Current Control.* A block diagram of the control structure adopted. Due to the VSPT, the sampling time *Ts* follows the grid period *Tg*, which changes slowly. This small and slow drift allows to treat the variable-time discrete system. as a fixed-time one with negligible error. A further discussion and stability analysis due to the variable sampling frequency is performed in Section IV-E. *P(z)* is the plant transfer function comprised by the modulator, the inverter, the LCL filter, and the grid. Signal *ig* is the current injected into the grid, *io* is the inverter output current, and *ic* is the capacitor current. Notice from Fig. 1 that $ig = io - ic$. , *id* is the reference (desired) current. Since only *io* is measured, *ig* will only follow *id* if *ic* is effectively compensated by the feedforward term *ic,* which is added to *id* . The exogenous signal *i p* represents the multiple disturbances affecting the output current: grid voltages not completely canceled by feedforward techniques, and inverter nonlinearities such as dead times [8], among others. Spectral components of *i p* are assumed to be at fundamental and harmonic multiples of the grid frequency. *C(z)* is a current regulator closing an inner loop to provide fast response to transients, typically within a few milliseconds. Classic control strategies, such as proportional, DBP or SFB controllers are typically employed. From Fig. 2, the resulting inner closed-loop transfer function is

$$H(z) = Io(z)$$

$$Id\,(z) = C(z)P(z)\;1 + C(z)P(z)$$

A plug-in repetitive controller *R(z)* can be attached to *C(z)* in a cascaded structure, as in Fig. 2, to improve the control loop disturbance rejection. According to the internal model principle [32], *R(z)* must add poles to the open-loop transfer function at dc ($z = 1$), fundamental, and harmonic frequencies of the grid to ensure that *i p* is completely rejected in steady state.

A. Pulse width modulation (PWM)

Pulse Width Modulation (PWM) is the most effective means to achieve constant voltage battery charging by switching the solar system controller's power devices. When in PWM regulation, the current from the solar array tapers according to the battery's condition and recharging needs consider a waveform such as this: it is a voltage switching between 0v and 12v.

It is fairly obvious that, since the voltage is at 12v for exactly as long as it is at 0v, then a 'suitable device' connected to its output will see the average voltage and think it is being fed 6v - exactly half of 12v. So by varying the width of the positive pulse - we can vary the 'average' voltage. The PWM is a large amplitude digital signal that swings from one voltage extreme to the other. And, this wide voltage swing takes a lot of filtering to smooth out. When the PWM frequency is close to the frequency of the waveform that you are generating, then any PWM filter will also smooth out your generated waveform and drastically reduce its amplitude. So, a good rule of thumb is to keep the PWM frequency much higher than the frequency of any waveform you generate.

Finally, filtering pulses is not just about the pulse frequency but about the duty cycle and how much energy is in the pulse. The same filter will do better on a low or high duty cycle pulse compared to a 50% duty cycle pulse. Because the wider pulse has more time to integrate to a stable filter voltage and the smaller pulse has less time to disturb it the inspiration was a request to control the speed of a large positive displacement fuel pump. The pump was sized to allow full power of a boosted engine in excess of 600 Hp.

At idle or highway cruise, this same engine needs far less fuel yet the pump still normally supplies the same amount of fuel. As a result the fuel gets recycled back to the fuel tank, unnecessarily heating the fuel. This PWM controller circuit is intended to run the pump at a low speed setting during low power and allow full pump speed when needed at high engine power levels.

B. PWM controller features

This controller offers a basic "Hi Speed" and "Low Speed" setting and has the option to use a "Progressive" increase between Low and Hi speed. Low Speed is set with a trim pot inside the controller box. Normally when installing the controller, this speed will be set depending on the minimum speed/load needed for the motor. Normally the controller keeps the motor at this Lo Speed except when Progressive is used and when Hi Speed is commanded (see below). Low Speed can vary anywhere from 0% PWM to 100%.

Progressive control is commanded by a 0-5 volt input signal. This starts to increase PWM% from the low speed setting as the 0-5 volt signal climbs. This signal can be generated from a throttle position sensor, a Mass Air Flow sensor, a Manifold Absolute Pressure sensor or any other way the user wants to create a 0-5 volt signal. This function could be set to increase fuel pump power as turbo boost starts to climb (MAP sensor). Or, if controlling a water injection pump, Low Speed could be set at zero PWM% and as the TPS signal climbs it could increase PWM%, effectively increasing water flow to the engine as engine load increases. This controller could even be used as a secondary injector driver (several injectors could be driven in a batch mode, hi impedance only), with Progressive control (0-100%) you could control their output for fuel or water with the 0-5 volt signal. Progressive control adds enormous flexibility to the use of this controller. Hi Speed is that same as hard wiring the motor to a steady 12 volt DC source. The controller is providing 100% PWM, steady 12 volt DC power. Hi Speed is selected three different ways on this controller:

1) Hi Speed is automatically selected for about one second when power goes on. This gives the motor full torque at the start. If needed this time can be increased (the value of C1 would need to be increased).

2) High Speed can also be selected by applying 12 volts to the High Speed signal wire. This gives Hi Speed regardless of the Progressive signal.

When the Progressive signal gets to approximately 4.5 volts, the circuit achieves 100% PWM – Hi Speed.

III. VOLTAGE SOURCE INVERTER (VSI)

A voltage-source converter is a power electronic device that connected in shunt or parallel to the system. It can generate a sinusoidal voltage with any required magnitude, frequency and phase angle. The VSI used to either completely replace the voltage or to inject the "missing voltage". The "missing voltage" is the difference between the nominal voltage and the actual. It also converts the DC voltage across storage devices into a set of three phase AC output voltages

A. Full-Bridge VSI:

The power topology of a full-bridge VSI. This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. As expected, both switches S1 and S1ÿ (or S2. and S2ÿ) cannot be on simultaneously because a short circuit across the dc link voltage source vi would be produced. There are four defined and one undefined. The undefined condition should be avoided so as to be always capable of defining the ac output voltage. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant. It can be observed that the ac output voltage can take values up to the dc link value vi , which is twice that obtained with half-bridge VSI topologies. Several modulating techniques have been developed that are

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applicable to full-bridge VSIs. Among them are the PWM (bipolar and unipolar) techniques.

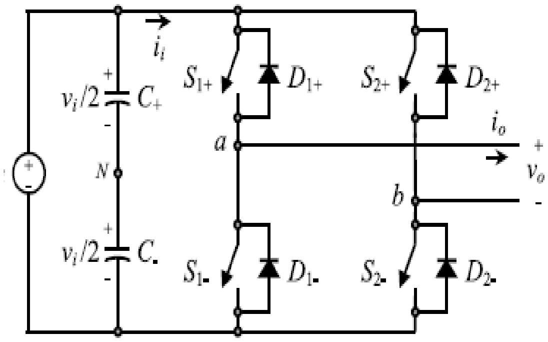

Fig. 2

IV. CONTROLLING STATAGIES

A. Current Control

A block diagram of the control structure adopted is shown in Fig.2. Due to the VSPT, the sampling time *Ts* follows the grid period *Tg*, which changes slowly. This small and slow drift allows treating the variable-time discrete system as a fixed-time one with negligible error. A further discussion and stability analysis due to the variable sampling frequency is performed in Section IV-E. *P(z)* is the plant transfer function comprised by the modulator, the inverter, the LCL filter, and the grid. Signal *ig* is the current injected into the grid, *io* is the inverter output Current, and *ic* is the capacitor current. Notice from Fig.1 that *ig* = *io* − *ic*. In Fig. 2, *id* is the reference (desired) current. Since only *io* is measured, *ig* will only follow *id* if *ic* is effectively compensated by the feed forward term *ic* , which is added to *id* . The exogenous signal *ip* represents the multiple disturbances affecting the output current: grid voltages not completely canceled by feedforward techniques, and inverter nonlinearities such as dead times [8], among others. Spectral components of *i p* are assumed to be at fundamental and harmonic multiples of the grid frequency. *C(z)* is a current regulator closing an inner loop to provide fast response to transients, typically within a few milliseconds. Classic control strategies, such as proportional, DBP or SFB controllers are typically employed the resulting inner closed-loop transfer function is

H(z) = Io(z) Id (z) / C(z)P(z) 1 + *C(z)P(z)*

B. Comparison with Other RC Approaches

An important drawback of RC is its gain loss when the grid frequency varies, which, in turn, reduces the control Loop disturbance rejection and reference tracking capability [20]. This occurs because the order *N* of the RC is not equal to the ratio *Tg/Ts* , and hence the RC poles no longer lie at multiples of *fg*. Several approaches have been proposed in the literature to deal with this issue, the most common being the introduction of a fictitious sampler operator [26]. A recent and more sophisticated approach uses an FIR filter with variable coefficients within the RC algorithm to emulate the fractional delay produced by the frequency drift [7]. A similar approach is found in [8], which employs a simple first-order low-pass filter, cascaded with the RC delay line, with adjustable cutout Frequency. This is much simpler than the FIR filter in [7], hence the computational cost is reduced at the expense of a degraded performance. In both cases, the filter coefficients must be accurately updated online to avoid Additional loss of performance; the proposed RC does not require any parameter update. In addition, both [7] and [8] suffer from coefficient quantization errors. In the proposed strategy, the VSPT allows the use of the simple RC algorithm (3) consisting of a delay and simple filters in *Q(z)* and *L(z)* (which are presented in detail, where the aforementioned numerical errors are nonexistent since all the coefficients are one or powers of two. The gain of several RC algorithms, operating with fixed *Ts* = 100μs and for a grid frequency of 49.38 Hz, a 1% variation from the nominal value of 50 Hz. The static RC, described by (2) and using a fixed order *N* = 200, exhibits the worst performance under grid frequency changes. The adaptive RC reduces the gain loss by setting online the order *N* to the nearest integer of the estimated signal period. The adaptive RC with linear interpolation further reduces the gain loss, for which a precise estimation of the grid frequency is required to update the algorithm coefficients. In all the cases described, notice the significant reduction in the RC gain, which may lead to high Distortion in the output currents. For high-order harmonics, the RC could even amplify disturbances (negative gain in decibels), which is the case for the static.

B. Variable Sampling Period Filter Phase-Locked Loop

The three-phase VSPF-PLL operates with a variable sampling period technique. As shown in Fig.3, the PLL receives the sampled three-phase voltages, which are transformed to the SRF, and the q component is used as an estimate of the phase error. A sliding-window filter (SWF) is applied to reject signals different from the fundamental positive sequence. This feature provides robustness to the VSPF-PLL against grid voltage distortions, unbalances, and faults. After the SWF, a lead-lag compensator with integral action is used to obtain a stable closed loop with zero SteadyState error. The output of this compensator is the value of Ts , which is updated in the PWM for the next period. A reference phase, ϕu, is internally generated by adding a phase step equal to $2\pi/N$ on each new sampling period. ϕu is employed to transform the sampled voltage to the SRF, so the loop will increase or reduce Ts to match ϕu to the actual positive sequence phase. ϕu is also sent to the control block to generate the current reference signals. The VSPF-PLL mathematical model, together with the design of the lead-lag compensator and the SWF, is described in detail. The VSPF-PLL distinctive component is the SWF, whose transfer function is

$$G\text{SWF}(z) = \frac{1 - z^{-N\text{SWF}}}{1 - z^{-1}} \quad (8)$$

which shares some properties with the RC, clearly visible by comparing it with (2). While (2) places N poles equally spaced along the unitary circle, (8) places NSWF zeros in the same places. Parameter NSWF is chosen as N or $N/2$ whether even harmonic components are significant or not in the grid voltages. If they are not, NSWF = $N/2$ can be used, reducing memory positions by half.

IV. MAT LAB AND SIMULATION

The simulations have been carried out using Matlab/Simulink. The grid is concerned to have a THD of 6.57% with the harmonic components.

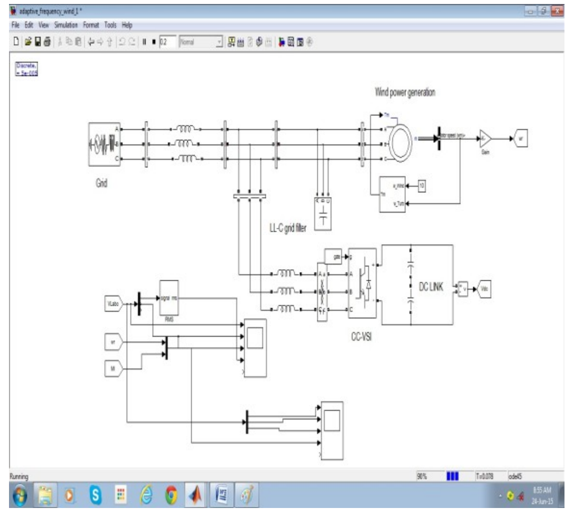

Fig.3 Without fault

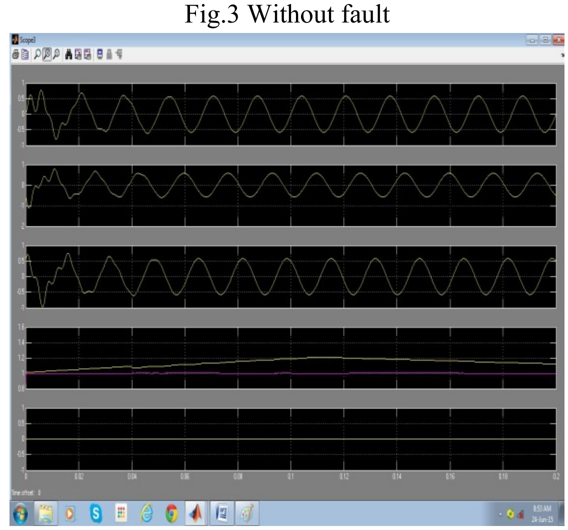

Fig.4 With fault

Comparative results of the transient response employing the proposed control combined with both a standard SRF-PLL and the VSPF-PLL under severe grid disturbances and faults. (a) Grid voltages. (b) Currents with SRF-PLL. (c) Currents with VSPF-PLL. (d) SRF-PLL output. (e) VSPF-PLL output.

V. CONCLUSION

An RC for WPGS was presented, which achieves optimal performance in steady-state conditions due to a VSPT. With this new control strategy, the loss of rejection due to

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grid frequency drift is corrected, as proven by the Experimental results. The sampling/switching frequency is slightly adjusted around 10 kHz with a VSPF-PLL, which also adds robustness to the system due to its inherent tolerance to grid voltage distortion and unbalances, and events like frequency steps and grid faults. Since grid frequency drift is usually small during inverter operation, switching losses and LCL filter design remained unaffected by the variable frequency.

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BIODATA

T.Swetha currently working as Assistant Professor, Department of EEE, in Kakatiya Institute of Technology and Science, Warangal. My areas of interest are Converters, Distribution Generation, Micro Grids and Power Quality.