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# Design A 8 Bit Fault Tolerant Parallel FFT's Using Parseval Checks

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**ABSTRACT:** *Presently, the circuits of communication and signal processing became more difficult. This is due to the CMOS technology scaling in which more transistors is integrated on a single device. The transistors which are operated with low voltages are known as scaling. These are more liable to the errors caused by the noise and manufacturing variations. Errors cause the reliability risk for advanced electronic circuits. Algorithm Based Fault Tolerance (ABFT) technique is used to utilize the algorithmic properties. FFTs are the major key building blocks in every system. Perseval or sum of square check is one of the techniques which are most extensively used. A technique has been proposed which utilizes this reality to implement fault tolerance on parallel filters. Initially, this technique is applied to secure the FFTs. Therefore, two protection schemes are proposed and evaluated which unify the usage of Error Correction Codes (ECC) and Parceval checks.*
*Index terms: Error Correction Codes (ECC), Fast Fourier Transforms (FFTs), Soft Errors.*

## I.INTRODUCTION

Error Correction Codes (ECC) techniques have been mostly utilized to correct the errors and to improve the reliability of memories. ECC contains data bits and additional check bits. Since, they are typically from the linear block codes. Data bits are written in data bit array and check bits are produced by using the data bits which are stored in check bit arrays. This operation is performed during write operation of memories. The check bits always should be tested for same fault models.

FFTs converting the signal from time domain to frequency domain. Error coding is one of the methods for detecting and correcting the errors to verify information.

The FFTs can maximize the possibility of applying error correction codes which are in parallel. Let us assuming that there can only be a single error on the system in the case of radiation-induced soft errors and may be two in worst case. On the basis of the Partial Summation with parity FFT the modern technique is implemented for multiple error corrections.

Hence, these parallel filters or FFTs generates an opportunity for implementing the ABFT technique.

## II.LITERATURE SURVEY

A modern technique called Parseval's method is used for detecting the errors in multiple FFT. This is attained by Sum of Squares (SOSs) check which is based on Parseval's theorem. If the FFT have no error then its Sum of Squares of the input must be equal with the Sum of Squares of its frequency domain output. This correlation is used to identify the errors with minimum overhead. The Parseval's check can be combined with the error correction codes for minimizing the area overhead for parallel FFTs.

Multiple error detection and correction can be attained through this combination. The easy way is to generate the redundant input for single

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FFT with all the four FFT inputs. The errors can be reduced when the parity FFT output is XORed with fault free outputs of the FFTs. These techniques can reduce the total number of Sum of Squares which is used. The parity SOS fault tolerance parallel FFT is shown in below figure.

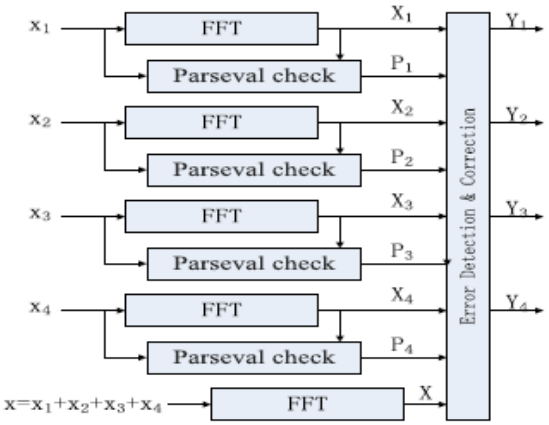


**FIG 1.PARITY SOS FAULT TOLERANT PARALLEL FFTS.**

This relationship can be used for detecting the errors for each input or output sample. SOS check is combined with the ECC for reducing the security for the parallel FFTs. Hence SOS check only detects the errors and ECC should implement the correction. This can be achieved by using a single parity bit for all FFTs. The combination of these two techniques can be used for reducing the number of additional FFTs. This method will be referred as parity-SOS.

In Parity-SOS scheme an additional parity FFT is utilized for correcting the errors. This technique is shown in above fig 2. This method is introduced as parity-SOS-ECC technique. Hence, final observation is that ECC scheme can detect all the errors which exceed a threshold and SOS can detect most errors.

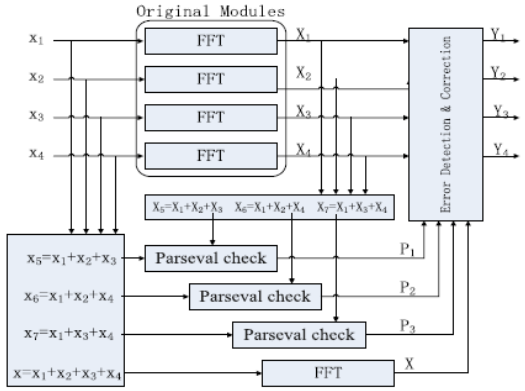


**FIG 2. PARITY SOS-ECC FAULT TOLERANT PARALLEL FFTS.**

Therefore, fault injection experiments to be done for determining the percentage of errors which are actually corrected.

## III.PROPOSED SYSTEM

Now-a-days, a modern scheme is obtained on the basis of the Error Correction Codes (ECC). Each filter in this technique can be equivalent of a bit. Parity check bits can be evaluated by using addition. The operation of this technique is the output of the sum of the several inputs is the sum of the individual outputs. So, this is valid for any linear operation.

It is supposed that there is only a double error on the system at any given point in time. There are three main contributions. They are:

1) The parallel FFTs are protected by the Error Correction Code. It exhibits its effectiveness in terms of overhead and protection effectiveness.
2) A new technique is presented in which we can use the Parseval or sum of squares (SOSs) checks combined with parity FFT.
3) It is the modern technique in which the ECC is used on the SOS checks instead of the FFTs.

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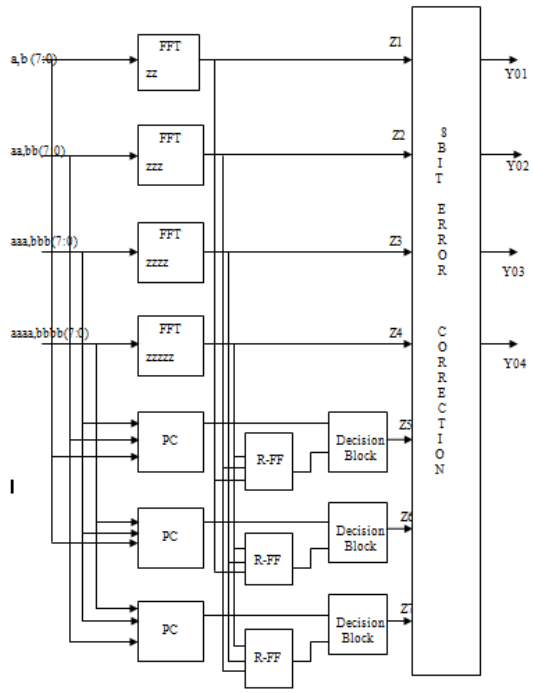


**FIG 3. PARALLEL FFT PROTECTION USING ECCS.**

This scheme is evaluated by using FPGA implementations to estimate the protection overhead. The protection overhead can be reduced by combining the use of ECCs and parseval checks.

## IV.RESULTS

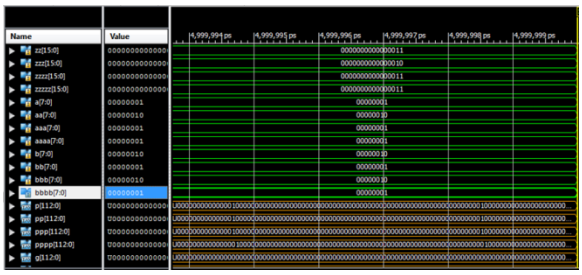

**FIG 4. INPUT WAVEFORM**

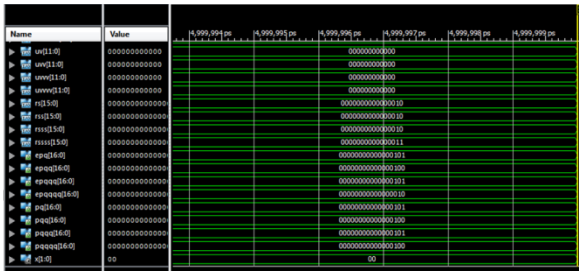

**FIG 5. OUTPUT WAVEFORM**

## V.CONCLUSION

Detecting and correcting errors such as critical reliability are difficult in signal processing which increases the use of fault tolerant implementation. Recently, it is common to signal processing circuits for finding the several filters operating in parallel. Proposed is an area efficient technique to detect and correct single errors. The approach is on the basis of applying SOS-ECC check to the parallel FFT outputs to detect and correct errors. A simple parity FFT is used for correction. The 8 point FFT with the input bit length 32 is protected using the proposed technique. This technique can detect and correct only single bit error and it reduces area results in high speed compared to existing techniques.

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