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Design of an Improved Star Configuration Based Statcom with H – Bridge Concept

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Abstract: *The main aim of this paper is to design a STATCOM which has the capability of compensating the fault and to overcome the conduction losses faced by the conventional STATCOM with traditional H-Bridge structure the future control procedures bestow themselves not only to the current loop control but also to the DC capacitor voltage control. With concerns to the current loop control, a nonlinear controller established on the passivity-based control (PBC) theory is used in this cascaded STATCOM. The capacitor voltage control, overall voltage control will control by embracing a proportional resonant controller. Clustered balancing mechanism will achieve by shifting the modulation wave vertically which can be easily executable in a field-programmable gate array. An artificial fault will be injected for a limited time period duration. Real and reactive power will be maintained for the compensated voltage and current. This work carried by using MATLAB /SIMULINK simulation tool.*

1 INTRODUCTION

Now-a-days use of Flexible ac transmission systems (FACTS) devices have been increasing rapidly in power systems due to their power quality control, power transfer capacity of AC system interconnections. Shunt FACTS devices are utilized at point of common connection (PCC) to absorb or inject the reactive power into the power system. Due to this the voltage quality of PCC is improved. Out of all shunt devices static synchronous compensator is preferred most due to its robust construction, wide range of voltage control, dynamic reactive current compensation and less response time. In recent years, many topologies have been applied to the STATCOM. Among these different types of topologies, H–Bridge Cascaded STATCOM is widely accepted for high power applications due to the following advantages:

- Quick response speed
- Small volume
- High efficiency
- Minimal interaction with the supply grid
- Individual phase control ability

2 CONFIGURATION OF STATCOM SYSTEM

The adjacent figure Fig. 4.1 shows the circuit of the star-configured STATCOM cascading 12 H-bridge pulse width modulation (PWM) converters in each phase and it can be expanded easily by adding more number of bridges or by removing the bridges according to the requirement. By controlling the current of STATCOM directly, it can absorb or provide the required reactive current to achieve the purpose of dynamic reactive current compensation. Finally, the power quality of the grid is improved and the grid offers the active current only.

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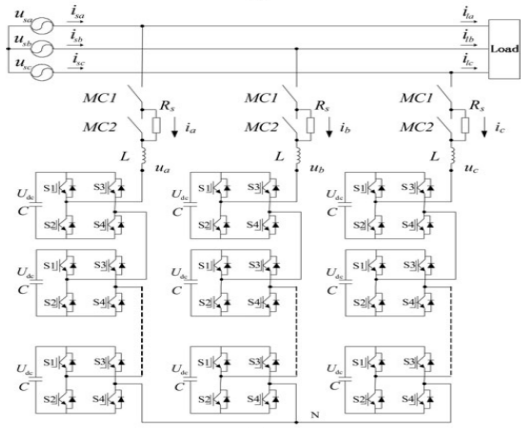

(a)

Fig. 1 Actual 10 KV 2 MVA H-bridge cascaded STATCOM. (a) Configuration of the system.

The power switching devices working in ideal condition is assumed. u_{sa}, u_{sb} and u_{sc} are the three-phase voltage of grid. u_a, u_b, and u_c are the three-phase voltage of STATCOM. i_{sa}, i_{sb}, and i_{sc} are the three-phase current of grid. i_a, i_b and i_c are the three-phase current of STATCOM. i_{la}, i_{lb} and i_{lc} are the three-phase current of load. u_{dc} is the reference voltage of dc capacitor. C is the dc capacitor. L is the inductor. R_s is the starting resistor.

Table 4.1 summarizes the circuit parameters. The cascade number of $N = 12$ is assigned to H-bridge cascaded STATCOM, resulting in 36 H-bridge cells in total. Every cell is equipped with nine isolated electrolytic capacitors which the capacitance is 5600 μF. The dc side has no external circuit and no power source except for the dc capacitor and the voltage sensor. In each cluster, an ac inductor supports the difference between the sinusoidal voltage of the grid and the ac PWM voltage of STATCOM. The ac inductor also plays an important role in filtering out switch ripples caused by PWM. For selecting insulated-gate bipolar transistor (IGBT), considering the complexities of practical industrial fields, there might be the problems of the spike current and over load. Consequently, in order to ensure the stability and reliability of H-bridge cascaded STATCOM, and also improve the over load capability, the current rating of the selected IGBT should be reserved enough safety margin.

In the proposed system, 1.4 times rated current operation is guaranteed, the peak current under the 1.4 times over load condition is 224 A, the additional 76 A (30− 224 A = 76 A) is the safety margin of IGBT modules. Due to the previous considerations, the voltage and current ratings of IGBT which is selected as the switching element in main circuit are 1.7 kV and 300 A.

Grid voltage	u_s	10 kV
Rated reactive	Q	2 MVA
AC inductor	L	10 mH
Starting resistor	R_s	4 kΩ
DC capacitor capacitance	C	5600 μF
DC capacitor reference voltage	U_{dc}	800 V
Number of H-bridges	N	12
PWM carrier frequency	f	1 kHz

Table 1 Circuit Parameters of the simulation System

The modulation technology adopts the carrier phase-shifted sinusoidal PWM (abbreviated as CPS-SPWM) with the carrier frequency of 1 kHz. Then, with a cascade number of $N = 12$, the ac voltage cascaded results in a 25-level waveform in line to neutral and a 49-level waveform in line to line. In each cluster, 12 carrier signals with the same frequency as 1 kHz are phase shifted by $2\pi/12$ from each other. When a carrier frequency is as low as 1 kHz, using the method of phase-shifted unipolar sinusoidal PWM, it can make an equivalent carrier frequency as high as 24 kHz. The lower carrier frequency can also reduce the switching losses to each cell.

3.CONTROL SYSTEM for H-BRIDGE CASCADED STATCOM

A *system* is a group of elements or components connected in a sequence to perform a specified function.

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A *control system* is a system whose response can be controlled by varying the input to the system. The output quantity is called controlled variable or response and the input quantity is called command signal or excitation.

There are two types of control systems. They are Open loop control and Closed loop control systems. The open loop control system has no feedback and it completely depends upon the input signal which we provide for the system to operate. It has robust construction, easy to operate, easy to design and highly economical. But the only defect is that it cannot vary the input signal according to the external disturbances caused during the system operation. Because of this the desired response is deteriorated when there are external disturbances.

Whereas in closed loop control system a feedback is provided to the input and an error signal is generated. This error signal changes the input according to the disturbances that are caused during the system operation. The external disturbances are also taken into account and the output is varied. Due to this the system becomes complicated and also loses its robust nature. It is also more costly than the open loop system.

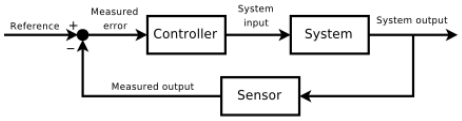

Fig. 3 A Closed Loop Control System

4 NON – LINEAR CONTROL SYSTEM

Nonlinear control theory is the area of control theory which deals with systems that are nonlinear, time-variant, or both. Control theory is a branch of engineering that is concerned with inputs, and how to modify the output by changing the input using feedback. The system to be controlled is called the "plant". In order to make the output of a system follow a desired reference signal, a controller is designed which compares the output of the plant to the desired output and provides feedback to the plant to modify the output and bring it closer to the desired output.

Linear control theory applies to systems made of linear devices; which means they obey the superposition principle; the output of the device is proportional to its input. Systems with this property are governed by linear differential equations. Nonlinear control theory covers a wider class of systems that do not obey the superposition principle. It applies to more real-world systems, because all real control systems are nonlinear. These systems are often governed by nonlinear differential equations.

An example of a nonlinear control system is a thermostat-controlled heating system. A building heating system such as a furnace has a nonlinear response to changes in temperature; it is either "on" or "off", it does not have the fine control in response to temperature differences that a proportional (linear) device would have. Therefore the furnace is off until the temperature falls below the "turn on" set point of the thermostat, when it turns on. Due to the heat added by the furnace, the temperature increases until it reaches the "turn off" set point of the thermostat, which turns the furnace off, and the cycle repeats. This cycling of the temperature about the desired temperature is called a *limit cycle*, and is characteristic of nonlinear control systems. There are specific properties of a Non – Linear Control System. They are:

- They do not obey the Superposition Principle.
- They do not exhibit linearity and homogeneity principles.
- They have multiple equilibrium points.
- Solution to Non – Linear systems may not exist for all times.

5 CONTROL BLOCKS OF H-BRIDGE CASCADED STATCOM

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Fig. 4.4 shows a block diagram of the control algorithm for H-bridge cascaded STATCOM. The whole control algorithm mainly consists of four parts, namely, PBC, overall voltage control, clustered balancing control, and individual balancing control. The first three parts are achieved in DSP, while the last part is achieved in the FPGA.

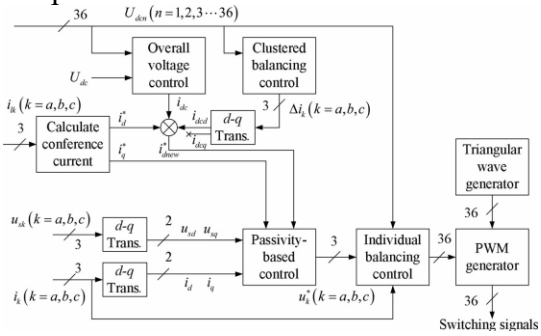

Fig. 4 Control block diagram for the 10 kV 2 MVA H-bridge cascaded STATCOM.

5.1 Overall Voltage Control

As the first-level control of the dc capacitor voltage balancing, the aim of the overall voltage control is to keep the dc mean voltage of all converter cells equaling to the dc capacitor reference voltage. The common approach is to adopt the conventional PI controller which is simple to implement. However, the output voltage and current of H-bridge cascaded STATCOM are the power frequency sinusoidal variables and the output power is the double power frequency sinusoidal variable, it will make the dc capacitor also has the double power frequency ripple voltage. So, the reference current which is obtained in the process of the overall voltage control is not a standard dc variable and it also has the double power frequency alternating component and it will reduce the quality of STATCOM output current.

In general, when using Proportional Integral (PI) controller, in order to ensure the stability and the dynamic performance of system, the bandwidth of voltage loop control is set to be 200–500 Hz and it is difficult to restrain the negative effect on the quality of STATCOM output current which is caused by the 100 Hz ripple voltage. Moreover, because of static error of PI controller, it will affect not only the first level control but also the second and the third one. Especially, during the startup process of STATCOM, it will make the voltage reach the target value with a much larger overshoot.

To resolve the problem, Proportional Resonant (PR) controller is adopted for the overall voltage control. The gain of the PR controller is infinite at the fundamental frequency and very small at the other frequency. Consequently, the system can achieve the zero steady-state error at the fundamental frequency. By setting the cutoff frequency and the resonant frequency of the PR controller appropriately, it can reduce the part of ripple voltage in total error, decrease the reference current distortion which is caused by ripple voltage, and improve the quality of STATCOM output current. Moreover, the dynamic performance and the dynamic response speed of the system also can be improved. In particular, during the startup process of STATCOM, the much larger dc voltage overshoot can be restrained effectively.

The PR controller is composed of a proportional regulator and a resonant regulator. Its transfer function or gain can be expressed as

$$G_{\mathrm{PR}}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}$$

where k_p is the proportional gain coefficient. k_r is the integral gain coefficient. ω_c is the cutoff frequency. ω_0 is the resonant frequency. k_r influences the gain of the controller but the bandwidth. With k_r increasing, the amplitude at the resonant frequency is also increased and it plays a role in the elimination of the steady-state error. ω_c influences the gain of the controller and the bandwidth. With ω_c

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Volume 04 Issue-17
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increasing, the gain and the bandwidth of the controller are both increased.

We select the values $k_p = 0.05$, $k_r = 10$, $\omega_c = 3.14$ rad/s, and $\omega_0 = 100\pi$ as the controller parameters. Fig. 4.5 shows the bode plots of the PR controller with the previous parameters and Fig. 4.6 shows the block diagram of overall voltage control. The signal of voltage error is obtained by comparing the dc mean voltage of all converter cells with the dc capacitor reference voltage. Then, the signal of voltage error is regulated by the PR controller and delivered to the current loop as a part of the reference current. U_{dc} is the dc capacitor reference voltage. U^*_{dc} is the mean value of overall voltage. i_{dc} is the active control current for overall voltage control.

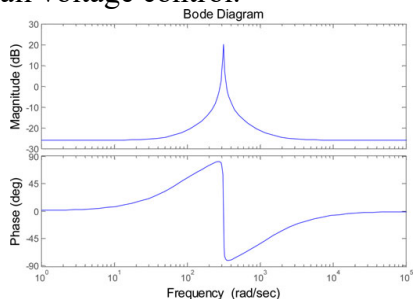

Fig. 5 Bode plots of the PR controller.

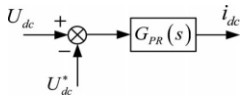

Fig. 6 Block diagram of overall voltage control.

5.2Clustered Balancing Control

Taking the clustered balancing control as the second level control of the dc capacitor voltage balancing, the purpose is to keep the dc mean voltage of 12 cascaded converter cells in each cluster equaling the dc mean voltage of the three clusters. ADRC is adopted to achieve it. Then, it requires several steps to complete the design of ADRC for H-bridge cascaded STATCOM, which are as follows.

H-bridge cascaded STATCOM is a first order system; thus, the first-order ADRC is designed. Taking the dc capacitor voltage of each cluster as the controlled object for analysis, the clustered balancing control model is built and the input and output variables and the controlled variable of the controlled object are determined.

By using the nonlinear tracking differentiator (TD) which is a component of ADRC, the transient process for the reference input of the controlled object is arranged and its differential signal is extracted. Selecting the mean value of overall voltage U^*_{dc} as the reference voltage, TD is obtained via linear differential element and it can be expressed as

$$\dot{v}_1 = -r_1 fal\left[(v_1 - U^*_{\mathrm{dc}}), \alpha_1, \delta_1\right]$$

Where v_1 is the tracking signal of reference voltage U^*_{dc} and $v^{\cdot}_1$ is the differential signal of the reference voltage U^*_{dc}. r_1 is the speed tracking factor which reflects the changing rule of TD. The larger the r_1, the faster the tracking speed and the larger the overshoot. Thus, it needs to select r_1 properly according to the requirement of the actual system. α_1 and δ_1 are the adjustable control parameters. α_1 determines the nonlinear form. The control effect will be changed greatly with the appropriate α_1 . δ_1 determines the size of the *fal* function linear range.

With the extended state observer (ESO) in ADRC, the uncertainties and the disturbances which lead to the unbalancing of the clustered dc capacitor voltages are observed and estimated dynamically.

The second-order ESO designed for the dc capacitor voltage of STATCOM could be written as

$$\begin{cases} \xi = z_1 - U_{kdc} \\ \dot{z}_1 = z_2 - r_{21} fal\left(\xi, \alpha_2, \delta_2\right) + b\Delta i_k \\ \dot{z}_2 = -r_{22} fal\left(\xi, \alpha_2, \delta_2\right) \end{cases}$$

where the *fal* function *fal* (ξ, α, δ) is defined as

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Volume 04 Issue-17
December 2017

$$fal(\xi,\alpha,\delta)=\begin{cases}|\xi|^{\alpha}\,sign(\xi) & (|\xi|>\delta)\\ \xi/\delta^{1-\alpha} & (|\xi|\le\delta).\end{cases}$$

U_{kdc} (k = a, b, c) is the real-time detected value of the dc mean voltage of 12 cascaded converter cells in each cluster in current cyclical and it is used as known parameter. z_1 is the state estimation signal of the dc capacitor voltage. ξ is the control deviation of the system. z_2 is the internal and the external disturbance estimate signals of the controlled object. Δi_k is the control variable. b is the feedback coefficient of Δi_k (k = a, b, c). r_{21}, r_{22}, α_2 , and δ_2 are the adjustable control parameters. r_{22} has an effect on the delay of z_2. The larger the r_{22}, the smaller the delay. But, the larger r_{22} will lead to system oscillation. With r_{21} increasing slightly, the system oscillation could be damped. However, it will result in system divergence. Consequently, the adjustment of r_{21} and r_{22} requires mutual coordination. It can set r_{22} beforehand and then improve the control effect with increasing r_{21} gradually.

Actually, there are errors in the detection unit of the dc capacitor voltage of STATCOM. Thus, control precision of the dc capacitor voltage can be improved considerably by using z_1 to estimate the state of the actual dc capacitor voltage precisely. For the changing of the system operation parameters in different applied environments, z_2 can estimate the unknown disturbances accurately and optimize the dynamic response speed of the clustered balancing control. Whether the unknown disturbances can be estimated accurately with ESO directly influences the control effect of ADRC. Therefore, the tuning of ESO parameters is very critical.

Nonlinear state error feedback (NLSEF) unit, a very important part of ADRC, is used to calculate the control variable of the active power adjustment for the clustered balancing control. However, in the practical application, the selection of NLSEF unit parameters in common ADRC is very difficult. Therefore, it is simplified with the linear optimization method in this paper and the newly obtained NLSEF unit can be expressed as

$$\begin{cases}\xi_1 = z_1 - v_1\\ i_0 = r_3\, fal\,(\xi_1,\alpha_3,\delta_3)\\ \Delta i_k = i_0 - z_2/b\end{cases}$$

where *fal* function is defined above. ξ_1 is the error value between the tracking signal v_1 and the state estimation signal z_1 . i_0 is the control variable without the disturbance feedback compensation. b is the feedback coefficient which has relations with the control variable Δi_k and the state variable of the ESO. If the controlled object existed delay, with a larger b, it would generate a large error control signal making the response speed of the output faster and compensation of the internal and the external disturbances more effective. r_3, α_3, and δ_3 are the adjustable control parameters. The regulating speed can be controlled by appropriately adjusting r_3. However, the faster regulating speed might cause increased overshoot and system oscillation.

Finally, by combining NLSEF unit with the observed disturbances from ESO, the simplified ADRC can be achieved and then the clustered balancing control of H-bridge cascaded STATCOM can be realized. Fig. 4.7 shows a block diagram of the clustered balancing control with the simplified ADRC. When ADRC receives the reference voltage U^*_{dc} and the real-

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p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

time detected value of the dc mean voltage U_{kdc} (k = a, b, c) of 12 cascaded converter cells in each cluster, it will trace the reference voltage rapidly with TD and obtain the tracking signal v_1 by filtering. Then, by subtracting the tracking signal v_1 from the state estimation signal of the dc capacitor voltage z_1, the control deviation command ξ_1 of the system voltage is calculated. ξ_1 is used as the input signal of NLSEF. Finally, the active adjustment control current Δi_k (k = a, b, c) of the clustered balancing control is achieved by subtracting the disturbance estimate signals which obtained in ESO from the output result i_0 of NLSEF.

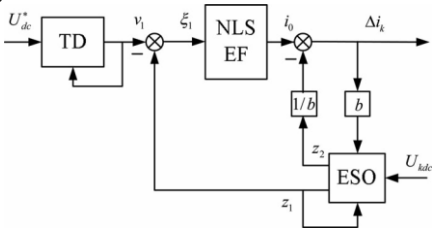

Fig. 7 Block diagram of clustered balancing control.

5.3 Individual Balancing Control

As the overall dc voltage and the clustered dc voltage are controlled and maintained, the individual control becomes necessary because of the different cells have different losses. The aim of the individual balancing control as the third level control is to keep each of 12 dc voltages in the same cluster equaling to the dc mean voltage of the corresponding cluster. It plays an important role in balancing 12 dc mean capacitor voltages in each cluster. Due to the symmetry of structure and parameters among the three phases, a-phase cluster is taken as an example for the individual balancing control analysis.

Fig. 4.8 shows the charging and discharging states of one cell. According to the polarity of output voltage and current of the cell, the state of the dc capacitor can be judged. Then, the dc capacitor voltage will be adjusted based on the actual voltage value.

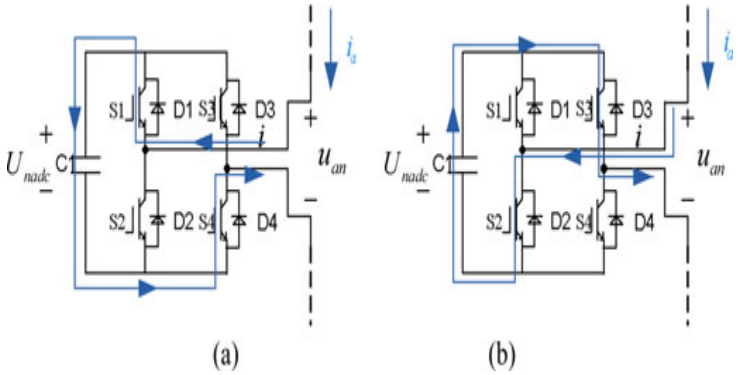

Fig. 8 Charging and discharging states of one cell. (a) Charging state. (b) Discharging state.

As shown in Fig. 4.8, at some point, the direction of the current is from the grid to STATCOM. If S1 and S4 are open, the output voltage of the *n*th cell is positive. The current flows into the dc capacitor along the direction which is shown in Fig. 4.8(a) and charges the capacitor. Likewise, if S2 and S3 are open, the output voltage of the *n*th cell is negative. The current flows into the dc capacitor along the direction which is shown in Fig. 4.8(b) and discharges the capacitor. Obviously, to make the capacitor voltage of each cell tend to be consistent, the turn on time of the cell with the lower voltage should be extended and the turn-on time of the cell with the higher voltage should be shortened in charging state. Then, in discharging state, the process is contrary. The adjustment principle of the dc capacitor voltage can be summarized as follows.

1. When ($i_a \times u_{an}$) > 0, if $U_{nadc} < U_{adc}$, it needs to increase the duty cycle. If $U_{nadc} > U_{adc}$, it needs to reduce the duty cycle.
2. When ($i_a \times u_{an}$) < 0, if $U_{nadc} > U_{adc}$, it needs to increase the duty cycle. If $U_{nadc} < U_{adc}$, it needs to reduce the duty cycle.

i_a is output current of a-phase cluster. u_{an} is ac output voltage of the nth (n = 1, 2,…., 12) cell of a-phase cluster. U_{adc} is the dc mean voltage of 12 cascaded converter cells in a-phase cluster. U_{nadc} is the capacitor voltage of the n^{th} cell of a-phase cluster.

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Volume 04 Issue-17
December 2017

According to the previous method, the direction and the magnitude of adjustment of the duty cycle for one cell can be achieved easily at some point.

Fig. 4.9 shows the adjustment method of the duty cycle by shifting the modulation wave vertically. Taking the first half period of the modulation wave as an example, the value of the modulation wave is greater than zero and the cell outputs zero level and 1 level. When the level is zero, the capacitor is not connected to the main circuit and it is not in the state of the charging and discharging. To reduce the charging time for one capacitor, it needs to reduce the action time of 1 level. And it can be realized by reducing the turn-on time of S1and S4 (as shown in Fig. 4.8). The state of the left bridge arm is decided by comparing the normal modulation wave with the triangular carrier. The state of the right bridge arm is decided by comparing the opposite modulation wave with the triangular carrier. Therefore, taking *x*-axis as the boundary, the duty cycle is reduced by shifting down the normal modulation wave and shifting up the opposite modulation wave according to

$$u_i = u_{i0} - k * e_{U\,\mathrm{dc}}$$

$$u_i = u_{i0} + k * e_{U\,\mathrm{dc}}$$

where $e_{U\,dc} = U_{nadc} - U_{adc}$. k is regulation coefficient. u_{i0} is the previous modulation wave. u_i is the new modulation wave.

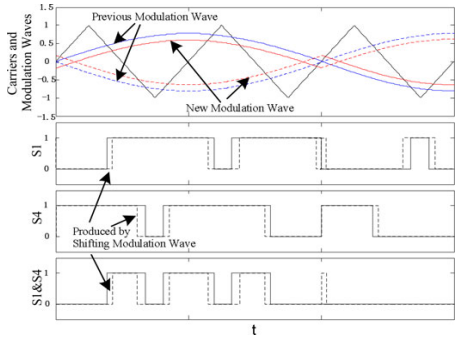


Fig. 9 Process of shifting modulation wave.

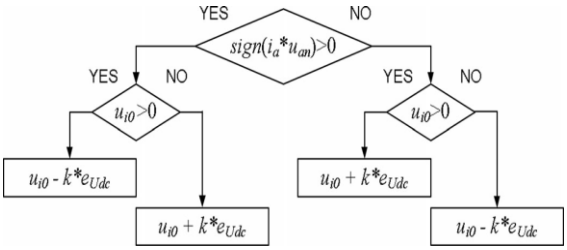


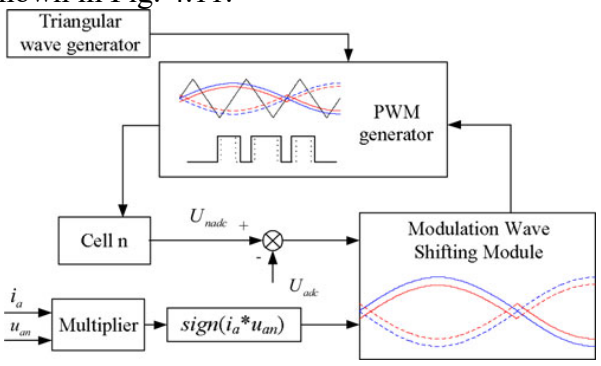
Fig. 10 Flowchart of shifting modulation wave.

The previous principle is also suitable for reducing discharging time and prolonging the charging and discharging times of the cell. Summing up the previous analysis, the method can be illustrated as follows.

1.If the requirement is to reduce the duty cycle, it needs to shift down the normal modulation wave and shift up the opposite modulation wave.

2.If the requirement is to prolong the duty cycle, it needs to shift up the normal modulation wave and shift down the opposite modulation wave.

The value of shifting is decided by k * $e_{U\,dc}$ and the flowchart is shown in Fig. 4.10. The previous method is the modulation strategy that is based on CPS-SPWM in this paper and it is very easy to be realized in the FPGA. But, it is not to say that this method must be used like this only. In order to regulate the duty cycle, as long as the pulse signal is achieved by comparing the modulation wave with the carrier, the modulation strategy is able to use this method. The implementation block diagram of the individual balancing control method is shown in Fig. 4.11.



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Volume 04 Issue-17
December 2017

Fig. 11 Block diagram of individual balancing control.

5.4 Passivity Based Control

Passivity based control looks over clustered balancing control and overall voltage control. The output of clustered balancing control, Δi_k (k = a, b, c) is transformed to d-q form by d-q transformations. The direct current output i.e. i_{dcd} is considered and the quadrature current output i_{dcq} is earthed. Conference current is calculated from the load currents i_{lk}(k = a, b, c) by d- q transformations and the direct current value i^*_d is considered. The output of overall voltage control i_{dc} is also considered. These three currents, i_{dcd}, i^*_d, i_{dc} are sent to the error detector and the error signal is sent to PBC as i^*_{dnew}.

The quadrature current value i^*_q of the conference current is also one of the inputs of PBC. The source voltages u_{sk}(k = a, b, c) are also transformed into d-q values and the outputs of these transformations u_{sd} and u_{sq} are fed to PBC. The line currents i_k(k = a, b, c) are also transformed to i_d and i_q values and are given as inputs to PBC.

Hence the six inputs of PBC block are i^*_{dnew}, i_d, i^*_q, i_q, u_{sd}, u_d out of which the latter two are voltage inputs where as the first four are current inputs. These current inputs are linked with the resistors and inductors and the output voltages are then compared to the voltage inputs. While linking with the inductors, differentiation of the current inputs is done. The reference voltages u^*_a, u^*_b, u^*_c are calculated by inverse d-q transformations of the calculated direct and quadrature voltages from these six inputs.

As shown in Fig. 4.12, the direct axis voltage u_d is calculated by the summation of the following terms.

1. Direct axis source voltage u_{sd}
2. Negative product of inductor L and differentiated value of i^*_{dnew}, - L * (di^*_{dnew}/dt)
3. Negative product of resistor R and i^*_{dnew}, – R * i^*_{dnew}
4. Product of inductance ωL and i^*_q, ωL * i^*_q
5. Product of i_d and resistance R_{a1}, i_d * R_{a1}

$u_d = u_{sd} - L * (di^*_{dnew}/dt) - R * i^*_{dnew} + \omega L * i^*_q + i_d * R_{a1}$

As shown in Fig. 4.12, the quadrature axis voltage u_q is calculated by the summation of the following terms.

1. Quadrature axis source voltage u_{sq}
2. Negative product of inductor L and differentiated value of i^*_q, - L * (di^*_q/dt)
3. Negative product of resistor R and i^*_q, - R * i^*_q
4. Negative product of inductance ωL and current i^*_{dnew}, ωL * i^*_{dnew}
5. Product of resistor R_{a2} and current i_q, R_{a2} * i_q

$u_q = u_{sq} - L * (di^*_q/dt) - R * i^*_q + \omega L * i^*_{dnew} + R_{a2} * i_q$

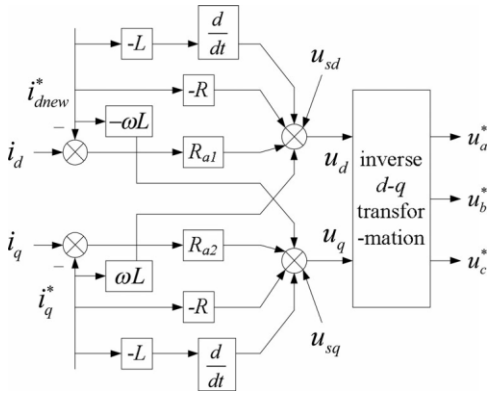

Fig. 12 Block diagram of PBC.

Thus these two voltages u_d and u_q which are calculated as shown above are transformed to three phase voltages by inverse d-q transformations and then those transformed voltages are sent to the individual balancing control as shown in Fig. 4.4.

6. SIMULATION RESULTS

The main theme of the paper is to reduce the size of the multilevel STATCOM and also for easy control of the system. The response time of the system has drastically improved due

to the introduction of closed loop control system containing different control blocks for different modes of control. Although the injection of harmonics occurs due to the introduction of power electronic equipment, it is also compensated by active disturbances rejection controller (ADRC), thanks to the extended state observer (ESO) in the ADRC system.

The complete system is developed in MATLAB and simulated for the output results. The outputs of the MATLAB circuit are as expected and quite satisfactory. At first let us see the circuit developed in MATLAB. Fig. 5.1 is the MATLAB circuit for H-Bridge Cascaded STATCOM. Fig. 5.2 is the complete control block of H-Bridge Cascaded STATCOM.

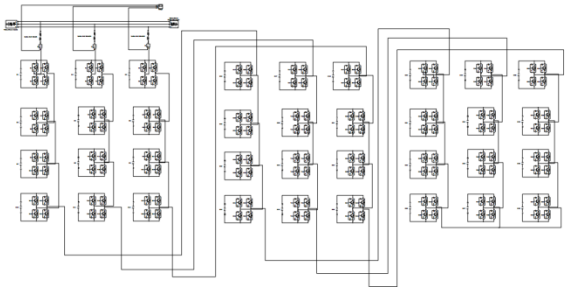

Fig. 13 H-Bridge Cascaded STATCOM with 12 Bridges per phase.

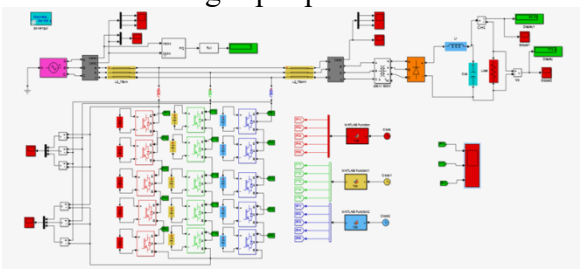

Fig. 14 H-Bridge Cascaded STATCOM with Control Block.

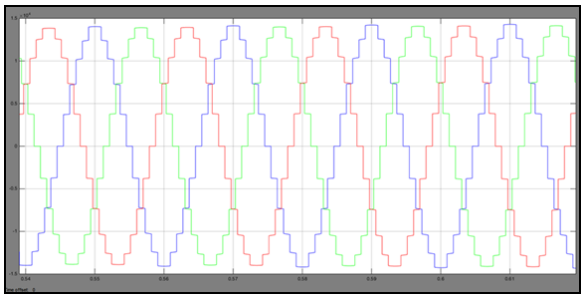

Fig. 15 Three phase STATCOM current output.

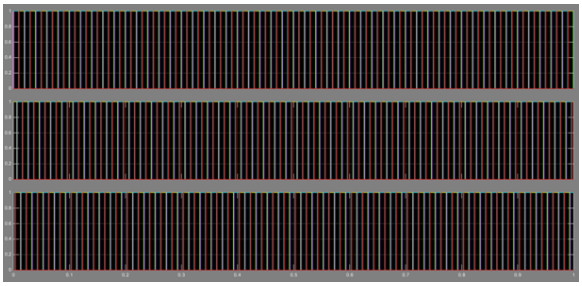

Fig. 5.4 Gate pulses for each block.

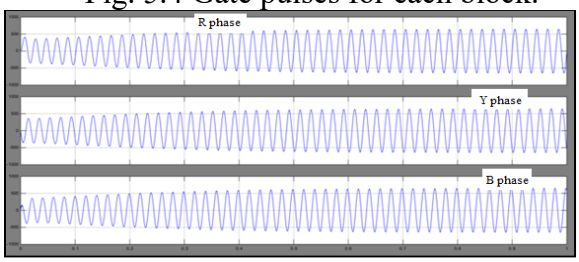

Fig. 16 Load current Pulses after STATCOM.

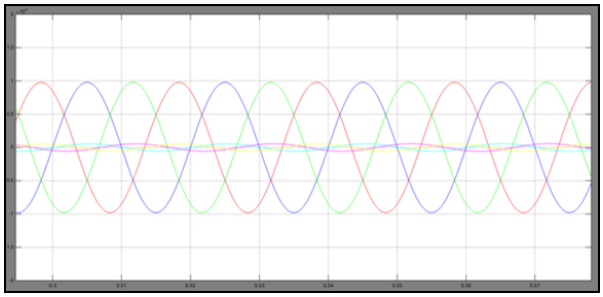

Fig 17. Source voltage and STATCOM Voltage Pulses.

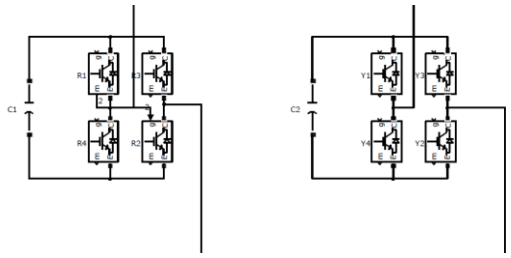

Fig. 18 Individual Capsule of H-Bridge

Section IV:
CONCLUSION

We have analyzed the fundamentals of STATCOM based on multilevel H-bridge converter with star configuration. And then, the actual H-bridge cascaded STATCOM rated at 10 kV 2 MVA is constructed and the novel

control methods are also proposed in detail. The proposed methods have the following characteristics.

A PBC theory-based nonlinear controller is first used in STATCOM with this cascaded structure for the current loop control, and the viability is verified by the simulation results.

The PR controller is designed for overall voltage control and the simulation result proves that it has better performance in terms of response time and damping profile compared with the PI controller.

The ADRC is first used in H-bridge cascaded STATCOM for clustered balancing control and the simulation results verify that it can realize excellent dynamic compensation for the outside disturbance.

The individual balancing control method which is realized by shifting the modulation wave vertically can be easily implemented in the FPGA.

The simulation results have confirmed that the proposed methods are feasible and effective. In addition, the findings of this study can be extended to the control of any multilevel voltage source converter, especially those with H-bridge cascaded structure.

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