International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

Analysis of Dual Flying Capacitor Active-Neutral-Point-Clamped Multilevel Inverter Induction Motor Drives

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ABSTRACT: *This thesis aims to extend the knowledge about the performance of different multilevel inverter induction motor drives through harmonic analysis. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. Hybrid multilevel converters combine features of conventional multilevel topologies to provide an acceptable tradeoff between the advantages and disadvantages of these converters. For many industrial applications, common dc link is a requirement that limits the choice of topologies to neutral point clamped (NPC) and flying capacitor multicell (FCM) hybrid types. This paper investigates the operation of a hybrid five-level topology and proposes a modulation method that takes the advantage of the combined features of NPC and FCM. The dual flying capacitor (FC) active-neutral-point-clamped (DFC-ANPC) converter provides certain advantages such as natural soft switching of line frequency switches, elimination of the transient voltage balancing snubbers, and a more even loss distribution. Simulation results and verification of the five-level DFC-ANPC converter are presented to validate the performance of the converter as well as the applied modulation technique.. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed.*

I. INTRODUCTION

1.1 GENERAL:

MEDIUM-VOLTAGE multilevel converters have found wide use in applications such as motor drive, grid-tied inverter and rectifier, and medium voltage dc (MVDC) [1], [2]. The main motivation for the use of multilevel converters is to achieve higher voltage capability with commercially available lower voltage semiconductor devices. Typical fast switches such as IGBTs and IGCTs with voltage ratings up to 6.5 kV can reliably operate at about 4 kV [3], [4]. One way to handle higher voltage applications is direct series connection of switching devices; however, this solution has inherent transient voltage balancing and high dv/dt issues. Multilevel converters thus rose to the occasion. They also have the added advantages of better waveform quality, lower total harmonic distortion (THD), and lower electromagnetic interference (EMI) over their two-level counterparts [5]. For applications such as MVDC, a common dc link among the three phases is a requirement. For some other applications such as motor drive, a common dc link offers the option of eliminating or reducing the complexity of phase-shift transformer at the passive front end. For certain configurations such as active front end, typically a common dc link is required. In addition, less protection and clamp circuit is required for a single common dc link in contrast to several dc links [5]–[9]. Conventionally, two multilevel converter topologies, neutral point clamped (NPC) [10] and flying capacitor multicell (FCM) [11], [12], are known to provide a common dc link. NPC and its enhanced variety, active NPC (ANPC), are widely used in industry for three-level applications [7]. For higher levels, however, NPC encounters the critical dc-link voltage balancing problem, excessive number of clamping diodes, and unbalanced loss distribution among semiconductor devices. FCM stands out as an alternative for higher levels with balanced flying capacitor (FC) voltage and excellent loss distribution [9]. The disadvantage of FCM topology, however, is the excessive number of capacitors in higher levels. Capacitors are usually avoided due to high initial price, maintenance and replacement surcharges, and low reliability [13]. Hybrid multilevel converter topologies with a common dc link combine some features of NPC and FCM that opens the possibilities to take advantages of both topologies. Among hybrid topologies, the five-level FC active NPC (FC-ANPC) provides an acceptable compromise between cost and performance and consequently, found its way to industrial applications [14]. FC-ANPC provides a balanced dc-link voltage by using only one FC at the cost of four additional switches per phase compared to the conventional basic topologies [15]. It offers a good trade off compared to the disadvantages of FCM and NPC converters. One drawback of the FC-ANPC topology is the four pairs of series-connected switches, which, although operating at the line frequency, require transient voltage balancing snubbers [16]. The uneven loss distribution among semiconductor devices is another major issue that limits the nominal power of this converter.

II. INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

3.1Cascaded H-Bridges inverter:

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 3.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \text{ where } n = 1,3,5,7 \ldots$$

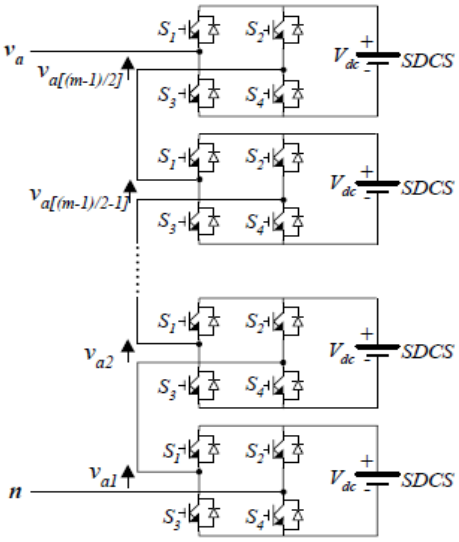

Fig.1Single-phase structure of a multilevel cascaded H-bridges inverter

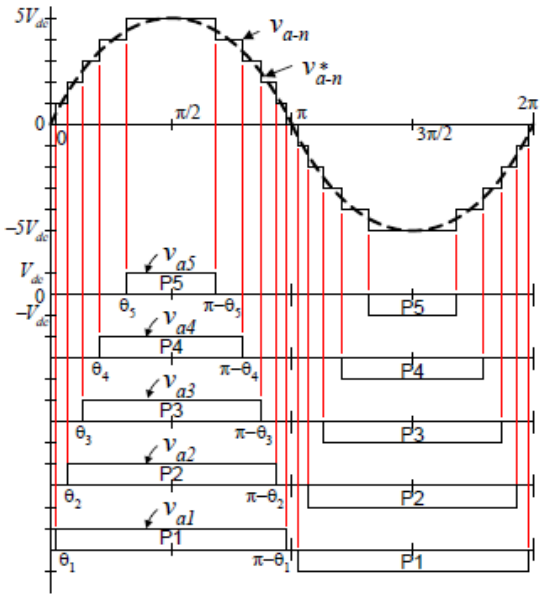

Fig.2 Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

III. DFC-ANPC TOPOLOGY AND OPERATION

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
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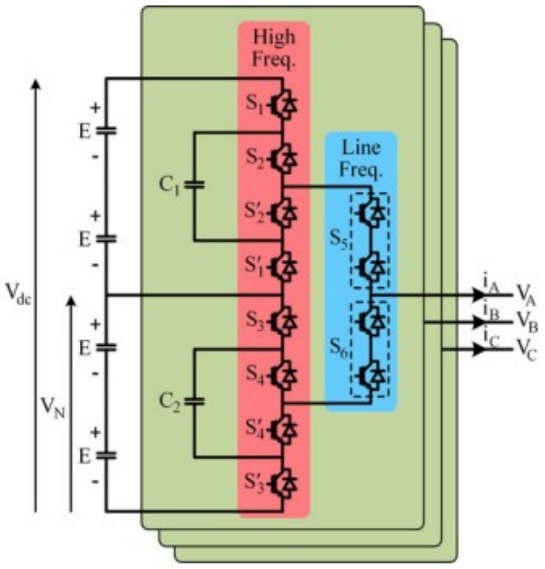

Fig. 3. Five-level DFC-ANPC topology

The five-level DFC-ANPC topology, as shown in Fig.3, can be viewed as two three-level FCM converter units connected to the output through line frequency switches S5 and S6 . The top FCM unit uses high-frequency switches S1 ,S 1 ,S2 , and S 2 along with capacitor C1 to generate the positive half cycle of the pulsewidth-modulated (PWM) waveform. The generated voltage is transferred to the output through S5 during the positive half cycle. During the negative half cycle, the bottom FCM unit, consisting of S3 ,S 3 ,S4 ,S 4 , and C2 , generates the PWM waveform, which is transferred to the output through S6 . The voltage of the FCs, C1 and C2 , can be individually balanced through the existing redundant states of each FCM unit. Table I lists the switching states for the DFC-ANPC converter and the effect of each state on the FCs voltages. The redundant states for level +E, i.e., +EP and +E0, are used to balance C1 's voltage. Similarly, the redundant states for level −E, i.e., −E0 and −EN, are used to balance C2 's voltage. During the normal operation, the operating voltage of both FCs in the DFC-ANPC five-level converter is a quarter of the dc-link voltage, which means E. This results in clamping the voltage stress of high-frequency switches to E. For line frequency switches, however, voltage stress is half of the dc-link TAB voltage, i.e., 2E, which may be realized by two switches in series, as shown in Fig. 1. An important feature of this topology is the "soft cycle commutation" between the positive and negative half cycles. States 0P, 0N, and 00, as listed in Table I, can generate level 0 either through the top part switches S 1 ,S 2 ,S5 , the bottom part switches S3 ,S4 ,S6 , or both. The inbound and outbound current paths in each case are shown in Fig. 2. At the transition from 0P to 00, S6 must turn on while the voltage across it is near zero. When switching back from 00 to 0P, S6 must turn off while the voltage across it is near zero. In a similar fashion, the voltage across S5 is near zero when switching between 00 and 0N. Therefore, if 00 is used as an intermediate state between 0P and 0N, line frequency switches S5 and S6 will hold zero-voltage switching operation at all times. So, when the phase voltage half cycle changes, the operating FCM unit can be softly detached from output, and the operation can be softly handed over to the other FCM unit. An advantage of this phenomenon is the elimination of switching loss on S5 and S6 . More importantly, no transient voltage balancing snubber is required when realizing S5 and S6 by series-connected switches. Note that the blocking mode voltage balancing resistors may still be required due to the switching devices' cutoff current tolerance [16].

TABLE I
SWITCHING STATES OF THE FIVE-LEVEL DFC-ANPC CONVERTER

Level	State	S_1	S_2	S_3	S_4	S_5	S_6	C_1	C_2
+2E	+2E	1	1	1	1	1	0	N.A.	N.A.
+E	+EP	1	0	1	1	1	0	$i_x > 0$ Charge $i_x < 0$ Discharge	N.A.
	+E0	0	1	1	1	1	0	$i_x > 0$ Discharge $i_x < 0$ Charge	N.A.
0	0P	0	0	1	1	1	0	N.A.	N.A.
	00	0	0	1	1	1	1	N.A.	N.A.
	0N	0	0	1	1	0	1	N.A.	N.A.
−E	−E0	0	0	1	0	0	1	N.A.	$i_x > 0$ Charge $i_x < 0$ Discharge
	−EN	0	0	0	1	0	1	N.A.	$i_x > 0$ Discharge $i_x < 0$ Charge
−2E	−2E	0	0	0	0	0	1	N.A.	N.A.

S_1', S_2', S_3', S_4' are switched complementary to S_1, S_2, S_3, S_4, respectively.
$i_x > 0$ represents outbound current and $i_x < 0$ represents inbound current.
N. A. = Not Affected.

3.1 MODULATION TECHNIQUES:

Various modulation techniques may be adapted for the DFCANPC topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation (SVM) and selective harmonic elimination (SHE) may be used to generate the gate signals [5], [19]. The choice of a modulation technique is mostly a tradeoff among the requirements of the application, complexity of the software, and relative cost of the control hardware. For the DFC-ANPC topology, the main requirement is to ensure the FC voltages are balanced and the neutral point voltage is maintained at half of the dc-link voltage

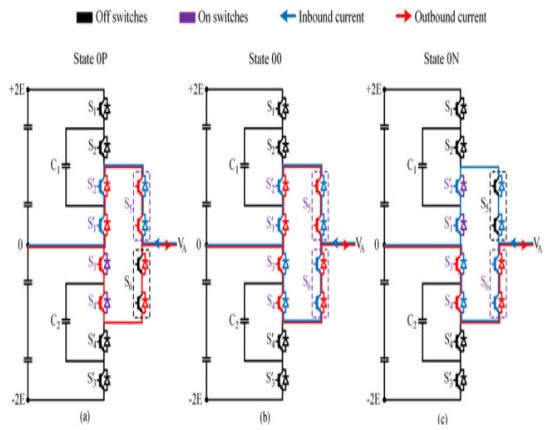

Fig 4. Soft cycle commutation concept. Inbound and outbound current paths for states (a) 0P, (b) 00, and (c) 0N.

A. Carrier-Based Modulation

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel converters. As for carrier set's arrangement, level-shifted carriers (LSCs) and phase-shifted carriers (PSCs) are the two main categories that are suitable for diode-clamped and multicell structures. Two members in the LSC family, alternative phase opposition disposition (APOD) and phase disposition (PD), are known to generate the best results for singe-phase and three-phase converters, respectively [19]. PSC in its original form has been shown to generate a multilevel PWM waveform that matches with APOD [20]. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [21]. The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to the possibility of common-mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc-link utilization, lower THD, lower loss, and neutral point voltage control [22], [23]. For the DFC-ANPC converter, a hybrid modulation technique is required due to the hybrid structure of the topology. Fig. 3 illustrates the carrier-based modulation technique using PSC with sinusoidal reference for single-phase case. It is intuitive to separate the operation to positive and negative half cycles, since each one is generated with an independent three-level FCM unit. The gate signals for each FCM unit is then generated using PSC to provide natural voltage balancing for the FCs [24]. Switches S5 and S6 must be on during the positive and negative half cycles, respectively, to connect the associated FCM unit to the output. Note that, soft cycle commutation, S5 and S6 can be achieved by a short duration of overlap at transition from positive half cycle to negative half cycle and vice versa. The PWM waveform generated at the output matches the APOD scheme. For three-phase cases, a similar approach may be adopted except that, to generate a PD scheme equivalent, the positive half cycle carriers should hold $\pi/2$ phase shift with respect to the negative half-cycle carriers. Also, the carriers incorporate a dynamic phase shift, which always adds up by $\pi/2$ at the carrier band transitions for sampled reference waveforms [21]. For the reference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar performance as SVM [22], [25]. Fig. 4 illustrates the modulation technique using sampled CSV-PWM along with modified PSC for the DFC-ANPC converter. It is important to choose a reference waveform with balanced common-mode injection to maintain the neutral point's voltage balance. Also, higher frequency and lower amplitude of the injected common mode can decrease the neutral point's voltage ripple.

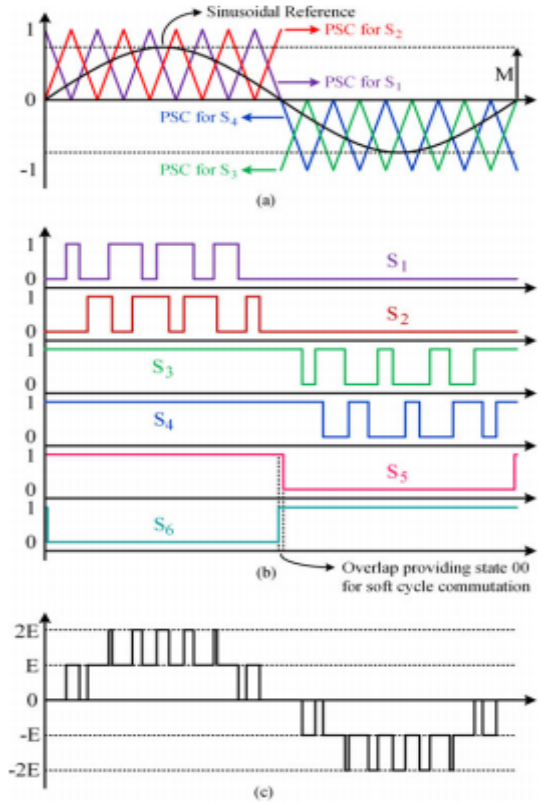

Fig 5: Carrier-based modulation using PSC with sinusoidal reference for single-phase converters. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform

IV. PROPOSED SIMULATION DIAGRAM

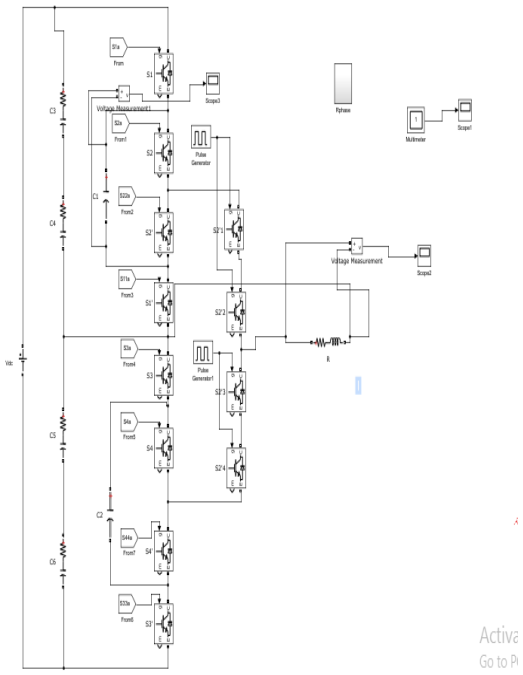

Fig6: Simulink model of single phase system

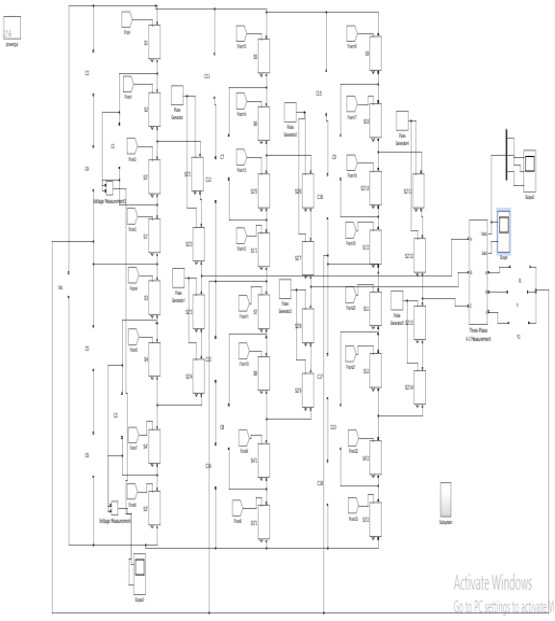

Fig7 Simulink model of three phase system

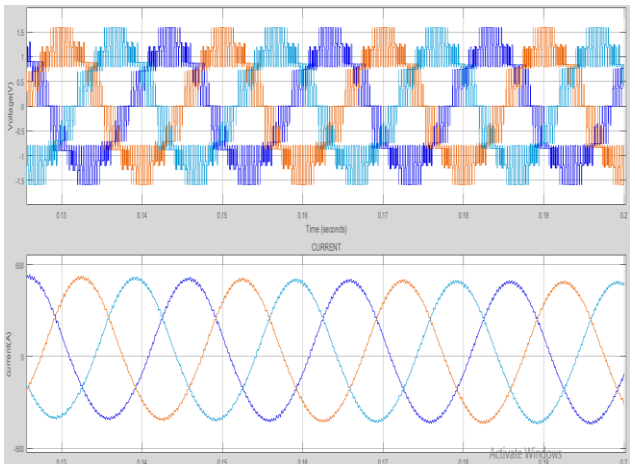

Fig 5.15 line to line voltage Voltage&cuurent

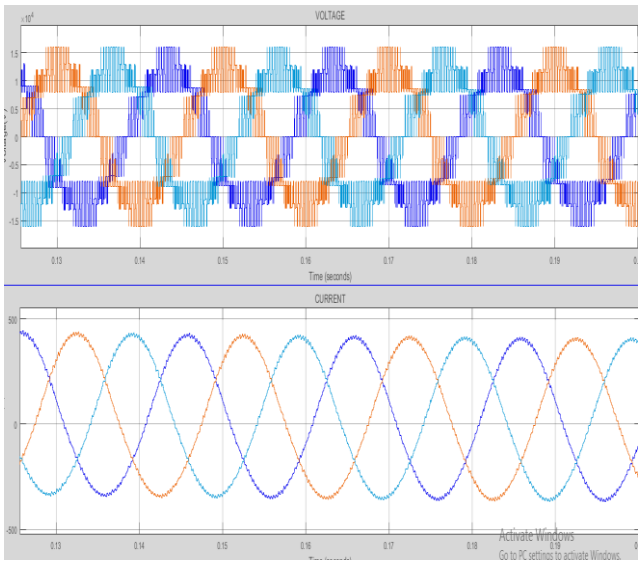

Fig 8: phase ground voltages&currents

V. CONCLUSION

In this paper, the operation of the DFC-ANPC topology has been investigated and the associated modulation techniques have been presented and verified by simulation and experimental results. Compared to the commercialized five-level FC-ANPC converter, the DFC-ANPC converter under the proposed modulation method has the following features: 1) provides more even loss distribution among semiconductor switches and thus higher power rating is expected; 2) eliminates the transient voltage balancing problem of series-connected switches; 3) decreases the switching loss and thus slight improvement in efficiency is expected; 4) can be extended to higher levels without transient voltage balancing problem. The comparison presented in this paper is mostly based on abductive reasoning and not quantified. For future work, a comparative study of the FC-ANPC and DFC-ANPC thermal models will verify the thermal performance superiority and provide an estimation of the amount of extra power processing capability.

FUTUTRE SCOPE

There are still some improvements which can be added to the system. First of all, it would be very interesting that the energy storage system such as battery or super-capacitor can be integrated into the system. This will make the system more reliable. When there is no radiation at all, the system can still provide power from the energy storage system.

Secondly, other micro-sources such as Fuel Cells can also be used as the separate DC sources for each module.

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