

Suppression of Double-Frequency Ripple with Fuzzy Control Based Single-Phase Pv Quasi-Z-Source Inverter

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Abstract- according to the single phase photovoltaic system (PV), which exist a double frequency mismatch that exist between the dc input side and ac output side. To buffer out the double frequency ripple energy it is necessary to required. A capacitance reduction control strategy is proposed to buffer the DFR energy in single-phase Zsource/quasi-Z-source inverter applications is proposed in this paper. In single-stage photovoltaic (PV) system, there is a power irregularity exist between the AC yield and DC input. Here we are using the fuzzy logic controller, because it has many advantages comparing to other controllers. Such as, the fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. The double-frequency ripple (DFR) energy needs to be buffered by passive network. The ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, due to their high capacitance electrolytic capacitors are usually used. Electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. The proposed control strategy can significantly reduce the capacitance requirement and achieve low input voltage DFR. Consequently, highly reliable film capacitors can be used. Due to the proposed control strategy the increased switching device voltage stress and power loss will also be discussed. By using the simulation results we can analyze the proposed method.

Index Terms—Capacitance reduction, doublefrequency ripple (DFR), Z-source (ZS)/quasi-Z-source (qZS), Fuzzy logic control.

INTRODUCTION

In the recent years for the photovoltaic application the voltage fed z-source inverter and quasi z-source inverter is considered. This inverter feature single stage buck boost transformer. It is due to shoot through capability. For the single phase and three phase applications the z-source inverter and quasi z source inverter are utilized. The voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) has been considered for photovoltaic (PV) application in recent years [1-3]. These inverters feature single-stage buck-boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1-5]. The single phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance [6-10].

The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In three-phase applications, the Z-source (ZS)/ quasi-Zsource (qZS) network only needs to be designed to handle the high frequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is shown in Fig. 1.





Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency. The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to study the low frequency ripple issues qZSI is used in this paper. A single phase qZSI system is shown in fig.1. The output power at DC side is pure DC and AC side power contains DC component plus AC ripple component whose frequency is two times the grid frequency. The mismatched AC ripple in the system is coined as double frequency ripple (DFR).

In this paper, a new control strategy is proposed for ZSI/ qZSI to mitigate the input DFR without using large capacitance, which enables us to use the highly reliable film capacitors. There is no extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. The gallium nitride (GaN)



devices are applied in the inverter to increase the system efficiency at high switching frequency. Finally, experimental results are provided to verify the effectiveness of the proposed control system.

In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which has higher voltage rating than C2. The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected.

Two additional smoothing-power circuits are employed to reduce the DFR of DC-link voltage in ZSI. However, the added circuits increase the system cost and complexity. A low-frequency harmonic elimination PWM technique is presented to minimize the double frequency ripple on Z-source capacitors. However, the method is used for application with constant voltage input source and double-frequency ripple current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels.

PROPOSED CONTROL SYSTEM FOR CAPACITANCE REDUCATION

The basic principle of the proposed capacitance reduction method can be explained by (1).

$$\Delta E = \frac{1}{2}C(v_{C-max}^2 - v_{C-min}^2) \quad (1)$$

where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and vC-max and vC-min are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE . One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input.



Fig. 2. The modulation strategy of (a) traditional method

In conventional single-phase qZSI, the modulation strategy is shown in Fig. 2(a). The two phase legs of the full bridge are modulated with 1800 opposed reference waveforms, m and , m , to generate three-level voltage output. Two straight lines *p v and * vn are used to generate the shoot through duty ratio. When the triangular carrier is greater than v*p or the carrier is smaller than * vn , all four switches S1 – S4 turn on simultaneously for shoot-through.

In the proposed control system, the shootthrough control lines * v p and vn* are modified to a line with doublefrequency component as shown in Fig. 2(b).





By doing so, the dc side and the qZS capacitor DFR can be decoupled. An input DFR suppression controller is added in the control system to generate the double-frequency component in v^*p and * vn.





Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, gridconnected current controller, qZS capacitor voltage controller and input DFR suppression controller. The MPPT controller provides the input voltage reference vIN*. The error between vIN * and vIN is regulated by a PI controller



and its output is the magnitude of the grid current reference. The grid current ig is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency. The qZS capacitor voltage is regulated by controlling dSH. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and vC2 information is required for the implementation. Due to the limited space, the detail of the active damping is not presented in this paper and will be covered in future paper. The vC2 voltage controller only regulates the average value of vC2, which is Vc2 ave, due to the low-pass filter in the signal feedback with a cutoff frequency of 25Hz. Therefore, the capacitor voltage controller has limited influence on double frequency component and most DFR energy can be kept in qZS capacitors. Vdc_ave* should be selected carefully so that the value of dSH does not become negative because of the double-frequency swing, and the summation of dSH and m is always smaller than 1. A feed forward component Vc2*/ Vdc_ave* is added to the output of the capacitor voltage controller to increase the dynamic performance.

IMPACT OF CAPACTICANCE REDUCTION A. System stability

In order to apply the proposed control system, it is necessary to study impact of decreasing C1 on system stability. The possible operation states of voltage fed qZSI have been presented in [13] and it is summarized in the appendix with equivalent circuits, and the averaged model of qZSI can be obtained as in (2).

$$\begin{cases} L_{1} \frac{di_{L1}}{dt} = \left(1 + \frac{T_{AB} + T_{0B}}{T_{s} - T_{AB} - T_{0B}}\right) (v_{C1} + v_{C2}) d_{SH} + \frac{T_{SBU}}{T_{s} - T_{AB} - T_{0B}} (v_{C1} + v_{C2}) - v_{C1} + v_{1N} \\ L_{2} \frac{di_{L2}}{dt} = \left(1 + \frac{T_{AB} + T_{0B}}{T_{s} - T_{AB} - T_{0B}}\right) (v_{C1} + v_{C2}) d_{SH} + \frac{T_{SBU}}{T_{s} - T_{AB} - T_{0B}} (v_{C1} + v_{C2}) - v_{C2} \\ C_{1} \frac{dv_{C1}}{dt} = i_{L1} - (i_{L1} + i_{L2}) d_{SH} - \frac{T_{SBU}}{T_{s}} (i_{L1} + i_{L2}) - \left(\frac{T_{AC}}{T_{s}} + \frac{T_{AB}}{T_{s}}\right) i_{DC} \\ C_{2} \frac{dv_{C2}}{dt} = i_{L2} - (i_{L1} + i_{L2}) d_{SH} - \frac{T_{SBU}}{T_{s}} (i_{L1} + i_{L2}) - \left(\frac{T_{AC}}{T_{s}} + \frac{T_{AB}}{T_{s}}\right) i_{DC} \end{cases}$$

$$(2)$$

where T s is the switching period, TAB, T0B, TSBU, TAC, and TSBI are time intervals of different operation states, as listed in the appendix, m is the modulation signal and dSH = TSBI / Ts. The small signal model can be derived accordingly as in (3).

$$\begin{pmatrix} L_{1} \frac{d\hat{\imath}_{L1}}{dt} = \left(1 + \frac{T_{AB} + T_{0B}}{T_{s} - T_{AB} - T_{0B}}\right) (v_{C1} + v_{C2}) \hat{d}_{SH} + \frac{T_{SBU}}{T_{s} - T_{AB} - T_{0B}} (\hat{v}_{C1} + \hat{v}_{C2}) - (1 - D_{sh}) \hat{v}_{C1} + D_{sh} \hat{v}_{C2} + v_{1N} \\ L_{2} \frac{d\hat{\imath}_{L2}}{dt} = \left(1 + \frac{T_{AB} + T_{0B}}{T_{s} - T_{AB} - T_{0B}}\right) (v_{C1} + v_{C2}) d_{SH} + \frac{T_{SBU} + T_{AB} + T_{0B}}{T_{s} - T_{AB} - T_{0B}} (\hat{v}_{C1} + \hat{v}_{C2}) - (1 - D_{sh}) \hat{v}_{C2} + D_{sh} \hat{v}_{C1} \\ C_{1} \frac{d\hat{v}_{C1}}{dt} = \left(1 - D_{Sh} - \frac{T_{SBU}}{T_{s}}\right) \hat{\imath}_{L1} - \left(D_{Sh} + \frac{T_{SBU}}{T_{s}}\right) \hat{\imath}_{L2} + (I_{l1} + I_{l2}) \hat{d}_{SH} - \left(\frac{T_{AC}}{T_{s}} + \frac{T_{AB}}{T_{s}}\right) \hat{\imath}_{DC} \\ C_{1} \frac{d\hat{v}_{C1}}{dt} = \left(1 - D_{Sh} - \frac{T_{SBU}}{T_{s}}\right) \hat{\imath}_{L1} - \left(D_{Sh} + \frac{T_{SBU}}{T_{s}}\right) \hat{\imath}_{L2} + (I_{l1} + I_{l2}) \hat{d}_{SH} - \left(\frac{T_{AC}}{T_{s}} + \frac{T_{AB}}{T_{s}}\right) \hat{\imath}_{DC} \end{cases}$$

$$(3)$$

This RHP zero will limit the system dynamic response. However, the decrease of C1 will not significantly change the position of the RHP zero. There are two pairs of conjugated poles located on the imaginary axis, which indicate possible resonances at two different frequencies. The lowerfrequency resonance is more related to C1 and the higher-frequency resonance is mainly determined by C2. Therefore, it is seen that the higher resonant frequency does not change much with the C1 change. The lower resonant frequency increases when C1 decreases. Because there is always a zero close to the lower-frequency pole, the lower-frequency resonance is largely damped. Decreasing C1 does not affect the system stability much.





When the proposed method is applied, the doublefrequency voltage ripple across vC1 and vC2 will be increased intentionally. The dc link voltage across the H-bridge vDC will also include DFR which could increase the voltage stress of switching devices. Because vC1 is much higher than vC2, most double-frequency energy is stored in C1. The value of vC1 can be calculated using the following equation

$$\frac{1}{2}C_1v_{C1}^2 = \frac{1}{2}C_1v_{C1-ave}^2 + \int_0^t (P_{in} - P_{AC})dt \quad (4)$$

where V ave c1 _ is the average value of vC1, Pin is the input power and pAC is the instantaneous ac output power. pAC can be calculated in (6).

$$PAC = V_{g-p} \sin(\omega t) * I_{g-p} \sin(\omega t) =$$
$$12Vg-pIg-pI-cos2\omega t=PinI-cos2\omega t(5)$$

where V g_p and Ig_p are the peak value of vg and ig. Therefore, we can get

$$v_{C1} = v_{C1-ave} + \Delta v_{C1-dfr} = \sqrt{V_{C1-ave}^2 + \frac{Pin}{\omega C_1} \sin(2\omega t)} = \sqrt{\left(\frac{V_{dc-ave} + V_{in}}{2}\right)^2 + \frac{Pin}{\omega C_1} \sin(2\omega t)}$$
(6)

where Δvc_1 dfr is the DFR component of vC1. In (7), the value of Vin and Pin are determined by the PV array operating point. Vdc_ave is indirectly controlled by regulating Vc2_ave as shown in Fig.3. Therefore, when Vdc_ave* is selected and the PV array operating point is determined, vC1 can be calculated. It is seen that larger Δvc_1 dfr can reduce the size of C1. vDC during non-shoot period can be obtained as

$$\frac{v_{DC} = 2v_{C1} - v_{in}}{2} = 2\sqrt{\left(\frac{V_{dc-ave} + V_{in}}{2}\right)^2 + \frac{P_{in}}{\omega C_1}\sin(2\omega t) - V_{in}}$$
(7)

It is seen from (8), when C1 and Pin are fixed, the switching device voltage stress is mainly determined by Vdc_ave and Vin. There is an optimized value of Vdc_ave* for different input voltage conditions to minimize the switching device voltage stress.

$$m = \frac{V_{g-p}\sin(\omega t)}{v_{DC}}$$
(8)

In order to take advantage of the buck-boost feature of the qZSI, the input voltage range is usually selected that Vg_p is among the input voltage range. For the proposed method, the maximum switching device voltage stress could happen at maximum or minimum Vin. When Vin is larger than Vg_p, no shoot-through is needed in conventional design and dSH equal to zero. However, for the proposed method, certain value of D sh_ave is needed to make sure dSH does not become negative values because

of the double-frequency swing. Higher Vin leads to higher peak value of vDC. Therefore, one of the worst cases for the increased device voltage stress could happen at maximum Vin.



Fig. 5. V*dc-ave and switching device voltage stress at different input voltages.

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.



The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

TABLE I: Fuzzy Rules

				2			
e è	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up



to appropriate system. The value of input error and change in error are normalized by an input scaling factor. In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

E(k) =	$\frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}}$	(9)
CE(k)	= E(k) - E(k-1)	(10)

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a nonfuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, "height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from



Fig.9 output variable Membership functions Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

SIMULATION RESULTS

For the proposed method, there is a design tradeoff between the demand of decreasing C1 and the increased voltage stress across the switching devices.



Fig.10 Block diagram of simulation TABLE II.

Parameters Of The Qzsi Under Study		
qZSI Component	Parameters	
Input voltage v	140-180V	

Input voltage v _{IN}	140-180V		
Grid voltage v_g	120Vrms		
C	2mF for conventional system		
C_I	200μ F for proposed system		
C_2	20µF		
L_{I}	330µH		
L_2	215µH		
L_g	600µH		
Switching frequency	100kHz		

They are provided in Fig. 10. It is seen that the maximum voltage stress across the switching devices happens at Vin=180V in this design.



Fig. 11. The vDC, vIN and vC2 waveforms of the qZSI with the conventional control, C1=2mF.



Fig. 12. The vDC, vIN and vC2 waveforms of the qZSI with the conventional control, $C1=200\mu F$

The waveforms for the qZSI with 200μ F capacitor, but without the proposed control provided in Fig. 12.The waveforms of the system with the proposed control strategy are shown in Fig. 13





Fig. 13. The vDC, vIN and vC2 waveforms of the qZSI with the proposed control, C1=200µF.

The efficiency comparison of the conventional qZSI and the qZSI with proposed control at different power outputs is provided in Table. III.

TABLE III. Efficiency Comparison Of The Conventional Qzsi And Qzsi With The Proposed Control

	300W	400W	500W	600W
C ₁ =2mF with conventional control	93.05%	93.18%	93.66%	93.76%
C ₁ =200µF with proposed control	92.36%	93.06%	93.48%	93.55%





According to the new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the double-frequency ripple energy. In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. By using the fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system control and improve the efficiency. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability. In this paper capacitance reduction control strategy is proposed to buffer the DFR energy in Z source or Quasi Z source inverter application. The proposed control strategy can significantly reduced the capacitance requirement without using any extra hardware component. This can also achieve low input voltage DFR. Consequently a highly reliable film capacitors can used.

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