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Soft-core Processor by Neural Network Pulse Compressor accomplishment

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Abstract: *In pulse radar detection system, pulse compression was achieved by traditional matched filtering techniques. These approaches resulted in low signal-to-sidelobe ratio and were also fault intolerant. Hence, in this paper we suggest a neural network based pulse compression application. The traditional approach of digital pulse compression is first realized by designing a Finite Impulse Response (FIR) based matched filter in matlab simulink. Then, a multilayer feed forward neural network (MFNN), trained using back propagation algorithm with 13-element barker code as the input for pulse compression is realized by coding in matlab. The performance of this neural network is then tested by taking various performance measures into consideration, such as, resolution ability of two mixed pulse trains with delays and different input magnitude ratios, misalignment performance of the network when a particular bit in the input code sequence is discarded or duplicated, the effect of received signal magnitude and signal-to-sidelobe ratio. The performance of both FIR filter and neural network approaches for matched filtering are then compared to decide which of the two approaches has greater advantages and better efficiency by means of matlab simulations. The neural network pulse compressor is then practically implemented on a Vertex-4 Sx-35 Field Programmable Gate Array (FPGA) using Xilinx ISE Design Suite, and results are observed.*

Keywords: **Pulse compression, Barker code, Matched filtering, FIR, MFNN, Vertex-4 Sx-35 FPGA.**

I. INTRODUCTION

In radars for long detection range and finite range resolution, extremely narrow pulses of exceptionally high peak power are required. In order to meet these requirements, a technique called pulse compression is used. In this internally modulated pulses of sufficient width are transmitted to provide necessary average power at a reasonable level of peak power. The echoes are then compressed by decoding their modulation [1].

II. MATAB SIMULINK DESIGN OF FIR MATCHED FILTER AND ITS SIMULATION

The matlab simulink design in Fig.1 shows the construction of modulation and demodulation systems and also pulse compression system with FIR filter based matched filter. The FIR filter based matched filter structure occurs after demodulator part in Fig. 1. The delay elements, equal to the code length, are arranged with respect to last bit of the barker code sequence (1,1,1,1,1, -1, -1, 1, 1,-1, 1, -1, 1) in first delay and first bit of sequence in the last delay. The demodulated barker code bits are then delayed, multiplied and added at each step [6]. Then output then comes out be maximum value whenever the exact code matching occurs, i.e., when the complete barker code is received. All the remaining outputs come out to be 0 or 1 as shown in Fig. 2.

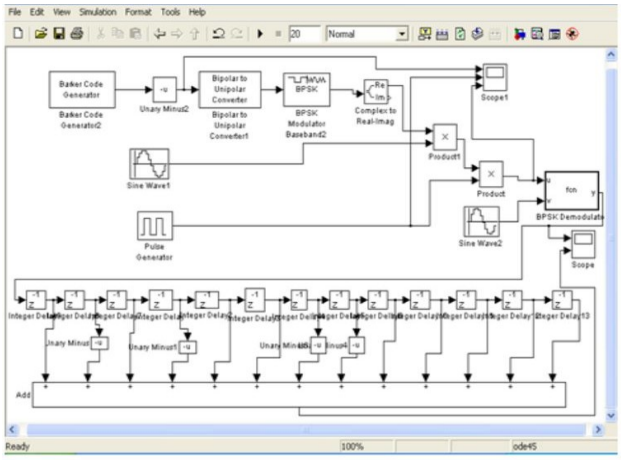

Fig. 1: Simulink block diagram of FIR filter based matched filter

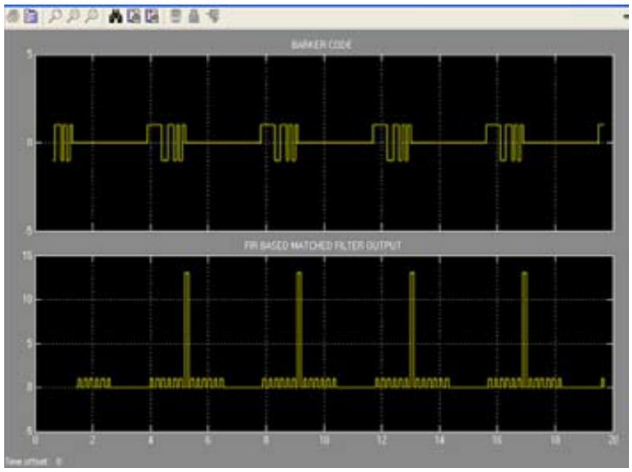

Fig. 2: Pulse compressed output

III. NEURAL NETWORK APPROACH

The neural network used is as shown in Fig. 3. It has thirteen input neurons in the input layer. The number of neurons in the hidden layers is found to be three by pruning the neural network Two among the three hidden layer units are used for proper detection, and another unit

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for robustness. The output unit is a classifier. It gives the output nearly equal to one, if the code used is received and presented as a whole to the input layer. A bias unit which always has a value of 1, is connected to all neurons through weights in the hidden and output layers for better classification. The learning rule used here is the back propagation algorithm with biases training. The activation function used in the hidden and output layers is the sigmoid function. This is used for better classification

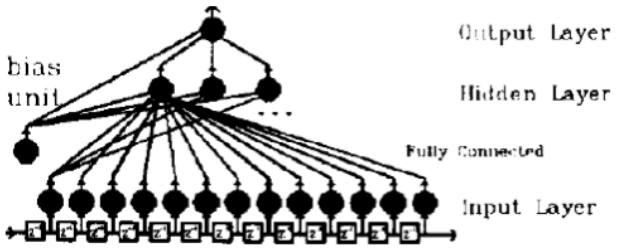

Fig. 3: Structure of neural network

IV. SIMULATION OUTPUTS OF NEURAL NETWORK USING MATLAB

A. Pulse Compressed Output

The pulse compression using neural network is performed by coding in matlab and the output after simulation is shown in Fig. 4. The output is maximum at the 13th position where the exact code match occurs.

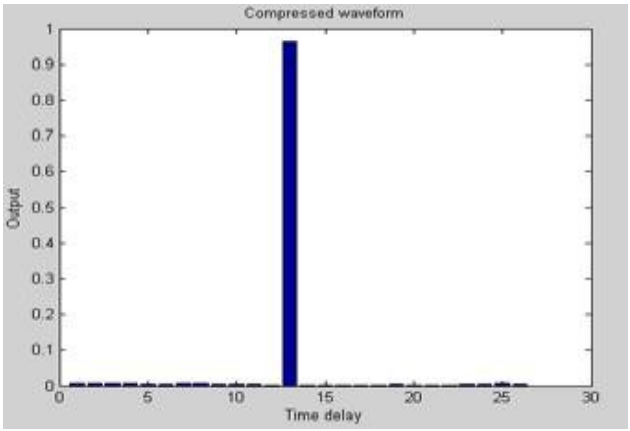

Fig. 4: Pulse Compressed output using neural network

B. Added Barker code Sequences of Same Magnitude

When input sequence is "1 1 1 2 2 0 0 2 0 -2 2 0 0 1 -1 1" a two added three delay apart barker code sequence, two peaks occur at 13th and 16th locations as shown in Fig. 5. It indicates the neural network capability to recognize mixed and delayed sequences.

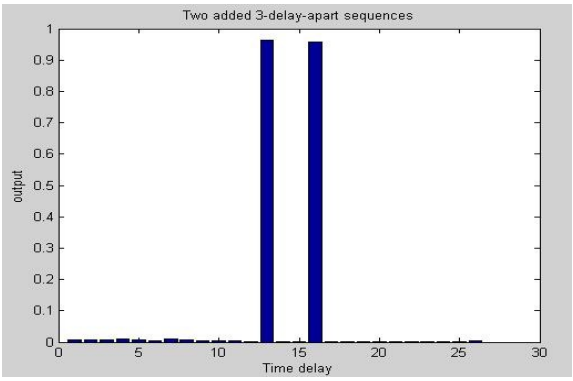

Fig. 5: Compressed waveform of two added 3-delay apart barker codes having same magnitude

C. Added Barker code Sequences of Different Magnitude

When input sequence is "0.5 0.5 0.5 1.5 1.5 0.5 0.5 1.5 -0.5 -1.5 1.5 0.5 -0.5 1 -1 1" a two added, three delay apart barker sequences of magnitude 1 and 0.5, the output will be as shown in Fig. 6.

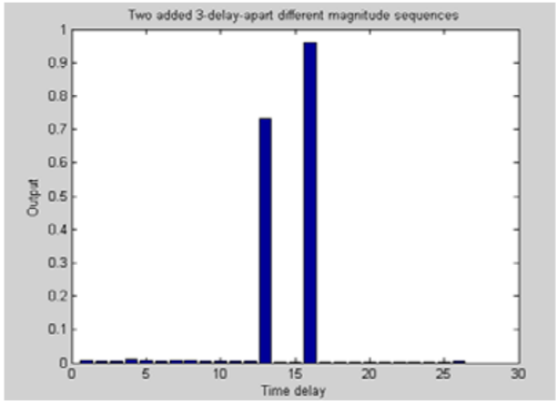

Fig. 6: Compressed waveform of two added 3-delay apart barker codes having magnitude ratio of two

The output in Fig. 6 indicates the neural network capability to recognize sequences of different magnitude which are added and also shifted.

D. Bit Discarding

When the input sequence is "1 1 1 1 1 -1 0 1 1 -1 1 -1 1" where the 7th bit of barker code is dicarded , the output is as shown in fig. 7. This indicates the neural network is tolerant to bit discarding.

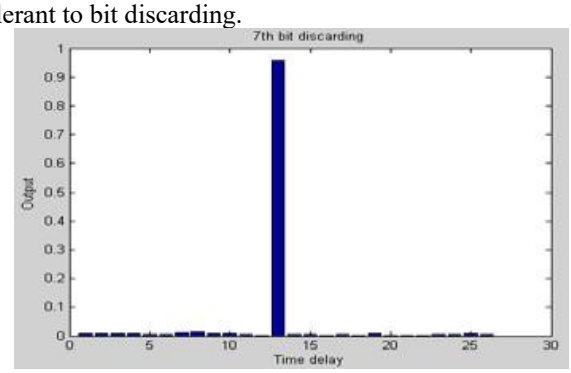

Fig. 7: Compressed waveform when 7th bit of barker code discarded

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E. Bit Duplication

When the input sequence is "1 1 1 1 1 -1 1 1 1 -1 1 -1 1" where the 7th bit is duplicated the output is as shown in Fig. 8. This indicates the fault tolerance capability of neural network because it recognizes the original sequence even after 7th bit is duplicated

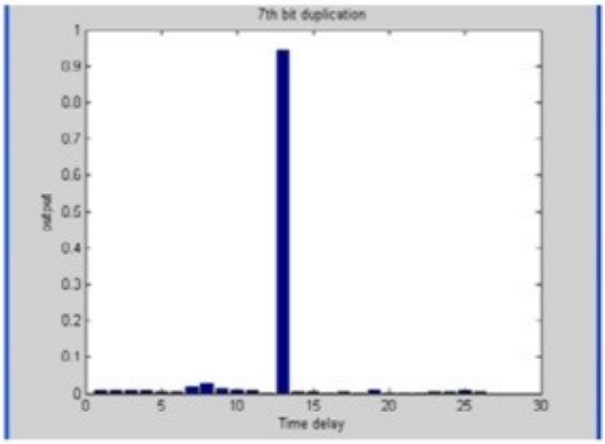

Fig. 8: Compressed waveform when 7th bit of barker code duplicated

F. Input-Output Characteristics

The input-output characteristics of neural network when the input code magnitude is varied from 0 to 1 is as shown in Fig. 9 This output shows that the output gets saturated to a value almost nearer to 1 when the input is verified from 0 to 1.

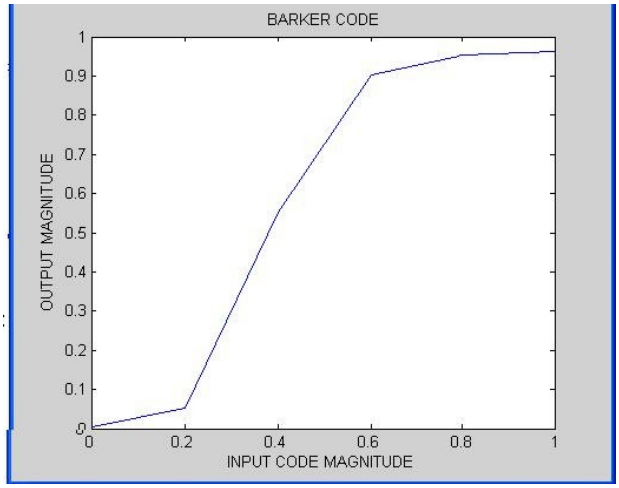

Fig. 9: Input-output characteristics

IV. SIMULATION OUTPUTS ON PROCESSOR

A. Xilinx Chip Scope Output

The simulation output of the softcore processor is obtained on the Xilinx Chip Scope, by dumping the C code designed to train the neural network, on to an embedded processor created on FPGA using Xilinx Design Suite. The output of the neural network thus obtained is as shown in Fig. 10.

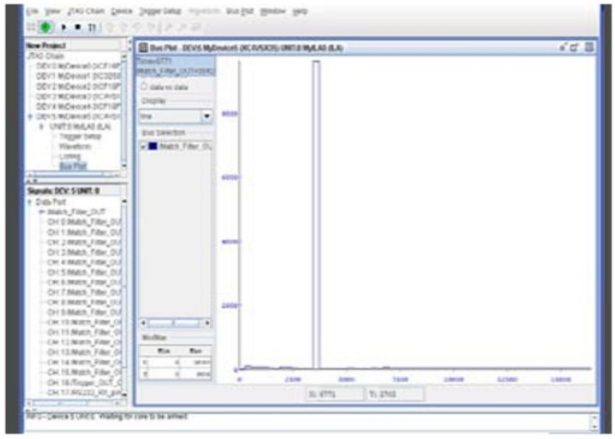

Fig. 10: Xilinx Chip Scope output

The output in figure 10 shows the successful realization of the neural network pulse compressor as it also gives the peak output at the 13th position where exact code match occurs.

B. Implementation on a Soft-core processor

The embedded processor created on the FPGA, its bus connections connection to other GPIOs and other blocks necessary for the operation are shown in the figure 10.

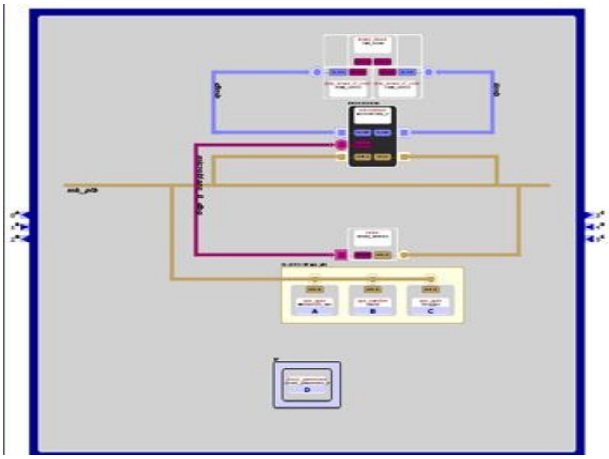

Fig.10: Processor's internal connections

V. OBSERVATIONS

By comparing the simulation outputs of the traditional FIR filter based pulse compressor to the neural network pulse compressor, it can be easily observed that, neural network approach has greater signal-to-sidelobe ratio, has high resolution capability, and is tolerant to any kind of errors or faults which are normally encountered in pulse radar detection. The neural network softcore processor implementation also proves the same.

VI. CONCLUSION

The radar pulse compression is successfully realized using neural network approach. By performing extensive

simulations, this approach is found to be much superior when compared to the traditional approaches. From the simulation output on Xilinx Chip Scope it is evident that the hardware realization of neural network is also performed successfully. In the near future, further improvements can be made by using advanced neural network architectures and also by using efficient coding techniques for radar pulse compression. The VLSI (Very Large Scale Integration) systolic array implementation of neural network can also be made possible.

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