International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

64 BIT MAC Unit Design using Multiplier & Ripple Carry Adder Using Vedic Multiplier

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Abstract—

Multiplier Accumulator Unit (MAC) is a piece of Advanced Signal Processors. The speed of MAC relies upon the speed of multiplier. The proposed MAC unit diminishes the zone by decreasing the quantity of increase and expansion in the multiplier unit. Increment in the speed of operation is accomplished by the various leveled nature of the Vedic multiplier unit. So by utilizing a productive Vedic multiplier which exceeds expectations as far as speed, power and zone, the execution of MAC can be expanded. For this quick strategy for augmentation in light of old Indian Vedic arithmetic is utilized. Among different strategy for augmentation in Vedic science, Urdhva Tiryagbhyam is utilized and the augmentation is for 64 X 64 bits. Urdhva Tiryagbhyam is a general augmentation recipe relevant to all instances of augmentation. It empowers parallel age of halfway items, kills undesirable augmentation ventures with zeros.

Keywords— MAC, Vedic Multiplier, VHDL, Ripple Carry (RC) Adder

I. INTRODUCTION

Advanced multipliers are the center segments of all Digital flag processors. The speed of DSP is to a great extent controlled by the speed of its multipliers. Increase Accumulate (MAC) operation is a generally utilized operation in different Digital Flag Processing Applications. Utilization of a Digital Signal processor can fundamentally expand the execution of a Macintosh. Regularly a duplicate gather unit comprises of a multiplier alongside an aggregator which stores past duplication items. Since framework execution generally relies upon time expected to execute the direction and duplication being the most tedious, any change to duplication will naturally enhance the framework execution. Duplication can be outlined utilizing a few calculations such as exhibit, Booth, convey spare, Modified Booth calculation and Wallace tree.In exhibit multiplier increase of two numbers can be acquired with one smaller scale operation. It is a quick technique of augmentation since the main postponement is the ideal opportunity for the signs to proliferate through the entryways. Be that as it may, it requires bigger number of doors thus it is less conservative. Another calculation is created that utilizations Vedic arithmetic. The traditional numerical calculations can be streamlined what's more, even improved by the utilization of Vedic science. The Vedic calculation is appropriate to math, trigonometric, plain and round geometry, math. The entire of Vedic arithmetic depends on 16 sutras. Here we utilize Urdhva Tiryagbhyam of Vedic arithmetic. This sutra was customarily utilized as a part of antiquated for the increase of two decimal numbers in generally less time [2]. The design of urdhva tiryagbhyam is clarified that any NxN augmentation can be effectively composed by breaking it into littler quantities of size (N/2=n) and these littler numbers can again broken into littler numbers (n/2) till we reach multiplicand size of (2 x2). Along these lines improving the entirety increase process. This

work show a precise outline procedure for quick and zone effective advanced multiplier based on Vedic science and after that a MAC unit has been made which utilizes this multiplier [5].

1.1 MAC Operation

The Multiplier-Accumulator (MAC) operation is the key operation in DSP applications as well as in media data handling and different applications. As said above, MAC unit comprise of multiplier, viper and gatherer. The MAC inputs are gotten from the memory area and given to the multiplier piece. This will be helpful in 64 bit computerized flag processor. The info which is being encouraged from the memory area is 64 bit. At the point when the information is given to the multiplier it begins registering an incentive for the given 64 bit input and henceforth the yield will be 128 bits. The multiplier yield is given as the contribution to Ripple convey snake which performs expansion. The capacity of the MAC unit is given by the accompanying condition [1]:

$$F = \text{sum}(PiQi) \ldots\ldots\ldots (1)$$

The output of Ripple carry adder is 129 bit i.e. one bit is for the carry (128bits+ 1 bit). Then, the output is given to the accumulator register. The output of the accumulator register is taken out or fed back as one of the input to the Ripple carry adder. The figure 1 shows the basic architecture of MAC unit.

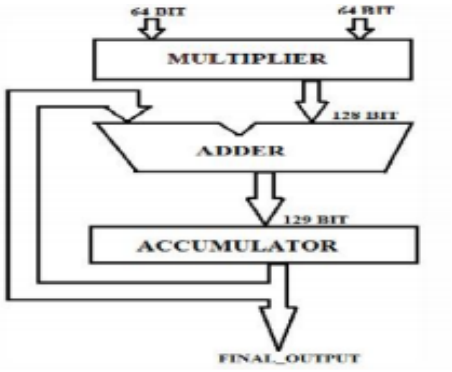

Fig 1. Basic architecture of MAC unit

II. VEDIC MATHEMATICS PRINCIPLE

Vedic mathematics is the name given to the ancient system of mathematics, which was discovered between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The word "Vedic" is derived from the word "Veda" which means the store house of all knowledge. The Vedic mathematics is based on 16 sutras which deal with various branches of mathematics. These sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The possible multiplier architecture of Vedic mathematics to be designed on DSP applications is Urdhva Tiryagbhyam. Traditional Indian mathematicians used this sutra to do multiplication of two decimal numbers in less time. It multiplies the number in the vertical and crosswise fashion. It is applicable to all cases of multiplication [3].

2.1 Urdhva Tiryagbhyam Sutra

Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. "Urdhva" and "Tiryagbhyam" words are derived from Sanskrit literature. It literally means "vertical and crosswise". The method of urdhva tiryagbhyam is explained that any NxN

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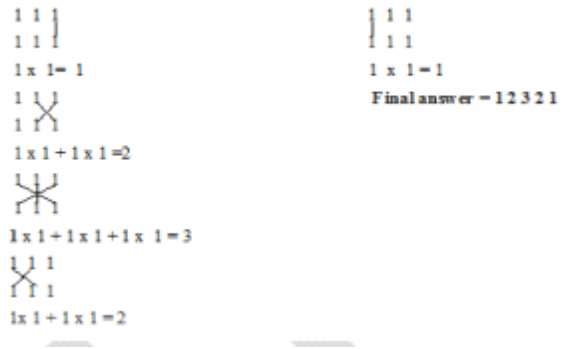
multiplication can be efficiently designed by breaking it into smaller numbers of size (N/2=n) and these smaller numbers can again broken into smaller numbers (n/2) till we reach multiplicand size of (2 x2). Thus simplifying the whole multiplication process . Ex.1. the product of 111 and 111 using Urdhva Triyakbhyam (vertically and crosswise) is given below. Methodology of Parallel Calculation



III. MULTIPLIER ARCHITECTURE

Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

3.1 Vedic Multiplier for 2x2 bit Module

The technique is clarified underneath for two, 2 bit numbers An and B where A = a1 a0 and B = b1 b0 as appeared in Fig. 2. Initially, the minimum huge bits are duplicated which gives the slightest huge piece of the last item (vertical). At that point, the LSB of the multiplicand is increased with the following higher piece of the multiplier and included with, the result of LSB of multiplier what's more, next higher piece of the multiplicand (across). The whole gives second piece of the last item and the convey is included with the incomplete item acquired by increasing the most critical bits to give the entirety and convey. The total is the third relating bit and convey turns into the fourth piece of the last item.

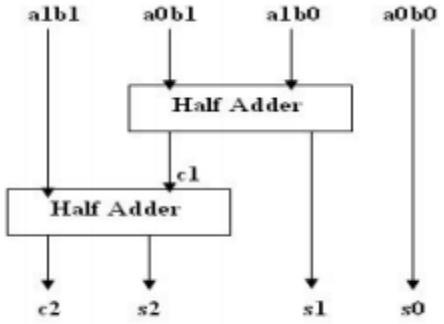


Fig 2 : Block Diagram of 2x2 bit Vedic Multiplier

3.2 Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier module is designed using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let's analyze 4x4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7 S6 S5 S4 S3 S2 S1 S0 Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3 B2 & B1 B0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig. 3. Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1A0 and B1B0. The last block is 2x2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1 B0 and A1 A0 & B3 B2. So the final result of multiplication, which is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0 and three 4-bit Ripple-Carry (RC) Adders are required. The proposed Vedic multiplier can be used to reduce delay. On the

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other hand, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 3, helps us to reduce delay.

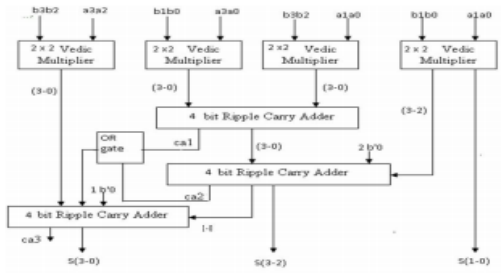

Fig 3 : Block Diagram of 4x4 bit Vedic Multiplier

3.3 Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 4 can be easily designed by using four 4x4 bit Vedic multiplier. Let's analyze 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5 B4 B3 B2 B1 B0. The output line for the multiplication result will be of 16 bits as – S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0. Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

P = A x B = (AH-AL) x (BH-BL)

= AH x BH + (AH x BL + AL x BH) + AL x BL

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 4.

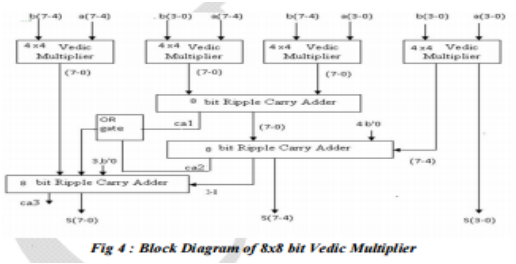

Fig 4 : Block Diagram of 8x8 bit Vedic Multiplier

3.4 Vedic Multiplier for 16x16 bit Module

The 16x16 bit Vedic multiplier module as shown in the block diagram in Fig. 5 can be easily designed by using four 8x8 bit Vedic multiplier. The 16x16 multiplications, say A= A15 A14 A13 ……..A3 A2 A1 A0 and B= B15 B14 B13..... B3 B2 B1 B0. The output line for the multiplication result will be of 32 bits as – S31 S30 S29 S28 ……. S3 S2 S1 S0. Let's divide A and B into two parts, say the 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. Using Vedic multiplication, taking four bits at a time and using 8 bit multiplier block . The outputs of 8x8 bit multipliers are added accordingly to obtain the final product. Here total three 16 bit Ripple-Carry Adders are required as shown in Fig. 5.

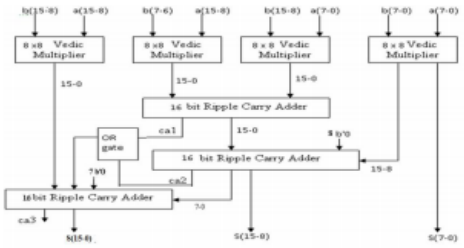

Fig 5: Bblock Diagram of 16x16 bit Vedic Multiplier

3.5 Vedic Multiplier for 32x32 bit Module

The 32x32 bit Vedic multiplier module as shown in the block diagram in Fig. 6, it can be designed by using four 16x16 bit Vedic multiplier modules as discussed. Let's analyze 32x32 multiplications, say A= A31 A30 A29 A28…….. A3 A2 A1 A0 and B=

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B31 B30 B29 B28……. B3 B2 B1 B0. The output line for the multiplication result will be of 64 bits as – S63 S62 S61 S12……..S4 S3 S2 S1 S0. Let's divide A and B into two parts, say the 32 bit multiplicand A can be decomposed into pair of 16 bits AHAL. Similarly multiplicand B can be decomposed into 16 bits BH-BL. The outputs of 16x16 bit multipliers are added accordingly to obtain the final product. Here total three 32 bit Ripple-Carry Adders are required as shown in Fig. 6.

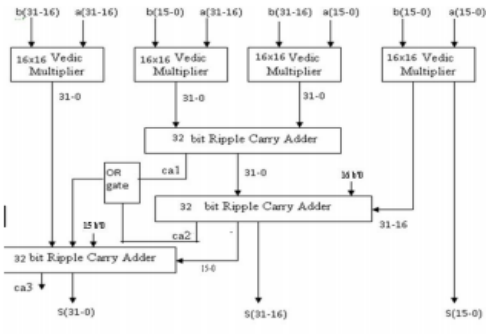

Fig 6 : block Diagram of 32x32 bit Vedic Multiplier

3.6 Vedic Multiplier for 64x64 bit Module

The 64x64 bit Vedic multiplier module as shown in the block diagram in Fig. 7 by using four 32x32 bit Vedic multiplier. The 64x64 multiplications, say A= A63 A62 A61 A60……. A3 A2 A1 A0 and B= B63 B62 B61 B60……. B3 B2 B1 B0. The output line for the multiplication result will be of 128 bits as – S128 S127 S126 S125…… S3 S2 S1 S0. Let's divide A and B into two parts, say the 64 bit multiplicand A can be decomposed into pair of 32 bits AH-AL. The multiplicand B can be decomposed into 32 bits BH-BL. The outputs of 32x32 bit multipliers are added accordingly to obtain the final product. Here total three 64 bit Ripple-Carry Adders are required as shown in Fig. 7.

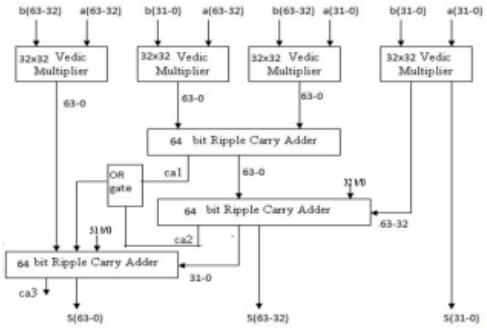

Fig 7 : block Diagram of 64x64 bit Vedic Multiplier

IV. LITERATURE REVIEW

In 2013 P. Jagadeesh, Mr.S.Ravi and Dr. Kittur Harish Mallikarjun, "Design of High Performance 64 bit MAC Unit" in this paper designed of high performance 64 bit Multiplierand Accumulator (MAC). The total MAC unit operates at a frequency of 217 MHz. The total power dissipated by 64 bit MAC unit is 177.732 mW. The total area occupied by it is 542177 11m2. Since the delay of 64 bit is less, this design can be used in the system which requires high performance in processors involving large number of bits of the operation. The MAC unit is designed using Verilog-HDL and synthesized in Cadence 180nm RTL Complier.

In 2013 Shishir Kumar Das, Aniruddha Kanhe, R.H. Talwekar, "Design and Implementation of High performance MAC Unit" in this paper implemented 32 bit IEEE 754 Floating point multiplier based on Vedic Multiplication technique. These multipliers are implemented using VHDL. In order to get the power and delay report the multipliers are synthesized using Xilinx ISE tool and Spartan 2E FPGA is used. They gives simulation result of multipliers with Vedic Multiplier on basis of time delay and power.

In 2013 Sreelekshmi M. S., Farsana F. J., Jithin Krishnan3, Rajaram S, Aneesh R,

"Implementation of MAC by using Modified Vedic Multiplier"in this paper they observed that for 16x16 Vedic multiplier the delay obtained is 21.4ns. Model sim is used for simulation and synthesis of the Vedic multiplier is carried out using Xilinx ISE 10.1. The delay of 16x16 Vedic multiplier is 21.4ns with nearly 8% device utilization.(number of slices: 508 out of 704) and number of 4 input LUTs: 98 out of 1408(6%). The number of bonded IOBs: 28 out of 108(25%).

V. SIMULATION RESULT

The 64x64 multiplier is outlined utilizing model sim for reenactment and union of the vedic multiplier is done utilizing Xilinx ISE 13.1 on Spartan 7A. Thus the proposed multiplier engineering is discovered most proficient as far as speed.

Table 1. SYNTHESIS RESULT

Name of multiplier	Number of Slice LUTs	Number of fully used FF pairs	Number of bonded IOBs
64 bit	178800 (available) used 9900.	9900 (available) used 0.	600 (available) used 256.
32 bit	178800 (available) used 2412.	2412 (available) used 0.	600 (available) used 128.
16 bit	178800 (available) used 574.	574 (available) used 0.	600 (available) used 64.
8bit	178800 (available) used 129.	129 (available) used 0.	600 (available) used 32.
4bit	178800 (available) used 25.	25 (available) used 0.	600 (available) used 16.
2bit	178800 (available) used 4.	4 (available) used 0.	600 (available) used 8.

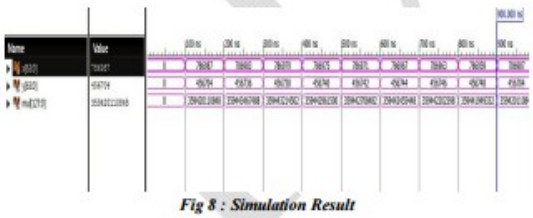

Fig 8 : Simulation Result

VI. CONCLUSION AND FUTURE WORK

Urdhva Tiryagbhyam Sutra is very productive calculation for augmentation. The plan of 64x64 piece Vedic multiplier has been acknowledged on Spartan 7A. The calculation delay got for 64x64 piece Vedic multiplier having an aggregate deferral of 42.98ns containing rationale defer 3.405ns and course postpone 39.578ns. This indicates change in execution.

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