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Implementation of Low power Baugh-Wooely Multiplier and Modified Baugh Wooely Multiplier Using Cadence (Encounter) RTL in DSM Technology

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Abstract *— excessive speed, low electricity consumption are key requirement to any VLSI layout. The power green multipliers play an vital role. This paper provides an efficient implementation of a excessive pace, low energy multiplier the use of shift and adds methods of Baugh Wooely Multiplier. This observe offered the design and implementation of Baugh wooely multipliers the usage of Cadence (stumble upon) RTL Complier. in this work, modified Baugh Wooely is having least vicinity, strength and put off. The changed Baugh wooley structure is 109X faster than traditional array multiplier and 102X quicker than conventional Baugh Wooley. The working frequency of five x five design changed Baugh Wooley multiplier is 160MHz. the choice of Multiplier need to be finished relying on performance degree and alertness nature.*

Kkey words— Baugh Wooely, Cadence, Low strength Multiplier, RTL Complier.

I. INTRODUCTION

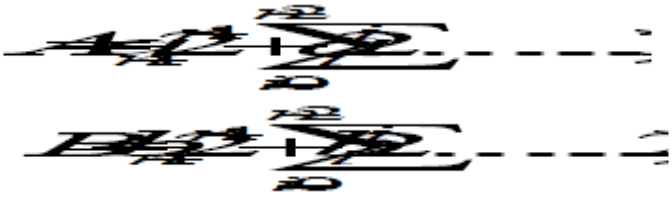
The increasing prominence of portable gadget and the need to restriction energy intake in very excessive density united states of america chips have caused fast and revolutionary developments in low electricity layout. The want for low energy layout is turning into a main problem in high overall performance digital systems, along with microprocessor, virtual sign processing and other packages. As needs for portable computing and conversation are developing, the strength efficient multiplier performs an essential role in Very massive Scale Integration (VLSI) device design. Multiplication is one of the critical operation in lots of algorithm used in virtual sign Processing (DSP). A number one requirement of high overall performance digital system is high velocity multiplication. in lots of cases multiplier can be present in crucial direction and pace of processing is in the long run get reduced by way of speed of multiplication. The Multiplier algorithm is also one of the predominant contributors to the total power dissipation. lowering the power dissipation is key criteria in design of multiplier. power ate up by using multipliers may be reduced at various stages of the design from set of rules to architectures to circuit [15]. The center of any processor is the arithmetic and good judgment unit (ALU). The ALU combines the addition and subtraction with other operation. The addition and subtraction of numbers are the basic operation in all digital computer systems. those operations arise on the device instruction stage and are applied using the simple common sense gates in arithmetic and common sense unit (ALU) subsystem of the microprocessor. The time had to carry out these operations influences the performance of processors. Multiplication is one of the crucial operations which calls for more complex circuitry than addition/subtraction operations. Multiplications are high priced and sluggish operations. in many computational problems the performance is ruled by means of the rate at which a multiplication operation may be

done. Multipliers are complex adder arrays. Multiplication consists of three basic operations: the generation of partial product, discount of partial products, final deliver propagate summation [21]. thinking about the timing constraints, devoted multipliers hardware implementations together with array multiplier had been delivered. Variable length partial product arrays aren't realistic for multiplier design and considering the fact that a extra state-of-the-art techniques had been proposed. The changed sales space recoding scheme is one of the more famous implementation. The benefit of modified sales space recoding set of rules is that, it reduces the number of generated partial products through 1/2. Bit pair recoding of the multiplier derivedfrom booth algorithm, reduces the number of summands through a aspect 2. these summands can then be decreased to simplest two By means of the use of a fairly small range of carry store addition steps. The very last product can be generated via an addition operation that uses a deliver look ahead adder [19]. The partial sum adders may be rearranged in a tree like style, decreasing both the crucial course and the quantity of adder cells required e.g wallace tree multiplier, Dadda. because of irregular shape, it's far tough to vicinity and path for the duration of the layout of a multiplier. A reduced length of the reduction circuit eases the implementation and improves the overall performance of the multiplier [12]. There are a number of techniques that can be used to perform multiplication. the choice is primarily based upon factors such as latency, throughput, vicinity and design complexity. greater green parallel technique uses a few type of array or tree of complete adders to sum the partial merchandise. The wide variety of partial merchandise to sum may be decreased using booth Encoding and the variety of good judgment stages required to carry out the summation may be decreased with Wallace bushes. Wallace trees are complicated to layout and have lengthy abnormal wires, so hybrid structures may be more attractive. Multiplications are highly-priced and sluggish operation. essentially multiplication manner can be regarded to consist of following steps (1) assessment of partial product (2) Accumulation of the shifted partial product. therefore, quicker manner to put into effect multiplication is to lodge to an method much like manually computing a multiplication. all of the partial merchandise are generated at identical time and prepared in an array. A less variety of partial products additionally reduces the complexity and as a result will increase the rate to build up the partial products. both answers can be applied simultaneous. In [1], complete custom flow of Wallace-Tree, Array and Baugh Wooley multiplier is carried out the usage of low electricity design techniques. In layout the parallel multipliers,the quantity of partial merchandise to be added is the key parameter which determines the performance of multiplier. In [2] comparative take a look at of modified booth Multiplication and Baugh Wooley Multiplier is performed. The 32 bit multiplier the usage of 65nm and 130nm is designed and simulated using Cadence software. in line with [11] for a 32 bit multiplier, a modified sales space implementation has large electricity dissipation, region and simplest small development in delay compared to Baugh Wooely multiplier implementation. The [3] affords an green high speed multiplier Baugh Wooely multiplier. In [3], the observe of 4 bit pipelined multiplier is presented and carried out in VHDL. The parallel multiplier uses less quantity of adders, as end result of less space is occupied as compared to serial multiplier. The main standards within the chip fabrication and high performance device calls for that factor should be as small as viable. Baugh

wooley 's compliment signed multipliers is the best known set of rules for signed multiplication because it maximizes the regularity of the multiplier and permit all the partial merchandise to have effective signal bits. Baugh Wooely technique became advanced to layout direct multiplies for twos praise numbers. A Baugh Wooely multiplier become used for twos compliment multiplication due to its efficiency in coping with signed bits. The principle gain is that sign of all of the partial merchandise bits are high-quality permitting the product to be fashioned the usage of array addition techniques. In traditional twos complement multiplication there are partial product bits with terrible as properly as tremendous symptoms. The [4] provides the implementation of electricity green BaughWooely multiplier the use of FPGA Spartan 3 tool. The velocity, strength and location have a widespread effect as consistent with the specific programs and efficient attention of the multiplication is critical. The Spartan 3 AN FPGA device can be used to construct fundamental block reasonably. Many DSP set of rules needs the use of application unique integrated circuits. The computation time may be speedup through assigning computation extensive responsibilities to hardware and via exploiting the parallelism in algorithms. In [5], 16 X sixteen bit multiplier is layout and carried out. while the numbers are inside the 2's supplement form, the design of iterative arrays will become tough because the signal bit is embedded inside the wide variety itself. the two scheme which reduces those problems are the Pezaris and Baugh Wooely set of rules.The Pezaris, uses extraordinary forms of cells whilst Baugh Wooely set of rules requires real and complemented shape of each numbers. The power ate up via multipliers may be reduced at numerous tiers of the design from algorithms to architectures to circuit and tool level. Reference [8]- [12] offers a appropriate interior into the trouble and design optimizations in any respect the hierarchy tiers.

II. BAUGH WOOELY TWO'S COMPLEMENT SIGNED MULTIPLIER

When the operands are in two's complement form, the design of iterative arrays becomes more difficult since the sign bit is embedded in the number itself. Direct two's complement multiplication arrays have been proposed where the cells used are either more complex or the number of cells is significantly larger than for the positive-number multiplier array [16]. Baugh and Wooley modified the multiplication matrix into a form that contains only positively weighted partial products. To accomplish this, both the true and complement values of the operands are needed. There is also a slight increase in the number of adding cells and in the multiplication time. The resulting array, however, uses only Type 0 full adder cells. This uniformity is particularly advantageous for LSI implementation. Multiplying two 2's complement numbers. Let us consider two n-bit numbers A and B can be represented as



Where the and are the bits in A and B respectively and and are sign bits. The product P=A x B is then given by the following equation.

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$$P = A*B = (a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i)*(b_{n-1}2^{n-1} + \sum_{j=0}^{n-2} b_j 2^j$$

$$= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j}$$

$$- 2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1} 2^i - 2^{n-1}\sum_{j=0}^{n-2} a_{n-1} b_j 2^j \quad \ldots\ldots\ldots 3)..(3$$

Above equation indicates that the find product is obtained by subtracting the last two positive terms from the first two terms. One important complication in the development of the efficient multiplier implementation is the multiplication of two's compliment signed numbers. Baugh Wooley two's compliment signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits Baugh and Wooley have proposed an algorithm for direct two's complement array multiplication. The principal advantage of their algorithm is that the signs of all summands are positive, thus allowing the array to be constructed entirely with conventional type 0 full adders, whereas Pazaris two's complement multiplier uses mixture types of full adders. The Baugh Wooley algorithm is a relatively straightforward way of doing signed multiplications when multiplying two's complement number directly each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by Carry Save Adder(CSA) tree.

According to Baugh Wooley approach, an efficient method of adding extra entries to the bit matrix is suggested to avoid having to deal with the negatively weighted bits in partial product matrix. In equation (write equation no here), rather than doing a subtraction operation, we can obtain the 2's complement of the last two term and add all terms to get the final product. The last two terms are n-1 bits each that extend in binary weight from position 2^{n-1}up to 22^{n-3}. On the other hand, the final product is 2n bits and extends in binary weight from 20 upto 22^{n-1}. We pad each of the last two terms in equation 4 with zero's to obtain a 2n-bit number to be able to add them to the other terms. The padded terms extend in binary weight from 20 upto 22^{n-1}. The 2n-bit full precision product PFP can be written as

$$P_{FP} = X*Y = (x_{n-1}y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} x_i y_j 2^{i+j} +$$

$$2^{n-1}(-2^{n-1} + \sum_{j=0}^{n-2} \overline{x_{n-1}y_j}2^j + 1) +$$

$$2^{n-1}(-2^{n-1} + \sum_{i=0}^{n-2} \overline{y_{n-1}x_i}2^i + 1)) \quad \ldots\ldots\ldots\ldots\ldots 4)$$

Equation 4 shows the Baugh Wooley algorithm [13].The schematic circuit diagram of a 5-by-5 Baugh-Wooley array multiplier is shown in Figure 1.

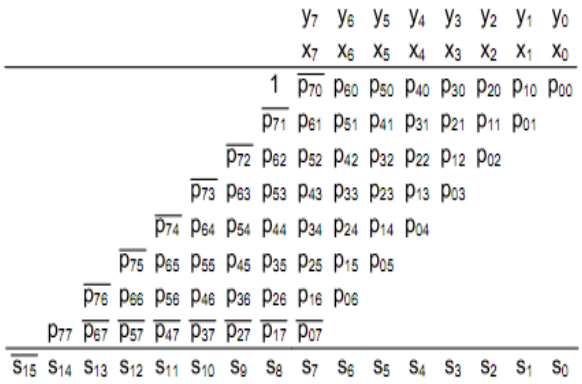

Figure 1: Schematic Circuit Diagram of a 5-by-5 Baugh- Wooley Array Multiplier

Example of Baugh-Wooley Algorithm

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					0	1	1	0	0	(12)(Multiplicand)
					0	0	1	1	0	(6)(Multiplier)
					0	0	0	0	0	
				0	1	1	0	0	x	
			0	1	1	0	0	x	x	
		0	0	0	0	0	x	x	x	
	0	0	0	0	0	x	x	x	x	
	1				0					
1	1				0					
0	0	0	1	0	0	1	0	0	0	(72)

					1	0	1	0	0	(-12)(Multiplicand)
					1	1	0	1	0	(-6)(Multiplier)
					1	0	0	0	0	
				0	0	1	0	0	x	
			1	0	0	0	0	x	x	
		0	0	1	0	0	x	x	x	
	1	1	0	1	1	x	x	x	x	
	0				1					
1	0				1					
0	0	0	1	0	0	1	0	0	0	(72)

					1	0	1	0	0	(-12)(Multiplicand)
					0	0	1	1	0	(6)(Multiplier)
					1	0	0	0	0	
				0	0	1	0	0	x	
			0	0	1	0	0	x	x	
		1	0	0	0	0	x	x	x	
	0	0	0	0	0	x	x	x	x	
	0				1					
1	1				0					
1	1	1	0	1	1	1	0	0	0	(-72)

					0	1	1	0	0	(12)(Multiplicand)
					1	1	0	1	0	(-6)(Multiplier)
					0	0	0	0	0	
				0	1	1	0	0	x	
			0	0	0	0	0	x	x	
		0	1	1	0	0	x	x	x	
	0	0	0	1	1	x	x	x	x	
	1				0					
1	0				1					
1	1	1	0	1	1	1	0	0	0	(-72)

III. MODIFIED BAUGH WOOLEY MULTIPLIER

Conventional Baugh Wooley Multiplier method increases the height of the longest column by two, which may lead to a greater delay through the carry save adder tree. As shown in Tabular bit form 4.3, column height is 7, requiring an extra carry save adder level. Removing b4from the fourth column and writing into b4entries in the third column, which has only four entries, can reduce the extra delay. Thus, the maximum number of entries in one column becomes six. All negatively weighted a4b4terms can be transferred to the bottom row, which leads to two negative numbers in the last two rows, where a subtraction operation from the sum of all the positive elements is necessary. Instead of subtracting a4b4 two's complement of a can be added b4times. This method is known as the Modified Baugh Wooely Algorithm. Fig. 2 shows the schematic diagram of Modified Baugh Wooely algorithm for 5 X 5 bit multiplier.

	a_4	a_3	a_2	a_1	a_0	A(Multiplicand)
	b_4	b_3	b_2	b_1	b_0	B(Multiplier)
			$\overline{a_4b_0}$	a_3b_0	a_2b_0	a_1b_0	a_0b_0
		$\overline{a_4b_1}$	a_3b_1	a_2b_1	a_1b_1	a_0b_1	
	$\overline{a_4b_2}$	a_3b_2	a_2b_2	a_1b_2	a_0b_2		
$\overline{a_4b_3}$	a_3b_3	a_2b_3	a_1b_3	a_0b_3			
a_4b_4	$\overline{a_3b_4}$	$\overline{a_2b_4}$	$\overline{a_1b_4}$	$\overline{a_0b_4}$			
1			1				
p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

Figure 2: The Schematic Circuit Diagram of a 5-by-5 Modified Baugh-Wooley array multiplier.

IV. SIMULATION RESULTS AND DISCUSSION

The code for multiplier is written in Verilog language. The RTL Compiler is used to compile the code. The Encounter (cadence) software is used for floor planning, power planning and routing purpose [22]. The functionality of the schematic is verified using Virtuoso (cadence) software. The major part of the design entry was done at the transistor

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schematic level. The layout where done in an attempt at estimating the area of the multiplier. Designs were entered using Cadence RTL compiler, using Encounter floor-planning, power-planning and routing is carried out. Cadence Virtuoso for pre layout and post layout simulation is using targeting NCSU AMI06 CMOS technology.

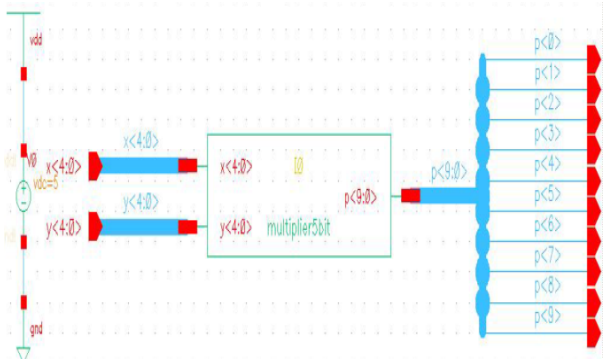

Figure 3: Test Bench Circuit for Simulation

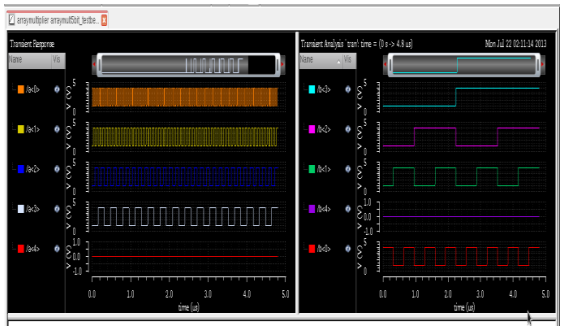

Figure 4: Functionality Proof: Two's Complement Array Multiplier Input Wave form

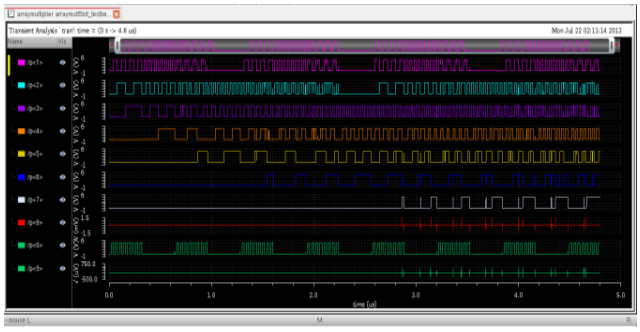

Figure 5: Functionality Proof: Two's Complement Array Multiplier Output Wave form

Figure 4 and Figure 5 show the input and output waveform of array multiplier. To verify the functionality of multiplier, the Analog Design Environment (ADL) is used.

When two numbers are negative, it will be in two's complement form. The two's complement of each is taken to convert it to a positive number, and then the two numbers are multiplied. The product is kept as a positive number and is given a sign bit of 0. Figure 6 and Figure 7 shows the input and output waveform of multiplication for two negative numbers. The resultant waveforms are compared with the test bench vectors written.

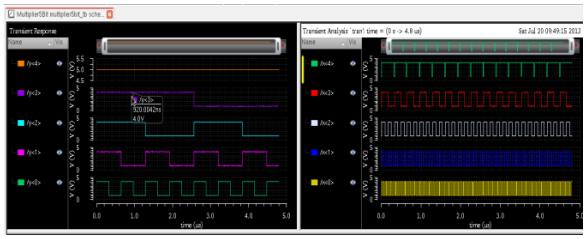

Figure 6: Functionality Proof: Baugh Wooely Multiplier Input Wave form: X- Negative Y-Negative

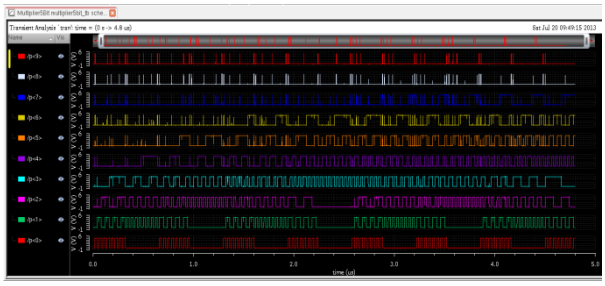

Figure 7: Output Waveform: X- Negative Y-Negative

TEST BENCH

The Test Bench is designed such that it can provide a series of stimuli to the Multiplier and vector (.vec) the results obtained. Simulation Result Files contains the multiplicand and multiplier sent to the Multiplier as well as the result received. In order to quickly validate the results, an automatic comparison is performed

between the theoretical results and the experimental results. A block diagram of the Test Bench architecture is shown in Figure 8.

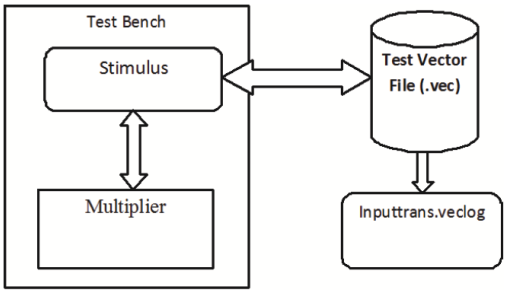

Figure 8: Test Bench Simulation Block Diagram

TEST VECTOR REPORT: The Test Bench is designed such that it can provide a series of stimuli to the Multiplier and vector (.vec) the results obtained. The Vector (.vec) file, included in Appendix B. Simulation Result Files contains the multiplicand and multiplier sent to the Multiplier as well as the result received. In order to quickly validate the results, an automatic comparison is performed between the theoretical results and the experimental results.

****VectorCheck for $p < 0 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 175
Number of One's matched correctly	= 64
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 1 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 143
Number of One's matched correctly	= 96
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 2 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 127
Number of One's matched correctly	= 112
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 3 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 119
Number of One's matched correctly	= 120
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 4 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 107
Number of One's matched correctly	= 132
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 5 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 99
Number of One's matched correctly	= 140
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 6 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 79
Number of One's matched correctly	= 160
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 7 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 46
Number of One's matched correctly	= 193
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 8 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 14
Number of One's matched correctly	= 225
Number of total states matched correctly	= 239
Number of total errors	= 0
****VectorCheck for $p < 9 >$: All good!	
Number of total vector checks	= 239
Number of X's matched correctly	= 0
Number of Zero's matched correctly	= 14
Number of One's matched correctly	= 225
Number of total states matched correctly	= 239
Number of total errors	= 0

Figure 9: Test vector report : Both Numbers are Negative

Delay Analysis (worst path)

check in transfer level (RTL) Timing evaluation (RTA) can provide accurate timing evaluation of designs as early as viable within

the layout cycle. acting timing analysis at the check in switch level (RTL) stage is faster and lots more cost powerful than ready to discover the same issues at some point of timing evaluation at the gate-level or format-degree. discern 10 suggests the worst case path for changed Baugh Wooley Multiplier. If Slack time is advantageous, the device is indicating that the signal arrives on the check in on the proper a great deal in advance than is needed. which means the circuit can work with a miles higher clock frequency. As shown in discern 10, the route from enter bit x[1] to output bit p[8] is having more delay compare to other. the entire put off of worst case course is 6.219ns. The maximum clock frequency of the multiplier is 160MHz. If slack time turns into terrible, then circuit does now not meet timing. One has to find the most clock frequency upto which slack time is high-quality i.e. near to at least one. table five.6 indicates the overall performance measures for various multiplier architectures. it's far observed that the changed Baugh Wooley multiplier is 1.five instances quicker than conventional Baugh Wooley multipler.

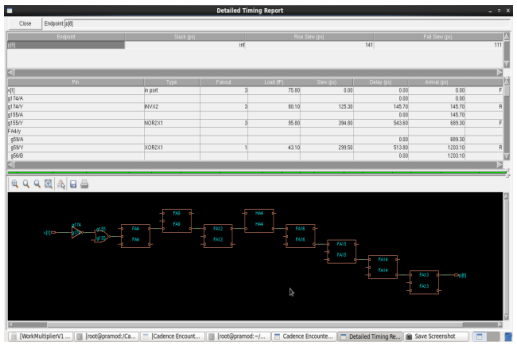

Figure 10: Timing Report: Worst Path Delay

Table 1: Comparison of various Multipliers

Multiplier Type	Power Dissipation (mW)	Area (μm^2)	Delay (ns)
Array Multiplier (Conventional)	8.909	83160	8.693
Baugh Wooely Multiplier	10.88	87912	9.62
Modified Baugh Wooely Multiplier	10.17	62646	6.219

publish layout Simulation

the electrical performance of a complete-custom design can be exceptional analyzed by means of performing a post-format simulation on the extracted circuit internet-list. The special (transistor-level) simulation executed the use of the extracted netlist will offer a clear assessment of the circuit velocity, the affect of circuit parasitic together with parasitic capacitances and resistances. After perform the LVS (layout vs. Schematic), RC extraction of the design is done to locate parasitic (resistance and capacitance) to carry out publish layout simulations. figure eleven indicates the RC extracted diagram. desk 2 suggests the strength intake of modified Baug Wooley Multiplier for the (check Vector case: each Numbers are high-quality) pre-format and put up-layout simulation. In digital circuit, energy intake is accelerated in physical format layout because of parasitic additives.

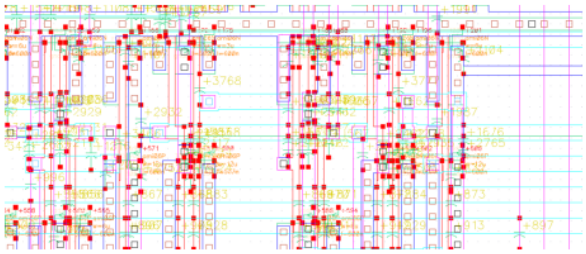

Figure 11: RC Extracted View of 5 Bit Modified Baugh Wooley Multiplier

Table 2: Comparison of Power Pre and Post Layout

	Pre layout (mW)	Post Layout (mW)
Modified Baugh Wooely Multiplier	7.36	7.47

V. CONCLUSION

An five-bit signed multiplier become layout the usage of cadence IC615 the usage of

NCSU ami06, format them in encounter with the aid of cadence and the evaluation of common dynamic strength dissipation became achieved. The changed Baugh wooley structure is 109X quicker than traditional array multiplier and 102X faster than traditional Baugh Wooley. Baugh Wooley consumes more strength compared to standard Baugh Wooley. strength can be further reduce by means of enforcing the design the usage of trendy technological node together with 45nm, 65nm and so on we are able to summarized some of the critical layout principles as 1. select the proper shape earlier than beginning an elaborate circuit optimization. 2. decide the crucial timing course via the circuit. 3. strength and velocity can be traded off thru a preference of circuit sizing, supply voltage and transistor thresholds. there's exceptional scope in layout of multiplier in one-of-a-kind architectures. The Baugh Wooley is used for 2's supplement signed multiplication. There are different architectures for two's complement signed multiplications. The identical may be applied using cutting-edge generation node together with 22nm, 32nm, 45nm so that you can reduce power and increase the speed.

REFERENCES

[1] P.V. Rao, C Prasanna Raj, S. Ravi, "VLSI Design and Analysis of Multipliers for Low Power", Fifth International Conference on Intelligent Information Hiding and Multimedia Signal Processing",2009.PP-1354-1357.

[2] M. Sjlander and P. Larsson-Edefors, "High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree",Department of Computer Science and Engineering, Chalmers University of Technology, March 2008.

[3] P. Mohanty, R.Ranjan, "An Efficient Baugh-Wooley Architecture & Unsigned Multiplication", International Journal of Computer Science & Engineering Technology (IJCSET),Vol. 3 No. 4 April 2012,pp-94-99.

[4] M. H. Rais, B. M. Al-Harthi, Saad I. Al-Askar and Fahad K. Al-Hussein,"Design and Field Programmable Gate Array Implementation of Basic Building Blocks for Power Efficient Baugh-Wooley Multipliers",American J. of Engineering and Applied Sciences 3 (2): 307-311, 2010.

[5] R. Bajaj, S. Chhabra, S. Veeramachaneni and M B Srinivas, "A Novel, Low-Power Array Multiplier Architecture",International Institute of Information Technology-Hyderabad.

[6] R. B and H. M Kittur, "Faster and Energy Efficient Signed Multipliers", School of Electronics Engineering, VIT University.

[7] N. Bandeira, K. Vaccaro, And J. A. Howard, "A Two's Complement Array Multiplier Using True Values of the Operands",IEEE Transactions On Computers, VOL. c-32, NO. 8, August 1983.

[8] J Rabaey, A Chandrakasan, B Nikolic, "Digital Integrated Circuits A Design Perspec tive, 2nd Ed., New Jersey : Prentice-Hall Inc, c2003.

[9] Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design- A Circuit and Systems Perspective", Pearson, 2006,pp.345-357.

[10] Carl Hamacher, Zvonko Vranesic, Safwat Zaky," Computer Organization",Tata McGraw Hill,2011,pp.376-390.

[11] Wayne Wolf, (2002). Modern VLSI Design: System-On-Chip Design. 3rd Edition, Pren tice Hall, Upper Saddle River, N.J.

[12] Partha Sarathi Mohanty,"Design And Implemnetation Of Faster And Low Power Multipliers", Department Of E & TC, NIT,Rourkela, 2009.

[13] Erik Brunvand,"Crafting a Chip A Practical Guide to the UofU VLSI CAD Flow",School of Computing,University of Utah,August 24, 2006, PP-292-335.

[14] Cadence Design Systems. [Online]. Available: http://www.cadence.com