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Design of Dual Fault Tolerant Parallel Ffts Using Parseval Checks

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ABSTRACT: *Presently, the circuits of communication and signal processing became more difficult. This is due to the CMOS technology scaling in which more transistors is integrated on a single device. The transistors which are operated with low voltages are known as scaling. These are more liable to the errors caused by the noise and manufacturing variations. Errors cause the reliability risk for advanced electronic circuits. Algorithm Based Fault Tolerance (ABFT) technique is used to utilize the algorithmic properties. FFTs are the major key building blocks in every system. Perseval or sum of square check is one of the techniques which are most extensively used. A technique has been proposed which utilizes this reality to implement fault tolerance on parallel filters. Initially, this technique is applied to secure the FFTs. Therefore, two protection schemes are proposed and evaluated which unify the usage of Error Correction Codes (ECC) and Parceval checks.*
Index terms: Error Correction Codes (ECC), Fast Fourier Transforms (FFTs), Soft Errors.

1. INTRODUCTION

In Communication and Signal processing systems the complexity of the circuits increases. This is made feasible by the scaling of CMOS technology. Scaling means the transistor operates with low voltages and more sensitive to the errors which are caused by the noise and manufacturing variations. Soft errors can change the logical value of a circuit node.

This creates a temporary error that can affect the operation of a system. Various techniques are used to verify the soft errors. These techniques include the particular manufacturing processes for Integrated Circuits like Silicon On Chip (SOC). Other option is to design basic circuit blocks for minimizing the probability of soft errors. Hence, it is possible to add redundancy for detecting and correcting the errors at the system level.

Another example is to use Triple Modular Redundancy (TMR). This technique triples a block and votes among three outputs for detecting and correcting the errors. So the main issue is that they require a large overhead in terms of circuit implementation. However, another approach is to use algorithmic properties to detect/correct errors. This is frequently mentioned as Algorithmic Based Fault Tolerance (ABFT). It can reduce the overhead required for protecting a circuit.

Signal processing and communication circuits are well accommodating for ABFT because these circuits have regular structures and many algorithmic properties. Various ABFT techniques are proposed for protecting the basic blocks. Several works are considered to protect the digital filters. The protection of FFT is also extensively studied. Signal processing systems become more complex and it is to find various filters and FFTs which are operating in parallel. For example, Multiple-Input Multiple-Output (MIMO) communication system. Hence, these parallel filters or FFTs generates an opportunity for implementing the ABFT technique.

II.LITERATURE SURVEY

A single Error Correction Hamming Code is proposed. The original system contains four FFT modules and three redundant modules are added for detecting and correcting the errors. The inputs to the redundant modules are linear combination of inputs. They are used to check linear combinations of the outputs. In this technique, the overheads are lower than TMR as the number of redundant FFTs is related to the logarithm of the number of original FFTs. Let us take example, for protecting the four FFTs three redundant FFTs are needed and to protect eleven FFTs, four redundant FFTs are needed. Hence, it shows that decreasing the overheads with the number of FFTs.

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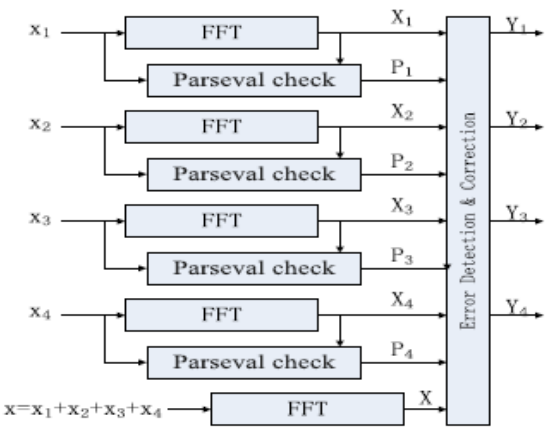

Fig 1.Parity SOS fault tolerant parallel FFTs.

Sum of Squares (SOSs) check is one of the techniques to protect the FFT. This technique is based on the Parseval theorem that states that the SOSs of the inputs to the FFT are equal to the SOSs of the outputs of the FFT excluding a scaling factor. This relationship can be used for detecting the errors with low overhead for each input or output sample.

SOS check can be combined with the ECC for reducing the protection overhead for the parallel FFTs. Hence SOS check only detects the errors and ECC should implement the correction. This can be achieved by using a single parity bit for all FFTs. The combination of a parity FFT and the SOS check can reduces the number of additional FFTs. This scheme will be referred as parity-SOS.

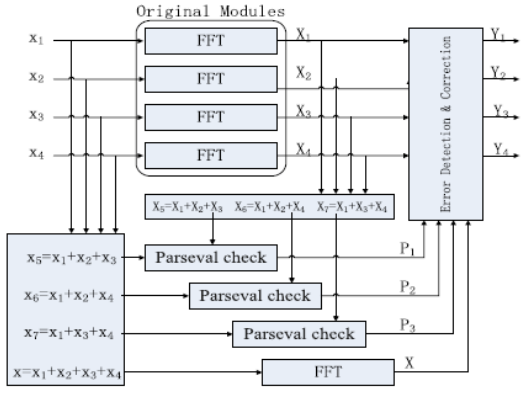

Fig 2. Parity SOS-ECC fault tolerant parallel FFTs.

An additional parity FFT is used for correcting the errors in Parity-SOS scheme. This technique is shown in above fig 2. The main advantage is to reduce the number of SOS checks needed. This scheme is referred as parity-SOS-ECC technique. Hence, final observation is that ECC scheme can detect all the errors which exceed a threshold and SOS can detect most errors. Therefore, fault injection experiments to be done for determining the percentage of errors which are actually corrected.

III.PROPOSED SYSTEM

Recently, a new scheme is existed which is based on the Error Correction Codes (ECC). In this technique, each filter can be equivalent of a bit and by using addition parity check bits can be computed. The operation of this technique is the output of the sum of the several inputs is the sum of the individual outputs. So, this is valid for any linear operation.

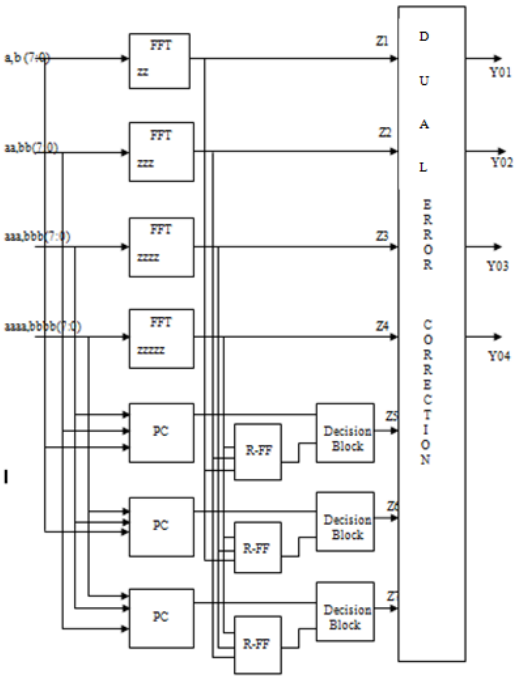

Fig 3. Parallel FFT protection using ECCs.

It is assumed that there is only a double error on the system at any given point in time. There are three main contributions. They are

1) Error Correction Code is assessed to protect the parallel FFTs which show its effectiveness in terms of overhead and protection effectiveness.

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2) A new technique is proposed based on the use of Parseval or sum of squares (SOSs) checks combined with parity FFT.
3) A new technique is proposed on which the ECC is used on the SOS checks instead of the FFTs.

This scheme is evaluated by using FPGA implementations to assess the protection overhead. The protection overhead can be reduced by combining the use of ECCs and parseval checks.

IV.RESULTS

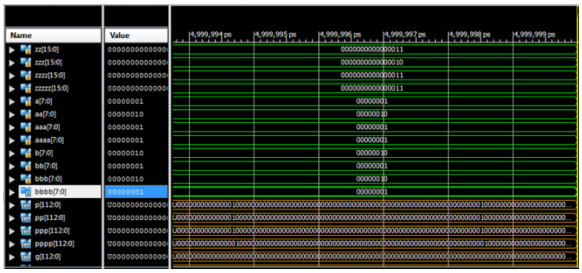

FIG 4. INPUT WAVEFORM

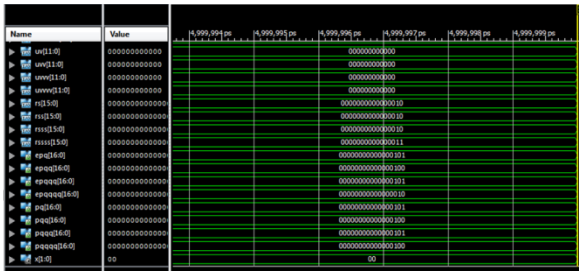

FIG 5. OUTPUT WAVEFORM

V.CONCLUSION

Detecting and correcting errors such as critical reliability are difficult in signal processing which increases the use of fault tolerant implementation. Recently, it is common to signal processing circuits for finding the several filters operating in parallel. Proposed is an area efficient technique to detect and correct single errors. The approach is on the basis of applying SOS-ECC check to the parallel FFT outputs to detect and correct errors. A simple parity FFT is used for correction. The 8 point FFT with the input bit length 32 is protected using the proposed technique. This technique can detect and correct only single bit error and it reduces area results in high speed compared to existing techniques. In the parity-SOS scheme and the parity-SOS-ECC scheme the fault coverage is 99.9% when the tolerance level for SOS check is 1.

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