International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

Mcm Based Digital Filter for Audio Applications

S.SaiSri & M.Venkateswarlu,
M.Tech, (VLSI Design) Department of ECE, Aditya College of Engineering (JNTUK),Surampalem,A.P
M.Tech, Assistant Professor, Department of ECE, Aditya College of Engineering (JNTUK),Surampalem,A.P

Abstract

In Digital signal processing, the concept of digital filter plays a major role. To design efficient filter the order should be small. A minimum order Finite Impulse Response (FIR) digital filter is designed for filtering noise from audio signal [5].

In this paper we propose the computationally efficient, low memory, low area and low delay FIR filter design using multiplier less multiple constant multiplication technique and synthesized using Xilinx ISE 13.2. The extended architecture of Digital filter is capable of filtering 16 bit of input data signal by using delays, adders and MCM. This architecture shows reduction in memory, area utilization and delay. The depth of operation reduced to avoid glitches.

Key Words: Multiple constant multiplication (MCM), FIR filter, Digital Filter.

I. Introduction

The development in electronic technology is taking place at a mind boggling speed. Digital Signal Processing (DSP) finds applications in almost all walks of life [10]. Now a day's multimedia requires the processing of the signal to be very fast with less power consumption. In multimedia audio signal processing is an important area. Many times we need to remove noise from the audio signals. Therefore Digital Filter is to be designed for removing noise.

Digital Filter coefficients can be represented by fixed and floating point formats. Deciding whether fixed or floating point is more appropriate for the given problem must be done carefully. In general it can be assumed that fixed point implementations have higher speed and lower cost, while floating point implementations have higher dynamic range and no need of scaling which may be attractive for more complicated algorithms .The research is going on the optimized digital filter in terms of area and speed.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

As multipliers consume additional power [5] in multiply and Accumulate (MAC) operation many multiplier less schemes are projected. Figure 1 shows the FIR filter.

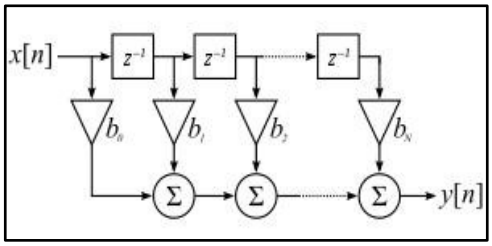


Fig.1: FIR Filter

There are 2 forms of constant multiplication. One is Single Constant Multiplication and another one is Multiple Constant Multiplication. Input is increased with single specific constant to supply output is termed SCM. A variable can be multiplied by a given set of fixed-point constants using a multiplier block that consists exclusively of additions, subtractions, and shifts. The generation of a multiplier block from the set of constants is known as the multiple constant multiplication (MCM).

II. Existing System

Distributed Arithmetic technique is bit-serial in nature. It is actually a bit-level rearrangement of the MAC operation. DA replaces multiplication with a high number of look up tables and a scaling accumulator [5].

Drawbacks:

- Area will be more by using LUT.
- Delay is high.
- The LUT in DA uses more memory.

III. Proposed System

Main objective is to eliminate the multiplier block and introducing the MCM design in FIR filter for reducing the requirement of number of multiplications and reduce area, delay, memory. Within the variety of shift and add operations [3].

Multiple constant multiplication (MCM) is a computation technique to replace multiplications with adders and shifts. Shifts can be hardwired [4] so the final cost is measured in terms of adders and subtractors. Multiple constant multiplication (MCM) has proven its use certainly benefits in efficient filter design [7].

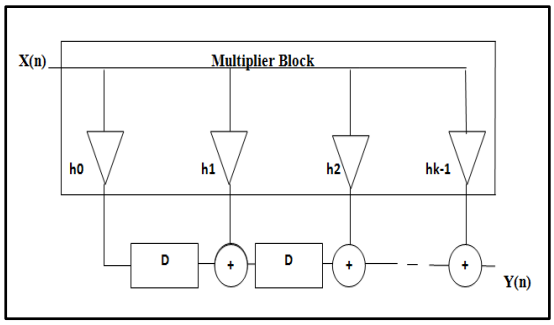
Advantages:

- Area will be minimized.
- Delay is minimized.
- MCM uses less memory.

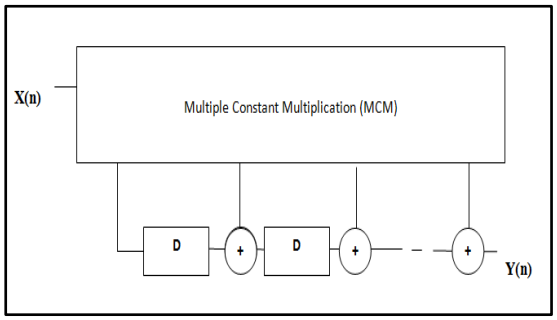
International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

A. MCM Based Filter Design

The constant multiplications are implemented by add/sub and shift operations [6]. Firstly, the constants are represented in binary format. The variable is shifted and adds up the shifted variable to get result. This chapter explains about MCM.



(a)



(b)

Fig. 2: FIR filters with MCM

Figure 2 shows the FIR filter with multiplier less MCM. To get the optimized solution, the original coefficients are multiplied by constant values as shown in figure 3 Variable x is multiplied by several constants C1, C2, C3...Cn in the multiplier block and results in C1x, C2x, C3x...Cnx. This can be done using multiplier block which consists of multiplier less techniques like addition, subtraction and shifts. Realizing such coefficients from multiplications of constant is known as Multiple Constant Multiplication (MCM) [2].

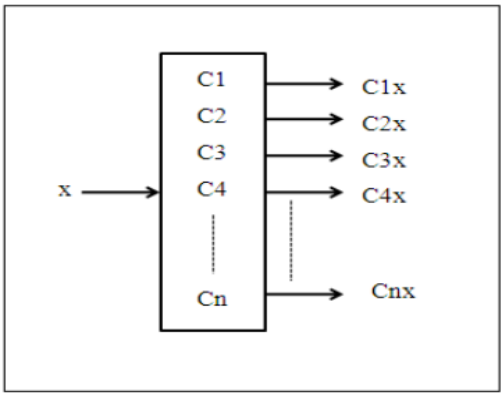


Fig. 3: MCM Operation

An MCM circuit results in significant improvement in digital designs since reduces the overall structure of the circuit and hence price.

However, implementation of constant multiplications in an exceedingly shift-adds design allows the sharing of common partial product among the constant multiplications that considerably reduces the realm and power dissipation of the MCM technique [2].

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

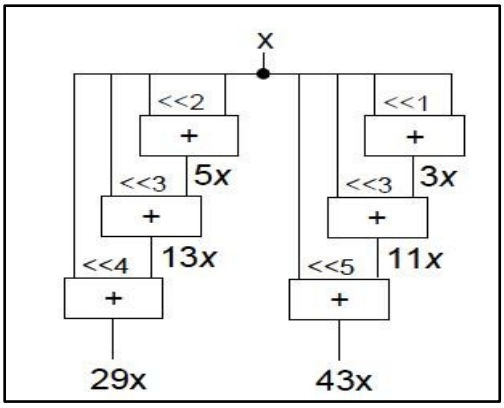


Fig.4: MCM Shift Add

figure 4 shows MCM implementation of add shift for {29,43}.

B. Cumulative Benefit Heuristic

This chapter explains HCUB algorithm of MCM. The Cumulative Benefit Heuristic **(**HCUB) presented by Voronenko [1] to improve performance for multiplications by longer constants. HCUB is graph based algorithm and outperforms other algorithms under most conditions. The disadvantage of previous algorithms is they use more add/sub/shift operations and they are not effective for constant with more than 19 bits. HCUB performs better for constants with more than 19 bits.

HCUB is also divided into two parts: optimal solution and heuristic solution [1]. The optimal part of the algorithm is almost the same as RAG-n; the big difference is the heuristic part. RAG-n uses a LUT for the heuristic part. Which is time consuming and computationally complex. The heuristic part of the HCUB algorithm does not need a LUT. For the optimal part of HCUB, instead of forming a successor set like RAG-n, it is computed incrementally. When there are no more coefficients found in the successor set, then no further synthesis is possible. At that point the algorithm jumps to heuristic part. Like RAG-n the heuristic part of HCUB algorithm uses adder distance, referred to as *A*-distance. The basic idea of the heuristic part is to calculate the adder distance to create an extra fundamental to realize the required coefficient without using a single constant multiplication (SCM) look-up table.The short coming of Rag-n is that it does not try to select the intermediate fundamentals and can be explained using an example where t = {23,81}[8].

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

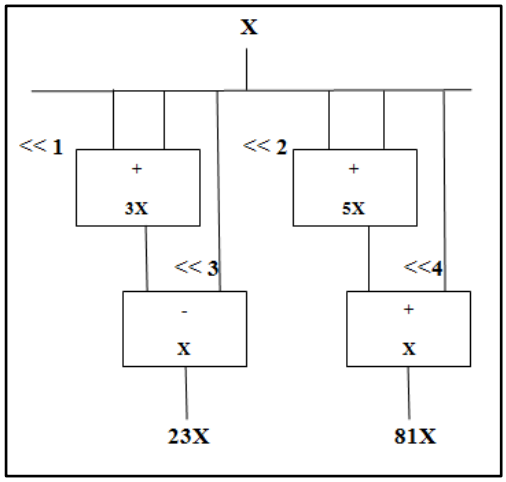


Fig.5: No Sharing (n-RAG)

By using sharing partial products reduces number of shifts from 4 to 3 and add/sub from 4 to 3. Finally figure 5 reduced as figure 6 using HCUB.

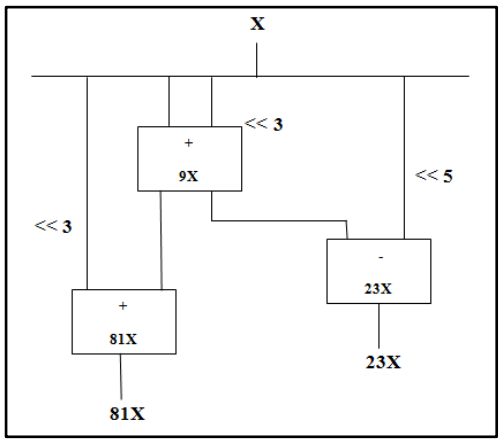


Fig.6: Sharing (HCUB)

HCUB outperforms RAG-n for coefficients with 32 to 100 bits. And it gives 20% improvement over RAG-n[1,7].

IV. Simulation Results

All the synthesis and simulation results are performed by Xilinx ISE 13.2 using Verilog HDL. The simulation results are shown below figures.

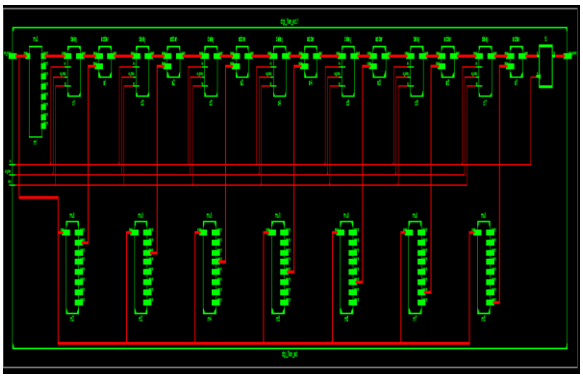


Fig.7: RTL Schematic

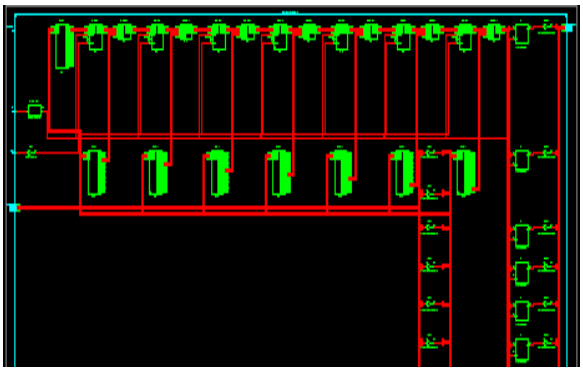
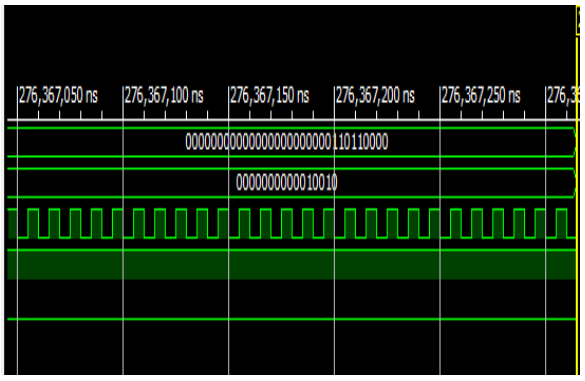


Fig.8: Technical Schematic



International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

Fig.9: Simulation Result

```
Device utilization summary:
---------------------------

Selected Device : 3s1200eft256-5

 Number of Slices:                 80  out of   8672    0%
 Number of Slice Flip Flops:      156  out of  17344    0%
 Number of 4 input LUTs:          159  out of  17344    0%
 Number of IOs:                    51
 Number of bonded IOBs:            50  out of    190   26%
 Number of GCLKs:                   1  out of     24    4%
```

Fig.10: Device Utilization

Table1. Comparison of DA and MCM

Name	DA	MCM
Number Of Slice	193	80
Number Of FF	144	156
Number of LUTs	224	159
Frequency(MHz)	41.544	249.719
Delay(ns)	24.071	4.005
Memory(kb)	249728	239744
Area	561	395

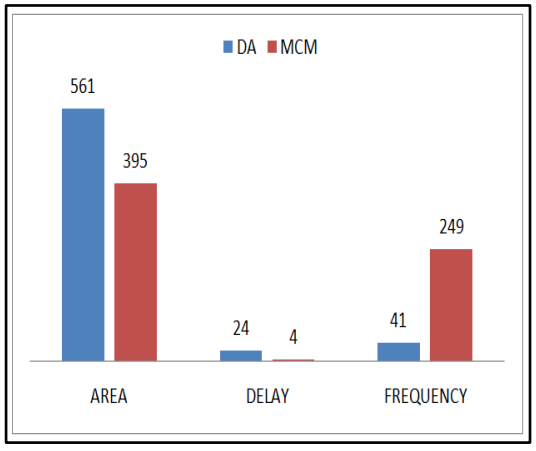


Fig.11: Comparison of area, delay, frequency

V. Conclusion

FIR filter using multiplier less multiple constant multiplication method is designed using Hcub algorithm. The design shows reduction in memory, area utilization and delay. The cost is reduced because of lower depth operation. Our proposed system uses 80 slices, 156 flip flops and 159 LUTs. Still there is a scope to apply appropriate techniques to reduce the number of resources utilized and reduction in the computation complexity.

References

[1] Yevgen Voronenko and Markus Püschel Multiplierless Multiple Constant Multiplication ACM Transactions on Algorithms, Vol. 3, No. 2, 2007

[2] Govardhan Patil, Abhijit. (2010). FPGA Implementation Of Digital Filters Using MCM.

[3] S. Sai Sreelekha 1, C. Vijaya Bhaskar," An Area Efficient Mcm Based Digital Fir Filter For Signal Processing System" Volume: 02 Issue: 02 | May-2015.

[4] N. Goel and A. Nandi, "Design of FIR Filter Using FCSD Representation," 2015 IEEE International Conference on Computational Intelligence & Communication Technology, Ghaziabad, 2015, pp. 617-620.
doi: 10.1109/CICT.2015.85

[5] G. S. Gawande and K. B. Khanchandani, Efficient Design and FPGA Implementation of Digital Filter for Audio Application,2015 International Conference on Computing Communication Control and Automation,

Pune, 2015, pp. 906-910. doi: 10.1109/ICCUBEA.2015.180

[6] A. G. Dempster, S. S. Dimirsoy and I. Kale, "Designing multiplier blocks with low logic depth," 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), 2002, pp. V-773-V-776 vol.5.doi: 10.1109/ISCAS.2002.1010818

[7] T. Sandhya Pridhini*, Diana Aloshius, Aarthi Avanthiga, Rubesh Anand, Design Of Multiple Constant Multiplication Algorithm For Fir Filter,

[8] Vincent Lefèvre. Multiplication by an Integer Constant. [Research Report] RR-4192, INRIA. 2001.

[9] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York: Wiley, 1999.

[10] Wiley: Digital Audio Signal Processing, 2nd Edition - Udo Zolzer, IJCSMC, Vol. 3, Issue. 3, March 2014, pg.438 – 444.