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Design of Non-Volatile memory with fast and low power amplifier and writing circuit based on VCMA technique

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Abstract:

A high-speed and low-power pre-read and write sense amplifier (PWSA) is presented for magneto resistive random access memory (MRAM). The sense amplifier incorporates a writing circuit for MRAM bits switched magnetic tunnel junction (MTJ). By combining read and write functions in a single power-efficient circuit, the PWSA allows for fast read and write operations while minimizing the bit error rate (BER) after data programming. Using the pre-read and comparison steps in the data program operation, we are able to reduce write power consumption under random data input conditions. By using the voltage controlled magnetic anisotropy (VCMA) effect for precessional switching, more than 10x reduction of write power and transistor size both in the memory cell and the write circuit is achieved, compared to using the spin transfer torque (STT) effect by the modified differential amplifier with XOR and XNOR gates. In this paper achieved less area, reducing the power and modified circuit for xnor by using MOS technology to compare the data of S Latch and D Latch.

Index Terms: MRAM (Magnetic Random Access Memory), PWSA (Pre-charge Writing and Sensing Amplifier), VCMA (Voltage Controlled Magnetic Anisotropy)

Introduction

Memory is the heart of the processor. On chip memory occupies a more portion of the over-all processor in a system. The last few years, advance improvements in memory density; this has also resulted in an increase of power dissipation, energy for data transfer and read/ write delay. The development of new generation non-volatile memories, such as Phase change Memories (PCMs) and Resistive RAMs, calls for accurate and controllable programming pulses, which are fundamental to adequately characterize the memory cell. Magnetic tunnel junction based logic has a great potential of the non-volatility, unlimited endurance, CMOS compatibility and fast switching speed of the MTJ devices. MRAM cells integrate a magnetic tunnel junction (MTJ) consisting of thin insulating barrier (i.e. Mgo) separating two ferromagnetic(TM) layers. Recently, voltage-controlled magnetic anisotropy (VCMA) has been introduced to achieve improved energy-delay efficiency and robust non-volatile writing control with an electric field or a switching voltage. VCMA effect is to enhance its efficiency to demonstrate the scalability. For example, for giga-bit class memory applications, VCMA coefficient of more than a few hundreds or even 1000 fJ/Vm is required. However, the VCMA effect with high speed response is limited to be 100 fJ/Vm at present. The VCMA effect originates from the fact that the interface of oxides with metallic ferromagnets (e.g., CoFeB/Mgo) shows a large perpendicular magnetic anisotropy (PMA), which is sensitive to voltages applied across the dielectric layer. Precessional switching offers the advantages of very high speed (down to ~100 ps) and low switching energy (down to ~1 fJ/bit using the VCMA effect, ~100 fJ/bit using the STT effect.

Magnetic Random Access Memory:

Unlike conventional RAM chip technologies, data in MRAM is not stored as electric charge or current flows, but by magnetic storage elements. The elements are formed from to ferromagnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity: the other plate's field can be changed to match that of an external field to store memory. The first one is difficulty in determining the switching direction. In principle, the state of the magnetic bit is always reversed during resonant switching, irrespective of its initial state. Despite of this issue, precessional VCMA switching only requires one pulse shape (amplitude and length) to write both the parallel and anti parallel data states. This greatly simplifies the pulse generation circuitry and provides more symmetric writes (which is better for device reliability/endurance).

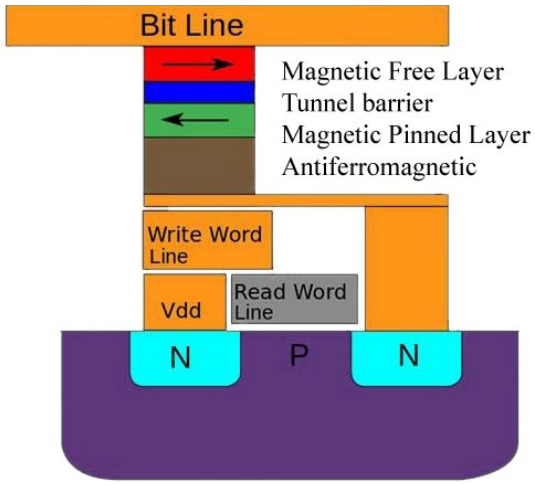

Fig 1: Simplified Structure of MRAM Cell

Magnetic Tunnel Junction:

An MTJ is comprised of two ferromagnetic layers divided by a tunnelling oxide, where the magnetic moment of one layer is fixed and the other can change freely based on electrical and magnetic bias conditions. The magnetization of the MTJ's free layer has two energetically stable states. When the magnetic moments of the free and fixed layers are aligned in the same direction, the parallel state (denoted as P), and the MTJ device has a low resistance (denoted as R_P). In the anti-parallel state (denoted as AP), the free layer magnetization is in the opposite direction to the fixed layer, resulting in a high MTJ resistance (denoted as R_{AP}).

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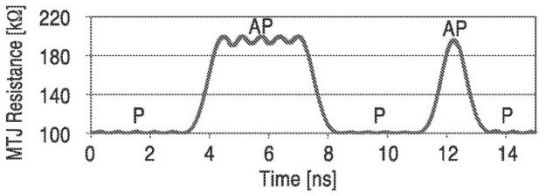

Fig 2: Magnetic Tunnel Junction

Existing System:

In existing system, the MRAM used STT technique and used TTL logic for xnor circuit. Due to the usage of STT technique we use more number of write pulses to the writing circuit. For MTJ one pulse is not required to operate both parallel and anti parallel state. It requires separate pulses for each state. So it does not provide symmetric writes for the writing circuit.

Drawbacks:

The average number of transistors is used more in our work due to the large current requirement for STT switching.

Proposed System:

In proposed system, the MRAM used VCMA technique and used CMOS technology for xnor circuit. Due to the usage of VCMA technique we use only one write pulse to the writing circuit. For MTJ one pulse is required to operate both parallel and anti parallel state. So it provides symmetric writes for the writing circuit.

Advantages:

✓ The large resistance of VCMA MTJ devices assures small write and read current, reducing the power consumption without impact on data programming speed.

✓ The number of transistors used is less than existing design due to the small voltage requirement for VCMA technique.

System Architecture:

This design includes MTJ, precharge sensing amplifier and writing/reading circuit.

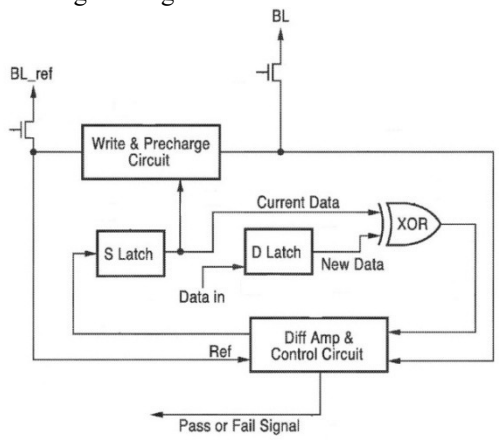

Fig 3: Shows concept diagram of the proposed sense amplifier

The diagram is composed of a Sensing Latch (S Latch), a Data Latch (D Latch), an XNOR logic gate which compares new and current data, a differential amplifier (Diff-amp), and a write and precharge circuit. The circuit is designed to perform a read operation and to compare the current MTJ state to the incoming data, leading to a decision on whether a write pulse should be applied.

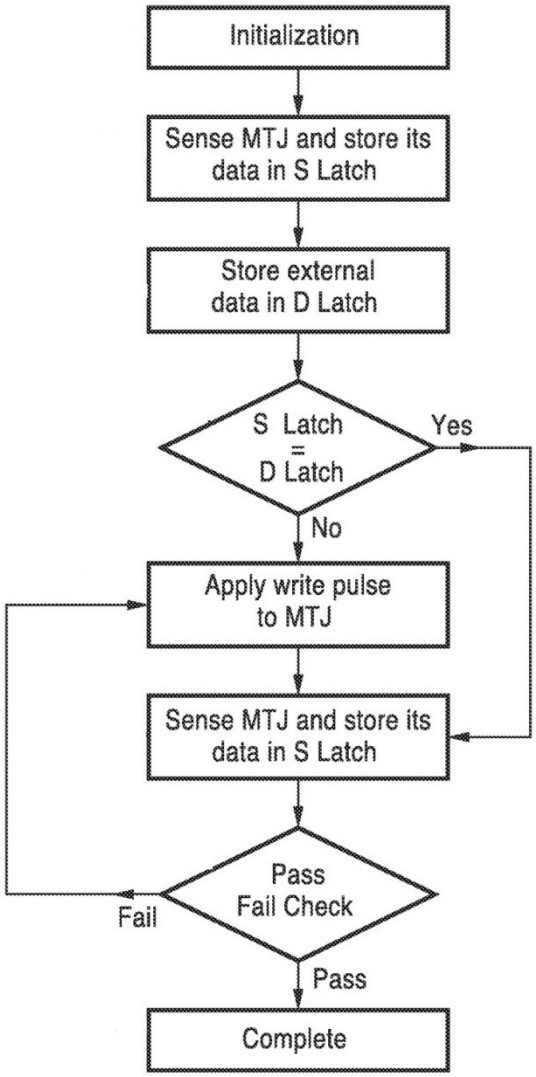

Fig 4: Shows proposed data program flow for the sense amplifier.

From The Fig Data Program Flow, During the Pre- read and comparison step, the circuit compares initial MTJ data and external input data and stores it in the s latch whether to provide a write pulse to the MTJ, based on the comparison result between the initial MTJ data and the external data. The MTJ state is verified after completion of a write pulse, by comparison with the

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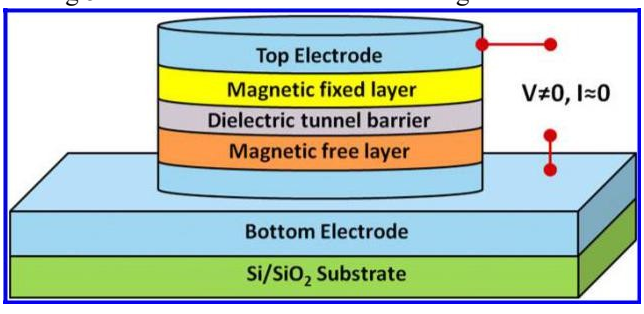
external data on the D latch. If the desired data is matched the operation finishes, and a 'high' pass signal is transferred to the external circuit. Otherwise, the circuit iterates until the MTJ is in the correct state or the maximum number of iterations n is reached

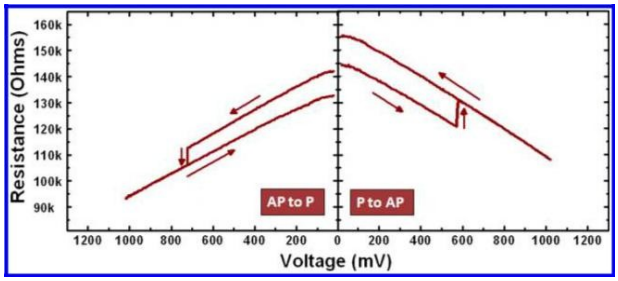
VCMA Technique:

A number of recent works have demonstrated the feasibility of using VCMA to induce or assist in the switching of MTJs. Compared to STT induced switching, VCMA-induced switching offers the potential to reduce power dissipation and enhance density and scalability by eliminating the need for large drive currents, offering a pathway to applications beyond STT MRAM where superior energy efficiency is required. VCMA controlled magnetic memory bit, with free and fixed layers as in a regular MTJ, allowing for the electrical readout of the memory state based on the TMR effect. Unlike STT MRAM, however, the leakage current through the device is small, allowing for the applied voltage (electric field across the tunnel barrier) to control the switching behaviour.

Fig 5: Schematic illustration of a voltage-controlled MTJ



using the VCMA effect, where switching

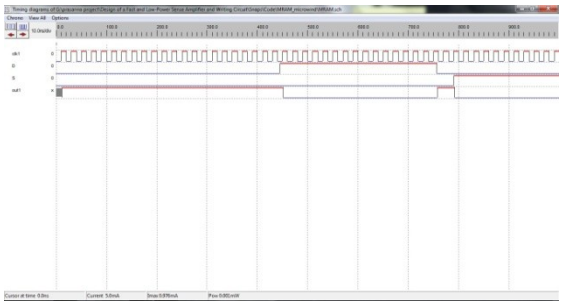


Note that switching in both anti-parallel (AP, high-resistance) to parallel (P, low-resistance) and P to AP directions is performed with voltages of the same polarity, conforming the VCMA-induced switching mechanism.

In the area of memory, VCMA may complement or even replace STT as the switching mechanism used in MRAM, with the potential to significantly enhance its energy efficiency. This will also affect other attributes of STT MRAM such as density and scalability, through reducing (or eliminating) the need to pass currents through the memory bits for writing. By allowing for precessional switching, VCMA can also be used to realize ultrafast write times in magnetic memory cells. Successful realization of these advantages, however, will require development of improved material structures with larger VCMA effects (i.e., operation with lower voltages), while maintaining other important attributes such as high TMR for fast and low-power readout.

The VCMA MTJ is assumed to have 100 kΩ resistance in the parallel state (R_P) and 200 kΩ in the anti-parallel state (R_{AP}), corresponding to the Tunnelling Magnetoresistance (TMR) of 100%. TMR is defined as $(R_{AP} - R_P)/ R_P$.

Circuit Diagram:



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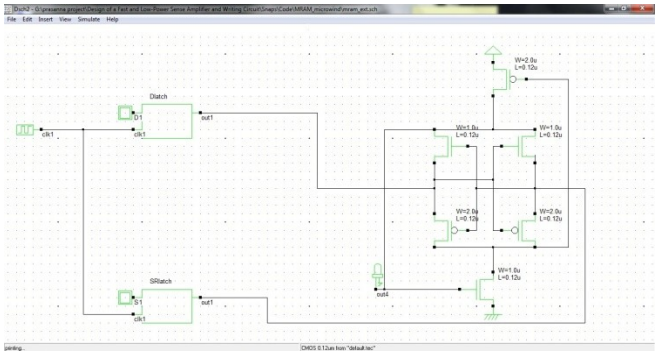

Fig 6: Proposed Circuit Diagram

Comparison of Simulation Results:

Fig 7:

Simulation result of existing system (power consumed=0.173mW)

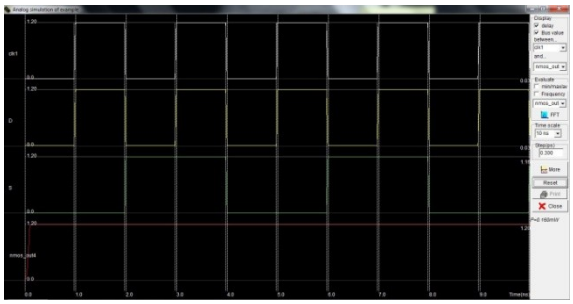

Fig 8: Simulation result of proposed system (power consumed=0.160mW)

Timing Diagrams:

Fig 9: Timing Diagram of Existing System

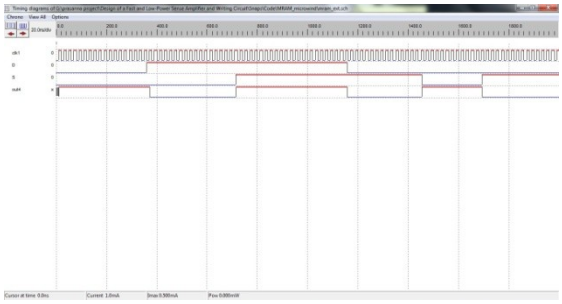

Fig 10: Timing Diagram of Proposed System

Layout Diagrams:

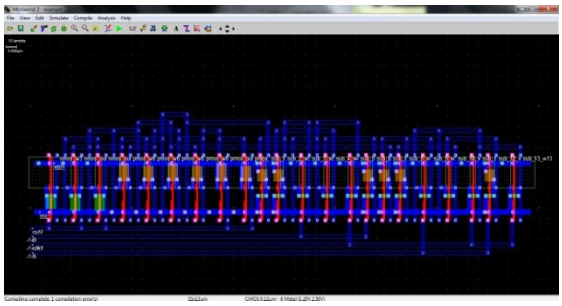

Fig 11: Existing System Layout

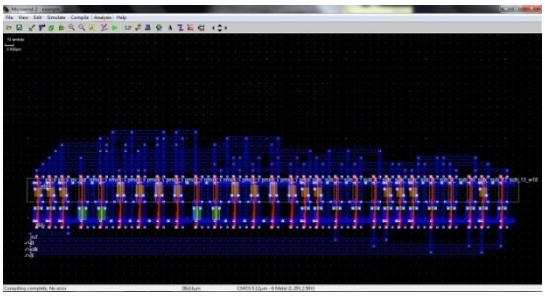

Fig 12: Proposed System Layout

Software Requirements:

✓ In this, the circuits can be designed and compile hear using Microwind and DSCH Software. Microwind is a tool for designing and simulating circuit at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator.

✓ DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation.

✓ Tools from Microwind:

• Microwind

• DSCH

• Microwind3 Editor

• Microwind 2D viewer

• Microwind 3D viewer

• Microwind analog simulator.

Conclusion:

In this paper, deign of PWSA circuit for MRAM is proposed in our work with CMOS technology. A PWSA including a comparison circuit for high speed MRAM is proposed circuit topology decreases the power consumption and area. The existing design that was based on TTL logic. Our proposed design provides promising result than existing system. Our work concentrated on reduction of power and also area efficiency, thus from the overall parameters we have achieved better performance than the existing deign. For this design held in CMOS design methodology and we have used Microwind as simulation tool to show the performance.

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