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Designing Tunable Subthreshold Logic Circuits Using Adaptive Feedback Equalization

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Abstract:-
In embedded applications, ultralow-power sub-threshold logic circuits have extensive use with limited energy budgets. By operating in the sub-threshold regime, we can achieve minimum energy utilization of digital logic circuits. However, in this regime process variations can result in up to an order of magnitude variation in ION/IOFF ratios. It leads to timing errors and have a harmful effect on the working of the sub-threshold circuits. These timing errors become often in scaled technology nodes and hence process variations are highly common. Therefore, mechanisms to check these timing errors while minimizing the energy consumption are necessary. In this paper, we propose a tunable adaptive feedback equalizer circuit which is used with a sequential digital logic to check the process variation effects and reduce the dominant leakage energy component in the sub-threshold digital logic circuits. We also present detailed energy-performance models of the adaptive feedback equalizer circuit.

Key words:-*Adaptive feedback equalizer, D-Flip flop, Adders, Filter.*

I. INTRODUCTION

Since 1970's VLSI plays a major role in communication and semiconductor devices. VLSI (Very Large Scale Integration) comprises thousands of transistors on a single IC Chips. VLSI is majorly linked with Low power, Area and Speed. The Power Consumption is important phenomenon in many applications. VLSI. The use of subthreshold digital CMOS logic circuits has became popular in energy-constrained applications where high performance is not required. If we scale down the supply voltage then it reduces the dynamic energy consumed by digital circuits. And also reduces the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors.

However, digital logic circuits suffer from process variations and he threshold voltage (VT) is directly affected by operating in the subthreshold region. This in turn has a great impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the subthreshold regime.

Moreover, subthreshold digital circuits suffer from the degraded *I*ON/*I*OFF ratios [2] resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded *I*ON/*I*OFF ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of *VT* varies inversely with the square root of the channel area [3], one approach to overcome the process variation is to upsize the transistors [2]. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates [4] to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption.

In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the subthreshold region while getting robustness .Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance.

Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. To reduce energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to check timing errors got from worse than expected process variations in the subthreshold digital logic.

In general, our approach of using feedback equalizer to reduce energy consumption and increase robustness is independent of the methodology used for designing a combinational logic block operating in the subthreshold regime. The main contributions of this paper areas follows.

1) We propose using an adaptive feedback equalizer circuit in the design of tunable subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the subthreshold digital logic circuits. At the same time, the tunability of this feedback equalizer circuit enables post fabrication tuning of the digital logic block to overcome worse than expected process variations as well as lower energy and improve performance.
2) We present detailed analytical models (AMs) for performance and energy of the adaptive feedback equalizer circuit. These models can be easily used in combination with the existing performance and energy models for subthreshold circuits to generate subthreshold designs that meet energy and/or performance constraints.
3) For a 4-bit adder example circuit, we show that compared with [2], the use of our proposed adaptive feedback equalizer circuit can reduce the energy-delay product (EDP) and also reduce the normalized variation ($3\sigma/\mu$) of the critical path delay. In addition, in case of worse than expected process variations, we show that the tuning capability of the equalizer circuit can be used post fabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy.

II. ADAPTIVE FEEDBACK EQUALIZER CIRCUIT

ADAPTIVE FEEDBACK EQUALIZER CIRCUIT WITH MULTIPLE FEEDBACK PATHS

Combinational logic refers to circuits whose output is strictly depended on the present value of the inputs. As soon as inputs are changed, the information about the previous inputs is lost, that is, combinational logics circuits have no memory. In many applications, information regarding input values at a certain instant of time is required at some future time. Although every digital system is likely to have combinational circuits, most systems encountered in practice also include memory elements, which require that the system be described in terms of sequential logic. Circuits whose outputs depend not only on the present input value but also the past input value are known as sequential logic circuits. The mathematical model of a sequential circuit is usually referred to as a sequential machine.
An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The three basic types are introduced here: S-R, J-K and D.
The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are called asynchronous inputs, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, these asynchronous inputs must both be kept LOW.
Subthreshold digital circuits suffer from the degraded ION/IOFF ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded ION/IOFF ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of VT varies inversely with the square root of the channel area, one approach to overcome the process variation is to upsize the transistors. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the subthreshold region while achieving robustness equivalent to that provided. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the subthreshold digital logic.

Propagation delay of global buses acts as performance bottleneck in many system-on-chip (SOC) and network-on-chip (NOC). While gate delay reduces with scaling, global wire delay increases. Repeater insertion mitigates the delay to some extent at the cost of additional power dissipation and chip area but the gap between logic and interconnect delay is still expected to increase with scaling.

On-chip signaling to date has focused on satisfying the resistance capacitance (RC) delay limit, which can be approximated by the Elmore delay of RC

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network composed of driver, interconnect, and receiver. Clocking a bus faster than the RC limit leads to inter-symbol interference (ISI) . ISI spreads out data pulses and reduces their peak magnitude resulting in bit errors at the receivers. In order to gain more insight into the behavior of ISI, consider the transmission of a lone pulse, i.e., a single 1 among a series of 0's or a single 0 among a series of 1's over an RC-dominated interconnect. We observe that the peak amplitude reduces with reduction in PW. Further, the peak amplitude goes below the decision threshold of 0.6 V for PW < 2.9 ns indicating that errors will occur. Thus, current day systems employ larger pulse widths in order to ensure reliable signaling in the presence of DSM noise and clock jitter, thereby limiting the achievable data rate.

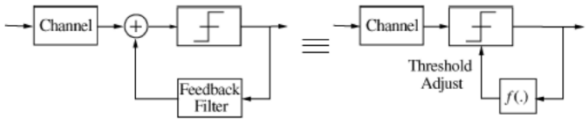
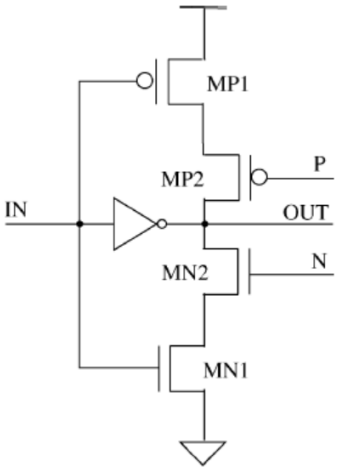


Fig.1. DFE



P	N	V_{th}
GND	VDD	V_{th}^{0}
GND	GND	V_{th}^{+}
VDD	VDD	V_{th}^{-}

Fig.2. Variable threshold inverter

We propose the use of equalization for signaling beyond the *RC* limit and demonstrate its utility in the context of global signaling in 130 nm CMOS process. For a 32-bit, 10-mm bus, we show that equalization alone provides a speedup of 1.28_with 1% area overhead over an unequalized and uncoded bus. We further propose the use of joint equalization and coding where a speedup of 2.3_ is achieved with 69% area overhead, where most of the area overhead is due to coding. To the best of our knowledge, this is the first work that proposes equalization and joint equalization and coding for on-chip signaling. Note that several chip input/output (I/O) signaling systems have begun to employ equalization for data rates greater than 3.125 Gb/s [12] and that equalization is expected to remain the workhorse for future I/O systems. Equalization and, more recently, joint equalization and coding have already been employed to enhance data rates in long-haul and macro networks. This work extends the applicability of equalization into the on-chip domain and is part of the general trend of retargeting communication-theoretic techniques to on-chip systems in order to tradeoff delay/power with reliability.

EQUALIZATION

In communication and I/O signaling systems, equalizers are implemented using filters. These filters mitigate ISI by canceling the effect of past and future bits on the current bit. Fig.1 shows a decision-feedback equalizer (DFE) [11], where the effect of past bits (or decisions) on the current received pulse is canceled by employing a feedback filter. The output of the subtractor is fed to a slicer in order to determine the transmitted bit. This operation is equivalent to modifying the threshold of the slicer based on the past bits as shown in the figure. Such a DFE requires multiply-and-accumulate circuits and is impractical for on-chip buses. Instead, we modify the threshold based on past bits using a variable threshold inverter shown in Fig.2, the threshold voltage of the inverter is controlled by using signals P and N. When P=GND and N=VDD, the threshold voltage is V0th, which is the nominal threshold voltage of the inverter. When P=GND and N = GND, the pull down path is off and the threshold voltage increases to V+th . Similarly, when P = VDD and N = VDD, the pull up path is off and threshold voltage decreases to V-th .A weak inverter is required to ensure that the output of the inverter is never floating. The relative sizing of transistors MP1, MP2, MN1, and MN2 determines the values of V+th and V-th .Further, there exists a tradeoff between the range of variability in the threshold voltage and susceptibility of the inverter to DSM noise due to change in the threshold voltage.

Equalizer for a Single Wire

For a single wire, worst-case delay occurs whenever the wire switches. Therefore, the threshold voltage of the inverter should be adjusted such that it anticipates a transition on the wire. If OUT = VDD (IN = GND), then the threshold voltage should be lowered (P = VDD,N = VDD) such that the delay of a GND ! VDD transition on the wire is reduced. Similarly, if OUT = GND, then the threshold voltage should be increased (P = GND, N = GND) such that the delay of a VDD! GND transition on the wire is reduced. Therefore, the control signals P and N are P = N = OUT: (1) shows the equalizer circuit for a single wire. A buffer is used to drive P and N nodes

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from OUT. The buffer is designed such that its delay is greater than delay from IN to OUT. Thus, the OUT node is able to charge or discharge before P and N signals change.

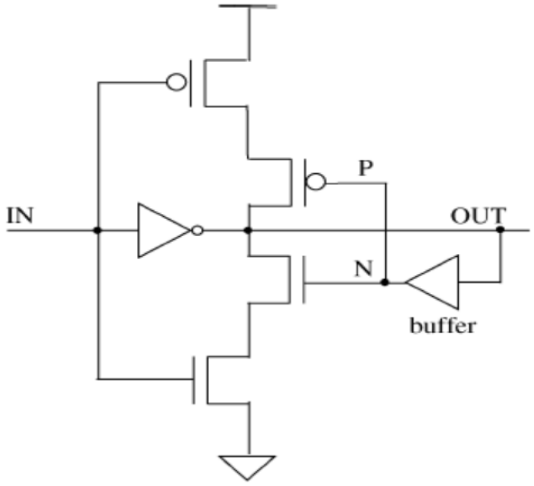

Fig.3. Equalizer for a single wire

Equalizers for Buses

In a bus, the worst-case delay occurs when both neighbors of a switching wire switch in the opposite direction. In other words, the middle wire in a set of three wires will have the worst-case delay when the wires transition from 101 to 010 or vice versa. Therefore, the equalizer for buses needs to utilize the past bits of all three wires when adjusting the threshold voltage for the middle wire. This is achieved by modifying the threshold voltage for the middle wire only when the past output of the set of three wires is either 101 or 010. When the past output is 101, the threshold voltage is raised to V +th and when the past output is 010, the threshold voltage is lowered to V-th . If the past output is neither 101 nor 010, then the threshold voltage is V 0th.

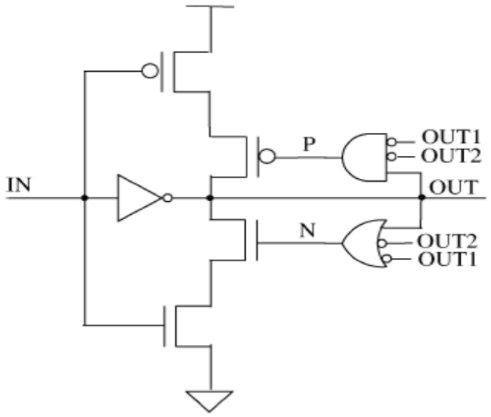

Fig.4. Equalizer for Buses

The previous settings of threshold voltage can be obtained by setting P = VDD when the past output is 010 and P = GND otherwise, and by setting N = GND when the past output is 101 and N = VDD otherwise. Therefore

P = OUT1 _ OUT _ OUT2 (2)

N = OUT1 + OUT + OUT2 (3)

where OUT1 and OUT2 are the outputs of the two adjacent wires. Fig.4 shows the equalizer circuit for buses. The control signals P and N are obtained by using AND and OR gates, respectively. Once again, the delays of the control logic gates are designed to be greater than IN-to-OUT delay so that the OUT node is able to charge or discharge before P and N change. In an equalized bus, all non boundary wires will have the equalizer as receivers, while the boundary wires can use CMOS inverters. This is because a boundary wire has only one neighbor and, hence, experiences much lower crosstalk. Modifying the threshold voltage of the receiver increases its susceptibility to noise, in general. We argue next that the robustness of the proposed equalizer is not reduced in any way if crosstalk noise is the dominant noise source. For example, in a crosstalk noise dominated scenario, the middle wire in a set of three wires will experience a glitch whenever a 000 ! 101 transition occurs. If the receiver threshold for such a wire is lower than the nominal, then the potential for an error increases. The proposed equalizer lowers (raises) the threshold when the past output is 010 (101). A glitch will be introduced if and only if the middle wire remains quiet and one or both of the adjacent wires make a transition from 0 ! 1 (1 ! 0). However, such a glitch will make the middle wire voltage to increase (decrease) beyond VDD (GND). Hence, such a glitch will not affect the robustness of the circuit. However, the modification of threshold voltage can make the bus prone to errors due to other sources of noise. Thus, the proposed technique is an example of the fundamental tradeoff between delay and reliability. The proposed equalizer can reduce the bus delay to (1 + 3_)_0 at best. This is because the threshold remains at the nominal level for all past outputs except 010 and 101. Therefore, when the past output is 110, the threshold voltage is V 0th. If a 110 ! 101 transition occurs, then the middle wire has a delay of (1 + 3_)_0. Since the proposed equalizer mitigates the effect of ISI only after the worst-case transition has occurred, its performance is bounded by (1 + 3_)_0. The worst-case bus delay can be also reduced to (1 + 3_)_0 by employing crosstalk avoidance codes referred to as forbidden overlap codes (FOC) [10]. In FOC, a codeword having bit pattern 010 does not transition to another codeword having the bit pattern 101 and vice versa. This is achieved by employing additional bus wires and codec circuits.

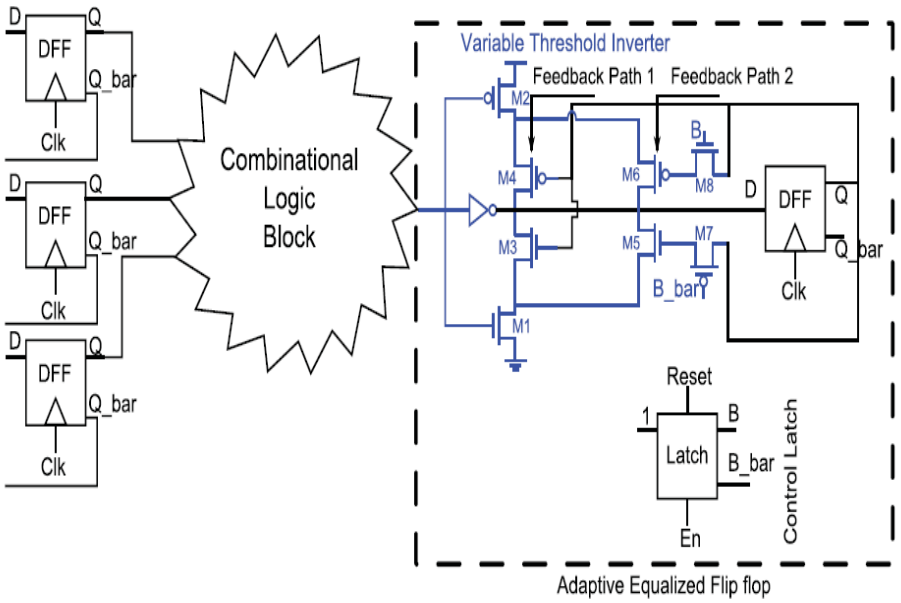

Fig.5. Adaptive feedback equalizer circuit with multiple feedback paths (designed using a variable threshold inverter) can be combined with a traditional master–slave flip-flop to design an adaptive E-flip-flop

III.ADAPTIVE EQUALIZED FLIP-FLOP VERSUS CONVENTIONAL FLIP-FLOP

In this section, we first explain the use of the adaptive feedback equalizer circuit in the design of an adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flop in terms of area, setup time, and performance. We propose the use of a variable threshold inverter [26] (Fig.5) as an adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop [29] (Fig.6) to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feed forward transistors (M1 and M2 in Fig.5) and four control transistors (M3 and M4 for feedback path 1that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON post fabrication in Fig.5) that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip-Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes.

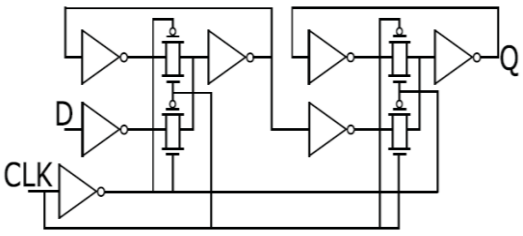

Fig.6. Circuit diagram of classic master–slave positive edge-triggered flip-flop

The control transistors M5 and M6 are enabled/disabled through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip boot up. After boot
up, if required a square pulse is sent to the En terminal to set the output of the latch to 1 to switch ONM7 and M8, which enables feedback path 2.

The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. If the previous output of the flip-flop is a 0, the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly if the previous output is 1,the switching threshold is increased, which speeds up the transition to 0. Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. The adaptive E-flip-flop has eight more transistors than the conventional master–slave flip-flop [29]. Compared with a classic master–slave flip-flop with 22 transistors [seven inverters and four transmission gates (TGs)], the area over head of the adaptive E-flip-flop is 36%. The area overhead of the control latch with ten transistors (three inverters and two TGs) is 45%. This area overhead gets amortized across the entire sequential logic block.

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However, the adaptive feedback equalizer circuit can significantly lower down the propagation delay of the critical path because the small input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic. The hold time of the classic master–slave positive edge-triggered flip-flop is zero [29].

Therefore, the adaptive feedback equalizer circuit does not impact the hold time violations. We analyze the capability of the adaptive feedback equalizer circuit to reduce the transition time of the last gate in critical path of the subthreshold logic and make a comparison with the original non-equalized design, and the buffer-inserted non-equalized design. The classic buffer insertion technique will reduce the total delay along critical path of the subthreshold logic. Like the gates in the combinational logic, the buffer used is upsized to account for the process variation effects based on the design methodology proposed in [2]. Using a minimum-sized inverter instead of an upsized inverter would further lower down the delay but has lower reliability with respect to the dominant process variation effects in the subthreshold regime. So, we propose to use a combination of minimum-sized inverter and feedback equalizer circuit along the critical path of the subthreshold logic. Minimum-sized inverter reduces the total delay and the feedback equalizer mitigates the effect of process variation.

EVALUATION OF ADDERS

By using an 4-bit adder designed in UMC 130-nm process as a sample circuit, we first explore the use of the feedback equalizer circuit to reduce energy consumption while maintaining reliable operation of the 4-bitadder. This is followed by the evaluation of the post fabrication tunability property of the adaptive equalizer circuit to manage the occurrence of worse than expected process variations in the 4-bit adder circuit after fabrication. In addition, we provide an evaluation of the use of feedback equalizer circuit in the8-bit adder designed using aggressive technology nodes.

Improvement of Energy Efficiency

We first explore the case where the feedback equalizer circuit reduces the rise/fall time of the last gate, and hence the delay of the critical path of combinational logic blocks leading to a higher operating frequency without any change in supply voltage. In general, the variable threshold inverter can be used to reduce the propagation delay of the critical path at any operating supply voltage. Here, we determined the optimum sizing for the feedback equalizer circuit that minimizes the propagation delay of the critical path and avoids sampling of glitches to achieve zero-error rate operation at each supply voltage. The sizing of the combinational logic block is the same for both the E-logic and NE-logic and is determined using the design methodology described in [2] to address the degraded noise margin levels in subthreshold regime. The operating frequency of the E-logic is 18.91% (on average) higher than the NE-logic over the range of 250–350 mV.

By reducing the propagation delay of the critical path, the feedback equalizer circuit is capable of reducing the dominant leakage energy consumption of the digital logic in the subthreshold regime.

Proposed FIR filter:

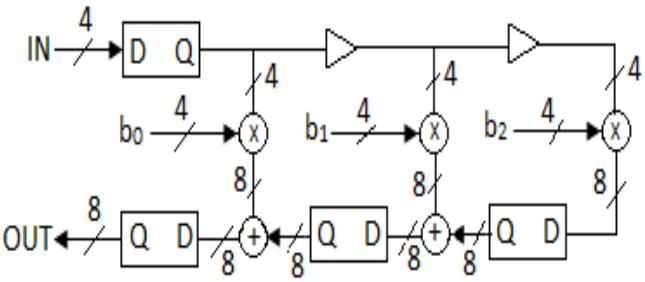

Fig.7. 4-bit filter using array multiplier, Full Adder and D-Flip flop

Proposed D-Flip flop circuit:

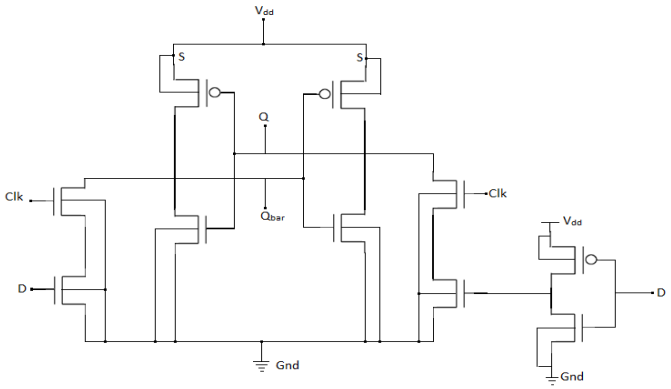

Fig.8. 1-bit CMOS logic circuit (Negative edge trigger)

By replacing the above circuit, the no. of transistor count and delay is reduced. The circuit consists of only 10 transistors comparatively occupies less area and power consumption is less.

SIMULATION AND RESULTS

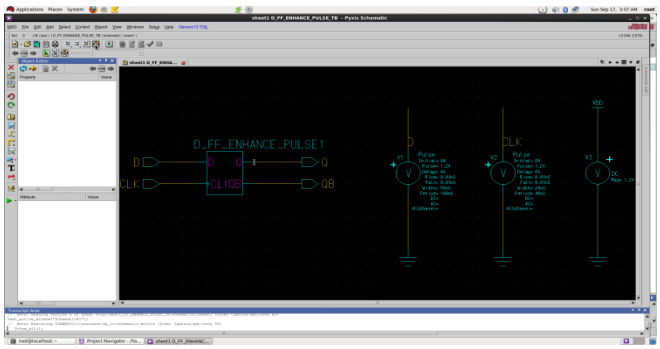

Fig.9. Test bench for Enhance D flip flop

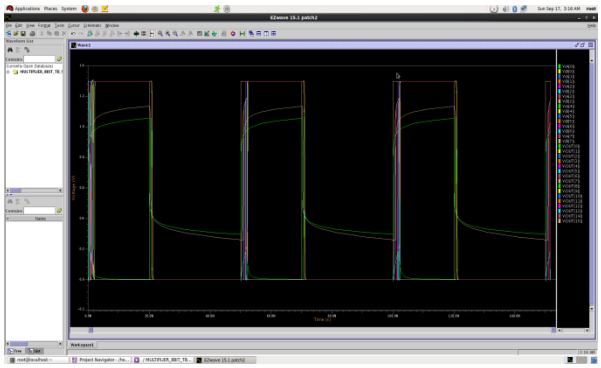

Fig.10. Final waveforms of Existing IIR filter

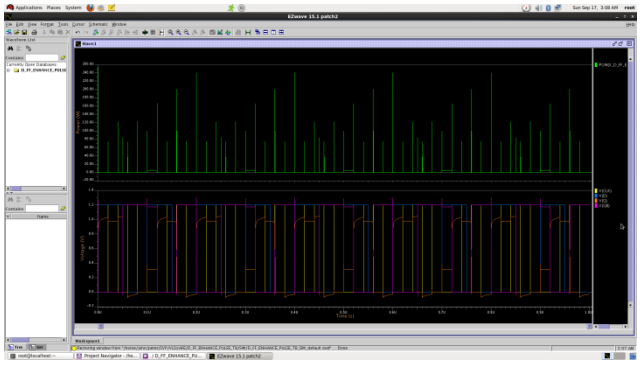

Fig.11. Waveforms for Proposed Enhanced D flip-flop

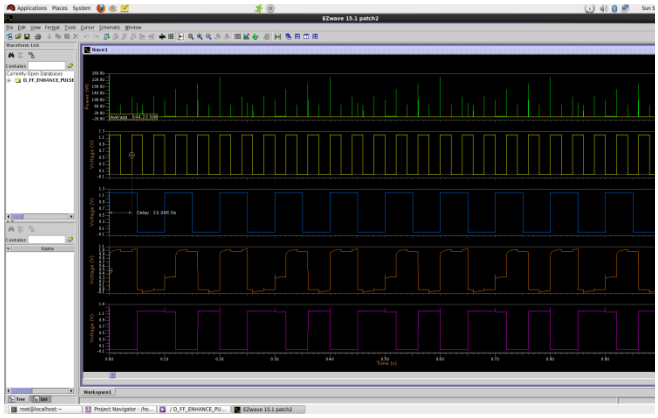

Fig.12. Waveforms for existing enhanced D-flip flop

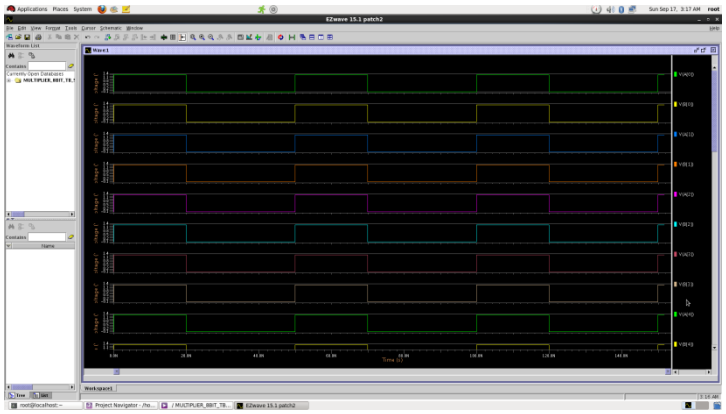

Fig.13. Waveform for proposed IIR filter

CONCLUSION

We proposed the application of a tunable adaptive feedback equalizer circuit to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the subthreshold regime. Adjusting the switching thresholds of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region. We implemented a non-equalized and an equalized design of a 4-bit adder in UMC 130-nm process using static complementary CMOS logic. Using the equalized design the normalized variation of the total critical path delay can be reduced at minimum energy supply voltage. Moreover, we showed that in case of worse than expected process variation, the tuning capability of the equalizer circuit can be used post fabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy. We also presented detailed delay and energy models of the equalized digital logic circuit operating in the subthreshold regime.

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