International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

Design of a PLL with Dual VCO'S for the Application of Bluetooth

B.Ashwini & P.Suresh Reddy

1. PG Scholar, Dept of ECE, Ellenki Institute of Engineering & Technology, Patelguda, Patancheru, Medak (Dist), India.
2. Assistant professor, Dept of ECE, Ellenki Institute of Engineering & Technology, Patelguda, Patancheru, Medak (Dist), India

.

ABSTRACT: *The project presents an Integer-N phase locked loop (PLL) for Bluetooth receiver implemented in CMOS 65 nm technology. The presented phase locked loop consists of an LC quadrature voltage controlled oscillator with capacitor bank, a tri-state phase-frequency detector with charge pump, a third order passive filter and a programmable divider. The PLL has a supply voltage of 1.2 V and dissipates 2.4 mW. The output frequency range of the phase locked loop is from 2.2 GHz to 2.8 GHz and phase noise is equal to 124 dBm/Hz at 3 MHz from carrier frequency.*

Keywords — Phase locked loop, frequency synthesizer, bluetooth, receiver.

I.INTRODUCTION

Superior advanced frameworks utilize tickers to succession operations and synchronize between useful units and between ICs. Clock frequencies and information rates have been expanding with every era of preparing innovation and processor design. Inside these advanced frameworks, very much coordinated tickers are created with stage bolted circles (PLLs) and after that conveyed on-chip with clock supports. The fast increment of the frameworks' check recurrence postures challenges in creating and appropriating the clock with low vulnerability and low power. This exploration presents imaginative strategies at both framework and circuit levels that limit the clock timing vulnerability with least power and zone overhead. In modern wireless communication systems phase locked loop (PLL) is a very important part of each transmitter and receiver. In a radio frequency (RF) receiver, PLL is employed as a local oscillator (LO).

LO determines the frequency at which the device receives the transmitted signal. The most important parameters of a local oscillator are: setting time, phase noise, channel spacing, output frequency range and power consumption. The LO parameters are determined by the proper wireless standard. There are several possible architectures for each block of the PLL. Each solution has some advantages and disadvantages. In this work the main goal was to meet the Bluetooth specification in such a way that the power consumption of the frequency synthesizer is minimized. The presented Integer-N PLL is the first part of a Fractional-N phase locked loop.

II. BLUETOOTH

Bluetooth is a wireless technology standard for data exchanging. It works in the open Industrial, Scientific, Medical (ISM) band from 2.40 GHz to 2.48 GHz. The specification of the main PLL parameters results from the Bluetooth specification [5]. The requirement, the most difficult to fulfill, is for the spectral density of the output signal phase noise, especially for the offset frequency equal to 3 MHz, where the phase noise has to be less than -121 dBc/Hz. Requirements for all PLL parameters, except the phase noise, can be obtained directly from the Bluetooth specification. The phase noise value can be calculated from the following expression:

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

$$PN(f) = \frac{C}{I} - 10\log(BW) - SNR - M,$$

where PN is phase noise in dBc/Hz, C/I is carrier to interference power ratio, BW is signal bandwidth, SNR is signal to noise ratio required by the demodulator to achieve the specified bit error rate and M is arbitrarily defined error margin. For this work the error margin is equal 10 dB. C/I can be found in the wireless standard specification.

III.PROPOSED WORK

The phase detector (PD) compares the reference signal (fref) phase with the phase of the feedback signal (ffb). The PD output signal is proportional to the phase difference of the two input signals. The low pass filter reduces the high frequency phase noise. The voltage control oscillator (VCO) generates a signal, which frequency is controlled by the low pass filter output voltage. The last part of the PLL is a frequency divider. The divider is placed in the feedback path and its output signal is compared with the reference signal in the phase detector. In modern PLL a charge pump (CP) is added to the output of the phase detector. CP transforms the error signal of the phase detector into a current impulse.

A. VCO

The voltage controlled oscillator is the most critical part of the presented loop. It determines the phase noise for the frequencies higher than the PLL bandwidth. VCO is also the most power consuming part of PLL. According to the Bluetooth specification, the output signal has to be Quadrature and differential. There are two ways to implement VCOs with Quadrature output signal. The first option is to design a VCO generating signal with the frequency two times higher than required and use a quadrature frequency divider. The second option is to create two VCOs that are coupled by an additional pair of transistors [9]. The latter provides lower phase noise, because the frequency divider generates additional noise in the circuit. Therefore, the second solution was chosen in this work (Fig. 2). The frequency of the VCO output signal is defined by the resonance frequency of the LC tank that contains an inductance and two varactors. The tuning range of the MOS varactors available in the United Microelectronics Corporation (UMC) CMOS 130 nm technology is narrow. The Bluetooth specification requires the frequency range between 2.40 GHz and 2.48 GHz. However, in order to meet the specification in all process corners at the operating temperature between -40°C and 125°C, the frequency tuning range has to be much wider. The presented VCO can be tuned from 2.2 GHz to 2.80 GHz. In order to obtain the required tuning range a capacitance bank containing two varactors and four switched capacitor pairs has been developed. Each switched capacitor pair consists of two capacitors and a switch transistor. If the switch transistor is on, additional capacitance appears in the resonant circuit. The capacitance bank is controlled by 4 bits, where one bit controls one branch.

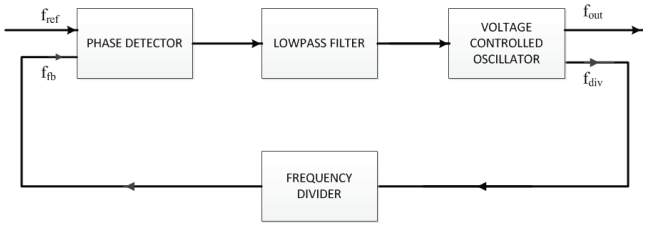

Fig. 1. Block diagram of phase locked loop.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

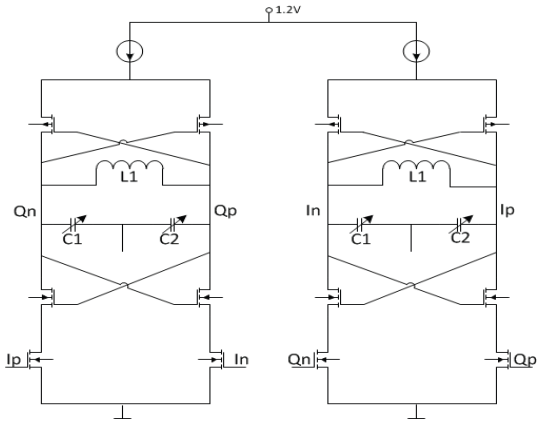

Fig. 2. Implemented architecture of the VCO.

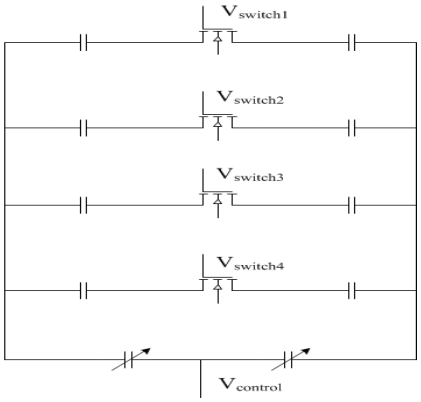

Fig. 3. Capacitor bank of the VCO.

B. Phase detector with charge pump

The phase detector was implemented as a tri state detector. TSPC (True Signal Phase Clock) dynamic flip-flops were used in this design. Fig. 4 shows a block diagram of the phase detector. It contains two TSPC flip-flops [7], two inverters and a NOR gate. The reference signal and the feedback signal are connected to the reset port of each flip-flop. The set ports work as asynchronous input and are connected in the feedback loop with the NOR gate. The two inverters make it possible to avoid the dead zone effect. There are three main architectures of the charge pump [1] that differ by the location of the switch transistor: drain switched CP, gate switched CP and source switched CP. Because drain switched CP provides the fastest switching time, this solution was implemented. The charge pump architecture is presented in Fig. 5. The CP consists of two current mirrors and four transistor switches. The output signal of the phase detector opens or closes the NMOS and PMOS mirrors, therefore a current impulse is generated at the output of the CP. The charge pump is an important part of the PLL, because its current determines the in-band noise and bandwidth of the PLL. Equation (3) presents the relationship between the CP current and phase noise.

C. Lowpass filter

In the presented work a third order passive filter was implemented. Passive filters introduce lower noise in the PLL output than the active ones. The filter was implemented to obtain a 350 kHz phase locked loop bandwidth to reduce the phase noise from the charge pump. 60 degree phase margin was achieved which ensures stable work of the PLL. The designed filter is presented in Fig. 6.

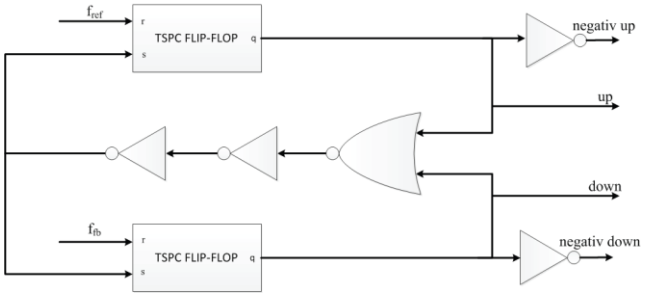

Fig. 4. Block diagram of phase detector.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 04 Issue-17
December 2017

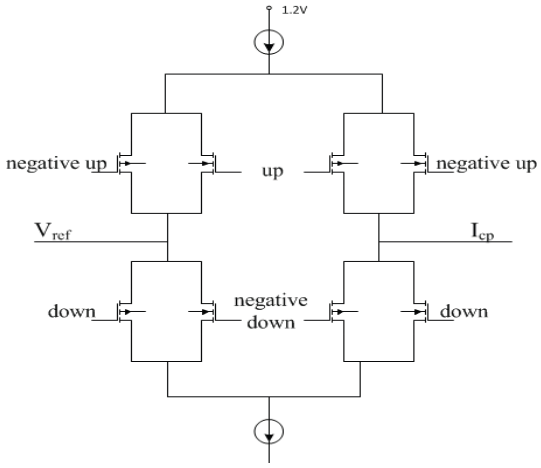

Fig. 5. Electrical diagram of charge pump.

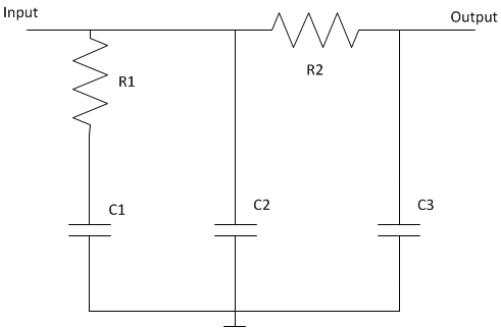

Fig. 6. Electrical diagram of low pass filter.

IV. SIMULATION RESULTS

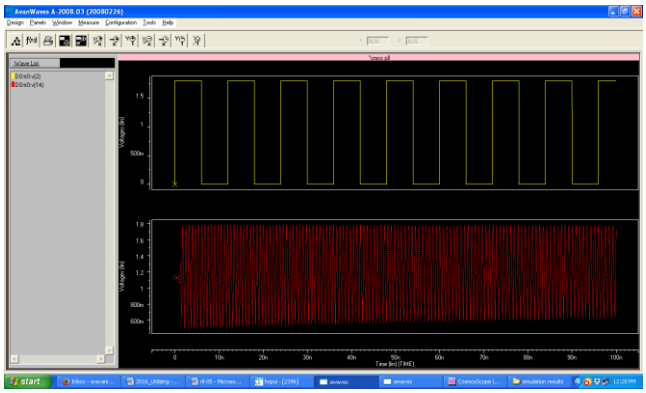

Fig 7: PLL with 135nm Technology

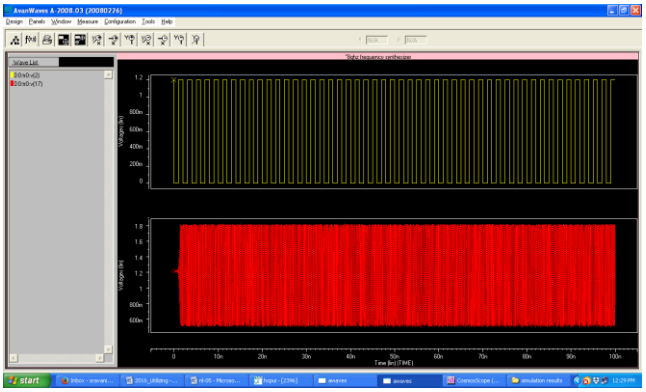

Fig 8: PLL with 65nm Technology

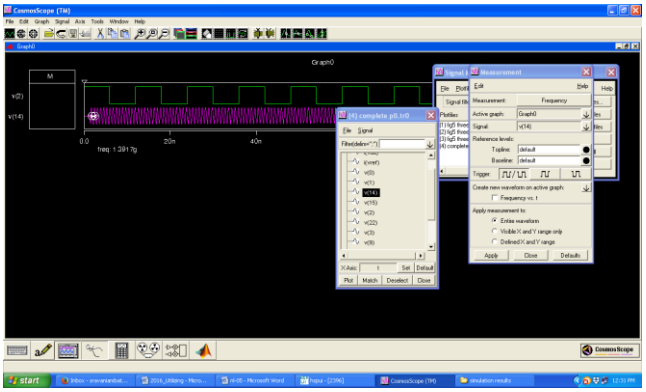

Fig 9: Frequency for 135nm PLL

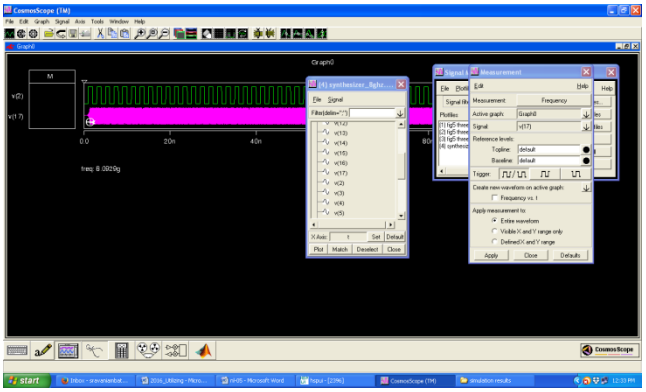

Fig 9: Frequency for 65nm PLL

V.CONCLUSION

In this task an Integer-N PLL with 65nm cmos technology has been exhibited. The introduced configuration shows great execution. The composed VCO gives - 125 dBc/Hz stage clamor at 3 MHz from transporter recurrence. The recurrence tuning range is 2.2 GHz-2.8 GHz, and the power utilization is equivalent to 2.4 mW. The transmission capacity of the displayed PLL is 350 kHz. The channel dispersing squares with the reference, which is not adequate for the Bluetooth beneficiary. The recurrence tuning step is higher than that required by Bluetooth particular channel dispersing. The recurrence tuning venture of the PLL can be enhanced by adding delta-sigma modulator to get a Fractional-N stage bolted circle. In a Fractional-N PLL the tuning step can be portion of the reference flag and this arrangement makes it conceivable to get the required tuning step. The fragmentary N PLL will be a continuation of the introduced circuit.

VI. FUTURE SCOPE

PLL configuration utilizing low power ideas can be incorporated to plan an Application Specific Integrated Circuit (ASIC) for the centers exhibited in this postulation. This work utilizes Zigbee correspondence interface amongst hubs and as a future heading of study, the information exchange might be up scaled to higher information rates and high working frequencies.

REFERENCES

[1] K. Siwiec, T.Borejko, W. Pleskacz, "computer aided design Tool for PLL Design", in Proc. Outline and Diagnostics of Electronic Circuits and Systems, 2011, pp. 283-286.

[2] W. Rhee, "Plan of elite CMOS charge directs in phaselockedloops", in Proc. IEEE International Symposium on Circuits and Systems, 1999, pp. 545-548.

[3] Ali Hajimiri, Thomas H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", IEEE Journal of Solid-State Circiut, vol. 33, 1998, pp. 179-194.

[4] Keliu Shu, Edgar Sánchez-Sinencio "A 2.4-GHz Monolithic FractionalN Frequency Synthesizer With Robust Phase-Switching Prescaler and Loop Capacitance Multiplier", IEEE Journal Solid State Circuit, vol. 38, 2003, pp. 866-874.

[5] Bluetooth specyfication rendition 4.0. The Bluetooth specific vested party Std., 4.0, Jun 2010. [Online]. Avaliable http://www.bluetooth .organization/en-us/specyfication/embraced/specyfication.

[6] Jinho, K.Jongmoon, C.Sanghyun, L.Kwyro, "A 19-mW 2.6-mm2 L1/L2 Dual Band CMOS GPS Receiver", IEEE Journal Solid State Circuit, vol. 40, 2005, pp. 1414-1425.

[7] H. Yoshizawa, K. Taniguchi, K. Nakashi "An execution strategy of dynamic CMOS circuit pertinent to nonconcurrent/synchronous rationale", in Proc. IEEE International Symposium on Circuits and Systems, 1998, pp. 145-148.

[8] Keliu Shu, Edgar Sánchez-Sinencio, CMOS PLL Synthesizers: Analysis and Design, Springer Science, 2005.

[9] Kang-Chun Peng, and Chan-Hung Lee "A 5 GHz CMOS Quadrature VCO with Precise Quadrature Phase", in Proc. Microwave Conference Proceedings, 2012, pp. 1211-1213.

[10] S. Saad, M. Mhiri, A. Ben Hammadi and K. Besbes, "A CMOS 0.35 µs, 3.3-V PLL synthesizer for Bluetooth transmitter", in Proc. Outline and Technology of Integrated Systems in Nanoscale Era (DTIS), 2012, pp 1-5.

Author Profile:

B. Ashwini

Qualification : M.Tech
Areas of Interest : VLSI System Design, Digital communications.

Mail id: bachu.ashwini@gmail.com

Author profile:

P. Suresh Reddy,
Designation: Assistant professor

Experience: 9+years of Teaching experience, Areas of Interest : Embedded Systems & VLSI Design, Digital Communications .

Mail id : purini009@gmail.com