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# CMOS Based Full Adder and its Scaling for Speed and Power Consumption

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**Abstract:** *A fast and energy-efficient Full Adder plays important role in electronics industry especially digital signal processing (DSP), image processing and performing arithmetic operations in microprocessors. Full Adder is such an important element which contributes substantially to the total power consumption of the system. In this paper, proposed 2-bit Full Adder has been taken which is then analyzed and a comparative study of the silicon area and the power consumption has been done in the circuit using different channel lengths such as 90nm, 70nm and 50nm. The designed circuit has shown a remarkable reduction in the consumed power of 94.5% and a reduction of 75.03% in consumed area in 50nm foundry as compared to 90nm COMS technologies. The designed Full adder are compared in terms of power consumption and surface area product using DSCH and MICROWIND tools.*

KEYWORDS: CMOS, VLSI, Full Adder, Power consumption, CMOS technology.

## I. INTRODUCTION

With the advance of VLSI technology, to either speed up the operation or reduce the power/energy consumption hardware implementation of many applications such as multimedia processing, digital communication can be possible. The essence of the approximately all digital computing lies in the full adder design [5]. Addition forms the basis for many processing operations, from counting to multiplication to filtering. As a result, adder circuits are of great interest to digital system designers. Adders are important components in the applications like Digital Signal Processing (DSP) architectures. For signal processing, digital full-adder are the basic logic circuits which can find applications in digital computing and packet labels processing. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. Computations need to be performed using low-power, area-efficient circuits operating at greater speed [1].

There are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). In electronics, pass transistor logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors [2]. Addition is the basic arithmetic operation and is used in VLSI system as a full adder circuit extensively. It adds binary numbers and is the main part for other operations such as subtraction (complement addition), multiplication (successive addition) and

division (successive subtraction) etc. The overall performance of system is mainly dependent on adder performance. CMOS VLSI circuit is used for increasing no of portable application with limited amount of power available. VLSI design has been focusing high performance for microprocessor and system component. The research effort in low power microelectronic has been intensified demand in application such as personal computing device, wireless communication system. Medical application and other due to fast growth of battery operation all logic structure has a single-bit full adder as a main component in it. Adder cell effect the performance of logic structure most [6].

## II. FULL ADDER CIRCUITS

The Full-Adder (FA) is used widely in systems with operations such as counter, addition, subtraction, multiplication and division etc. It is the basic core component of Arithmetic-Logic-Unit (ALU). Thus, the innovation and acceleration of FA means that the speed of the Central-Processor-Unit [3]. Adder is the most important operation in any digital logic design. High speed and accurate operation of any digital system is influenced by its performance of the adder design. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function but suffers with power dissipation. The XOR gate using CMOS inverter and pass transistor and the conventional full adder and full adder design using dual sleep approach. These circuits are considered as the basic circuits in this paper. The size of the transistor is defined as a ratio of Width/Length (W/L). Ground bounce noise is estimated when the circuits are connected with a sleep transistor. Sub-threshold current is directly proportional to the Width/Length ratio of transistor [2].

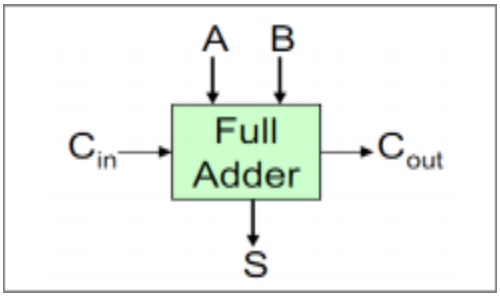
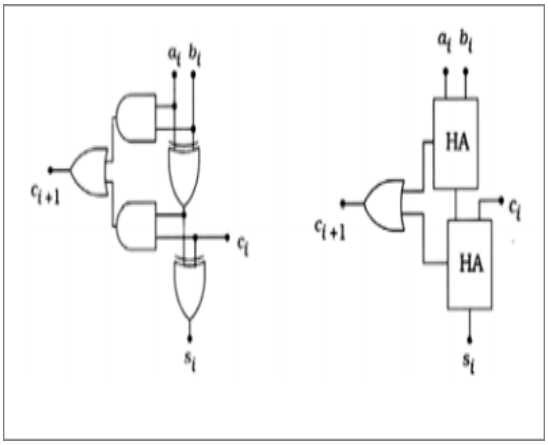



Fig.1-bit Full Adder Circuits

The most commonly used adder with complementary pull-up pMOS and pull-down nMOS networks in digital circuits is conventional 28 transistor full adder. A complementary static CMOS full adder circuit consists of an NMOS pull down network connecting the ground to the output and a dual pMOS pull up network connecting the power to the output. This adder implements the following Boolean equations [5]:

$$CARRY = A.B + B.Cin + A.Cin \ldots\ldots (1)$$




(a) Gate-level logic (b) HA based design

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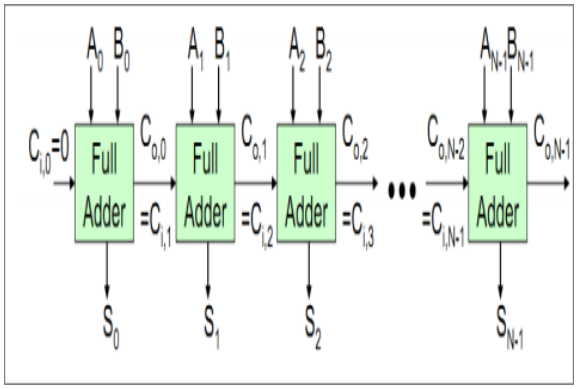



(b) Combinational Adder Fig.2 Full Adder Circuits

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires AND, OR gates. The basic logic diagram for full adder using its Boolean equations with basic gates can be represented as shown below [4].

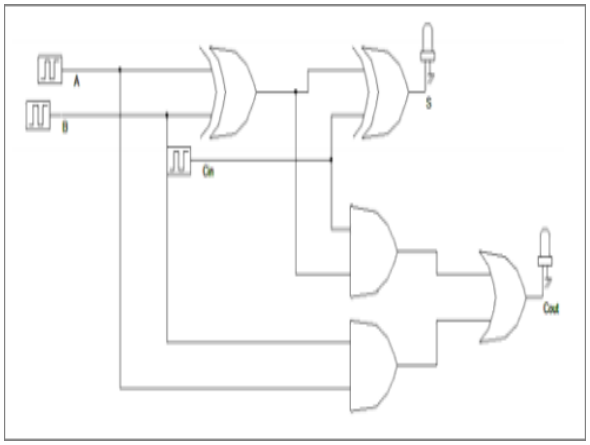


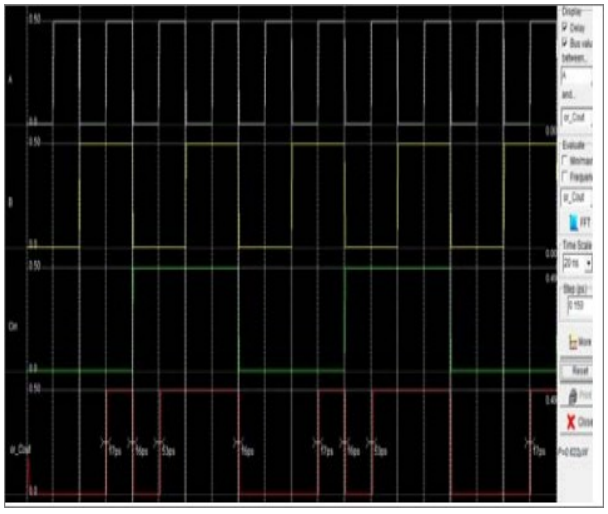

Fig.3 Schematic diagram of Full Adder

Table-1 Truth Table of Full Adder

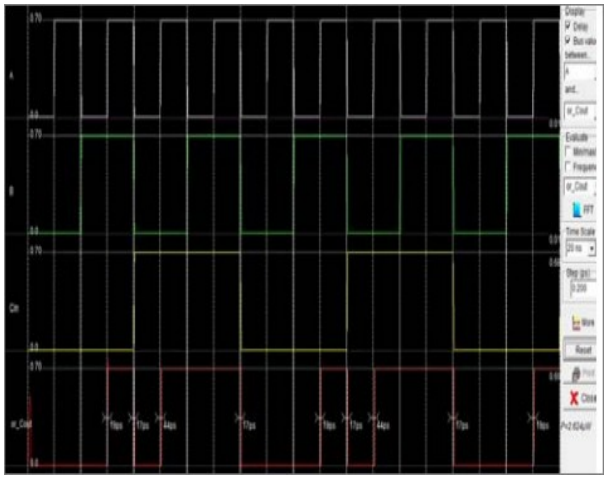
| A | B | $C_{in}$ | S | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## III. Results

The proposed 2-bit Full Adder are compared based on the performance parameters like surface area and power dissipation. To achieve better performance, the circuits are designed using CMOS process by Microwind 3.1 in 50nm, 70nm and 90 nm technology. The proposed 2-bit Full Adder circuit shown in figure 3, uses two 2-bit X-OR, one 2-bit OR and two 2-bit AND logic gates.



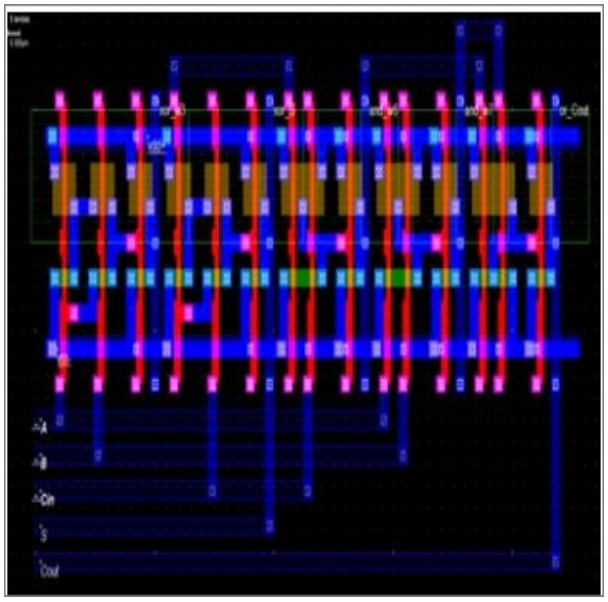
Output of proposed multiplier using 50 nm CMOS Technology



Output of proposed multiplier using 70 nm CMOS Technology.

LAYOUT SIMULATION.

Performance analysis of full adder is presented in this section. Designs are simulated using DSCH and MICROWIND Tools at different technologies like 90nm, 70nm, 50nm. The layout design rule describes how the small features can be and how closely they can be packed in particular manufacturing process. Different logical layers are used by the designers to generate the layout. There are specific layers for metal, contacts or diffusion areas, polysilicon. In the layout design red color presents polysilicon, green color indicates n+ diffusion, light green color indicates p+ diffusion, light and dark blue color.



Comparison table for Power.

| CMOS Technology / Parameters | 90 nm | 70 nm | 50 nm |
|---|---|---|---|
| Power (in µW) | 11.395 | 2.624 | 0.622 |
| Surface Area (in $\mu m^2$) | 72.5 | 35.5 | 18.1 |

## IV.CONCLUSION

The proposed 2-bit Adder is simulated with 50nm, 70nm and 90 nm CMOS technologies .The performance parameters power and surface area are compared. The proposed 2-bit Full Adder using the proposed logic in results reduction in the power and surface area. The power consumed by the circuit in 90nm, 70nm and 50nm CMOS technologies are 11.395 µW, 2.624 µW and 0.622 µW respectively. The surface area consumed by the circuit in 90nm, 70nm and 50nm CMOS technologies are 72.5 µm2, 35.5 µm2, and 18.1 µm2 respectively.

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