International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

Integrated Grid by Using Dual Voltage Source Inverter for Power Quality Improvement

K Govinda Rajulu[1], Kurakula Vimala Kumar[2], Thalluru Anil Kumar[3]
[1]M.Tech Student, [2]Assistant Professor, [3]Professor
[1,2]Dept. of EEE, JNTUA College of Engineering, Pulivendhula, Andhrapradesh, India
[3]Dept. of EEE, CVSR College of Engineering, Hyderabad, Telangana, India

Abstract

In this, we proposed a new concept for enhancing the power quality in unified grid system which is known as dual voltage source inverter. Our proposed approach consist of two converters, which permits the micro grid to trigger power generated by the distributed energy sources (DERs) as well as to compensate the neighborhood unbalanced and nonlinear load. This paper presents a dual current source inverter (DVSI) plan to boost the ability quality and reliability of the micro grid system. These DG models with coordinated control of local generation and storage facilities form a micro grid. Inside a micro grid, power from various renewable energy sources for example fuel cells, solar (PV) systems, and wind energy systems are interfaced to grid and loads using power electronic converters. The control algorithms are developed according to immediate symmetrical component theory (ISCT) to function DVSI in grid discussing and grid injecting modes. The suggested plan has elevated reliability, lower bandwidth dependence on the primary inverter, lower cost because of decrease in filter size, and usage of microgrid power while using the reduced electricity-link current rating for the main inverter. These functions result in the DVSI plan a promising option for micro grid offering sensitive loads. The topology and control formula are validated through extensive simulation results.

Keywords:-*Grid-connected inverter, instantaneous symmetrical component theory (ISCT), microgrid, power quality.*

1. Introduction

Inside a micro grid, power from various renewable energy sources for example fuel cells, solar (PV) systems, and wind energy systems are interfaced to grid and loads using power electronic converters. A grid interactive inverter plays an important role in swapping power in the micro grid to the grid and also the connected load [2]. Technological progress and ecological concerns drive the ability system to some paradigm shift with more renewable powers integrated towards the network by means of distributed generation (DG). These DG models with coordinated control of local generation and storage facilities form a micro grid [1]. This micro grid inverter can either operate in a grid discussing mode while offering a part of local load or perhaps in grid injecting mode, by injecting power to the primary grid. Maintaining power quality is yet another essential requirement which has to become addressed as the microgrid product is connected to the primary grid. The proliferation of power electronics devices and electrical loads with unbalanced nonlinear power has degraded the ability quality within the power distribution network. Furthermore, if there's a great deal of feeder impedance within the distribution systems, the propagation of these harmonic power distorts the current at the purpose of common coupling (PCC). In the same instant, industry automation has reached to an excellent degree of sophistication, w here plants like automobile manufacturing models, chemical industrial facilities, and semi conductor industries require clean power. Of these programs, it is important to compensate nonlinear and unbalanced load power [4].Load compensation and power injection using grid interactive inverters in micro grid happen to be presented within the literature. The primary focus of the jobs are to realize dual benefits within an inverter that will provide the active power injection from the photovoltaic system as well as works as an active power filter, paying unbalances and also the reactive power needed by other loads attached to the system. A distribution static compensator (DSTATCOM) is required for voltage regulation and for active power injection. The control scheme keeps the ability balance in the grid terminal during the wind versions using sliding mode control. This plan has got the capacity to inject power generated by WES also to perform like a harmonic compensator. The majority of the reported literature in this region discuss the topologies and control calculations to supply load compensation capability within the same inverter additionally for their active power injection. Whenever a grid-connected inverter can be used for active power injection and for load compensation, the inverter capacity that may be employed for experiencing this second objective is made the decision through the available immediate micro grid real power. Thinking about the situation of the grid-connected PV inverter, the accessible capacity from the inverter to provide the reactive power diminishes throughout the maximum solar isolation periods. In the same instant, the reactive capacity to regulate the PCC current is extremely needed during this time period. It signifies that supplying multi functionalities inside a single inverter degrades either the actual power injection or even the load compensation abilities. This paper demonstrates a dual current source inverter (DVSI) plan, where the power produced through the micro grid is injected just as real power through the primary current source inverter(MVSI) and also the reactive, harmonic, and unbalanced load compensation is carried out by auxiliary current source inverter(AVSI). It has a benefit the ranked capacity of MVSI can always be employed to inject real capacity to the grid, if sufficient renewable power can be obtained in the electricity link. Within the DVSI scheme, as total load power is provided by two inverters, power losses over the semiconductor switches of every inverter are reduced. This increases its reliability as in comparison to some single inverter with multifunctional abilities. Also, smaller size modular inverters can operate at high switching frequencies with a lower size interfacing inductor, the filter cost gets reduced. Furthermore, because the primary inverter is supply in real power, the inverter needs to track the essential positive sequence of current. This cuts down on the bandwidth requirement of the primary inverter. The inverters within the suggested plan use two separate electricity links. Because the auxiliary inverter is supplying zero sequence of load current, a 3-phase three-leg inverter topology having a single electricity storage capacitor may be used for the primary inverter. Therefore cuts down on the electricity-link voltage requirement from the primary inverter. Thus, using two separate inverters within the suggested DVSI plan provides increased reliability, better usage of micro grid power, reduced dc grid current rating, less bandwidth dependence on the main inverter, and reduced filter size. Control calculations are developed by immediate shaped component theory(ISCT) to function DVSI in grid-connected mode, while considering non-stiff grid current. The extraction of fundamental positive sequence of PCC current is completed by dq0transformation. The control technique is examined with two parallel inverters linked to a 3-phase four-wire distribution system. Effectiveness from the suggested control formula is validated through detailed simulation and experimental results.

2. Dual Voltage Source Inverter

A. System Topology

A. System Topology:-The suggested DVSI topology is proven in Fig. 1. It consists of an unbiased point clamped (UPC) inverter to understand AVSI and a 3-leg inverter for MVSI. They are connected to grid in the PCC and offering a nonlinear and unbalanced load. The part from the AVSI would be to compensate the reactive, harmonics, and unbalance components in load power. Here, load power in three phases is symbolized by ila, ilb, and ilc, correspondingly. Also, ig(abc), iμgm(abc), and iμgx(abc) show grid currents, MVSI power, and AVSI power in three phases, correspondingly. The electricity link from the AVSI relies on a split capacitor topology, with two capacitors C1 and C2. The MVSI delivers the available power at distributed energy resource (DER)to grid. The DER could be a electricity source or perhaps an ac source with rectifier combined to electricity link. Usually, alternative energy sources like fuel cell and PV generate power at variable low electricity current, as the variable speed wind generators generate power at variable ac current.

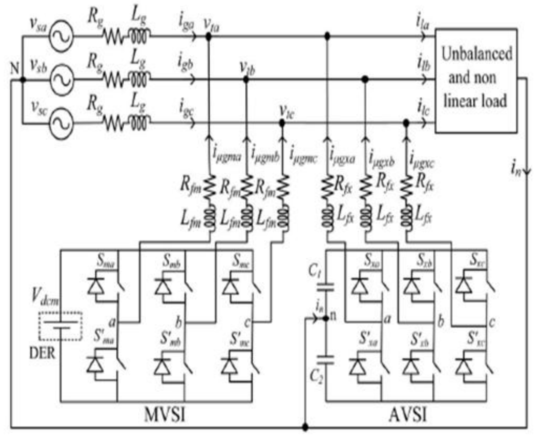

Fig.1. Proposed Dual voltage source Inverter scheme

Therefore, the ability produced from these sources make use of a power conditioning stage prior to it being connected to the input of MVSI. Within this study, DER is being re presented like a electricity source. An inductor filter can be used to eliminate the high-frequency switching components produced duet o the switching of power electronic switches within the inverters. The machine considered within this study is assumed to have some quantity of feeder resistance Rg and inductance Lg. Due to the existence of this feeder impedance, PCC current is affected with harmonics.

B. Design of DVSI Parameters

AVSI: The important parameters of AVSI like dc-link voltage (Vdc), dc storage capacitors (C1 and C2), interfacing inductance (Lfx) and hysteresis band (±hx) are selected based on the design method of split capacitor DSTATCOM topology. The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage. The total dc-link voltage reference (Vdcref) is found to be 1040 V. Values of dc capacitors of AVSI are chosen based on the change in dc-link voltage during transients. Let total load rating is S KVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to S KVA. AVSI needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the system time period. Hence, maximum energy exchange by AVSI during transient will be nST. This energy will be equal to change in the capacitor stored energy. Therefore

$$\frac{1}{2}C_1(V_{dcr}^2 - V_{dc1}^2) = nST \quad (1)$$

where Vdcr and Vdc1 are the reference dc voltage and maximum permissible dc voltage across C1 during transient, respectively. Here, S = 5 KVA, Vdcr = 520 V, Vdc1 = 0.8 ∗Vdcr or 1.2 ∗Vdcr, n = 1 and T = 0.02 s. Substituting these

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

values in (1), the dc-link capacitance (C1) is calculated to be 2000 μF. same value of capacitance is selected for C2. The interfacing inductance is given by

$$L_{fx} = \frac{1.6\ Vm}{4\, h_x\, f_{max}} \qquad (2)$$

Assuming a maximum switching frequency (Fmax) of 10 kHz and hysteresis band (hx) as 5% of load current (0.5 A), the value of Lfx is calculated to be 26 mH.

MVSI: The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as 1.15 ∗Vml, where Vml is the peak value of line voltage. This is calculated to be 648V. Also, MVSI supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI. In this analysis, a filter inductance (Lfm) of 5mH is used.

3. Control Strategy for DVSI Scheme

3.1. Fundamental Voltage Extraction

The control algorithm for reference current generation using ISCT requires balanced sinusoidal PCC voltages. Because of the presence of feeder impedance, PCC voltages are distorted. Therefore, the fundamental positive sequence components of the PCC voltages are extracted for the reference current generation. To convert the distorted PCC voltages to balanced sinusoidal voltages, dq0 transformation is used.

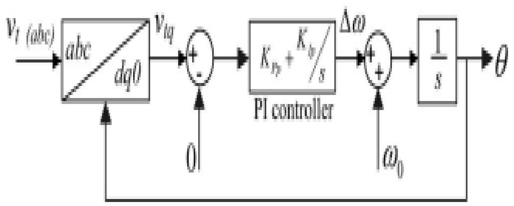

Fig. 2 Schematic Diagram of PLL

The PCC voltages in natural reference frame (Vta, Vtb, and Vtc) are first transformed into dq0 reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix}$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}.$$

In order to get θ, a modified synchronous reference frame (SRF) phase locked loop (PLL) is used. The schematic diagram of this PLL is shown fig.2. It mainly consists of a proportional integral (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-axis (vtq) is compared with 0 V and the error voltage thus obtained is given to the PI controller. The frequency deviation Δω is then added to the reference frequency ω0 and finally given to the integrator to get θ. It can be proved that, when, θ = ω0 t and by using the Park's transformation matrix (C), q-axis voltage in dq0 frame becomes zero and hence the PLL will be locked to the reference frequency (ω0). As PCC voltages are distorted, the transformed voltages in dq0 frame (Vtd and Vtq) contain average and oscillating components of voltages. These can be represented as

$$v_{td} = \overline{v_{td}} + \widehat{v_{td1}}, v_{tq} = \overline{v_{tq}} + \widehat{v_{tq}}$$

where Vtd and Vtq represent the average components of Vtd and Vtq, respectively. The terms Vtd and Vtq indicate the oscillating components of Vtd and Vtq, respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation as given by

$$\begin{bmatrix} v_{ta1}^{+} \\ v_{tb1}^{+} \\ v_{tc1}^{+} \end{bmatrix} = C^T \begin{bmatrix} \overline{v_{td}} \\ \overline{v_{tq}} \\ 0 \end{bmatrix}$$

These voltages v+ ta1, v+ tb1, and v+ tc1 are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

3.2. Instantaneous Symmetrical Component Theory

ISCT was developed primarily for unbalanced and nonlinear load compensations by active power filters. The system topology shown in fig.3 is used for realizing the reference current for the compensator. The ISCT for load compensation is derived based on the following three conditions.

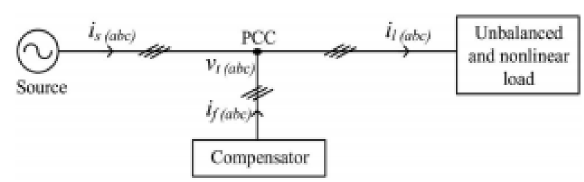

Fig. 3 Schematic of an Unbalanced and Nonlinear Load Compensation Scheme

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0$$

2) The phase angle between the fundamental positive sequence voltage (v+ ta1) and source current (isa) is φ< v_{ta1}^{+} =< $i_{sa} + \emptyset_0$

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta1}^{+} i_{sa} + v_{tb1}^{+} i_{sb} + v_{tc1}^{+} i_{sc} = p_1$$

Solving the above three equations, the reference source currents can be obtained as

$$i_{sa}^{*} = \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) p_1$$

$$i_{sb}^{*} = \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{ta1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) p_1$$

$$i_{sc}^{*} = \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) p_1$$

where β = tan√ φ 3 . The term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute β = 0. Thus, the reference source currents for three phases are given by

$$i^*_{s(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) p_1$$

Where i∗sa, i∗sb, and i∗ sc are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power Pl. The power Pl can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_1 = \frac{1}{T}\int_{t_1-T}^{t1} (v^+_{ta1} i_{la} + v^+_{tb1} i_{lb} + v^+_{tc1} i_{la})\, dt$$

where t1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i^*_{f(abc)} = i_{l(abc)} - i^*_{(abc)}$$

Above equation can be used to generate the reference filter currents using ISCT, when the entire load active power, Pl is supplied by the source and load compensation is performed by a single inverter.

A modification in the control algorithm is required, when it is used for DVSI scheme. The following section discusses the formulation of control algorithm for DVSI scheme. The source currents, is(abc) and filter currents if(abc) will be equivalently represented as grid currents ig(abc) and AVSI currents iμgx(abc), respectively, in further sections.

3.3. Control Strategy of DVSI

Control strategy of DVSI is developed in such a way that grid and MVSI together share the active load power, and AVSI supplies rest of the power components demanded by the load.

1) Reference Current Generation for Auxiliary Inverter: The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as Ploss should also be supplied by the grid. An expression for Ploss is derived on the condition that average dc capacitor current is zero to maintain a constant capacitor voltage. The deviation of average capacitor current from zero will reflect as a change in capacitor voltage from a steady state value. A PI controller is used to generate Ploss term as given by

$$P_{Loss} = k_{pr} e_{vdc} + k_{lv} \int e_{vdc} dt$$

Where evdc = Vdcref − Vdc, Vdc represents the actual voltage sensed and updated once in a cycle. In the above equation, KP V and KI V represent the proportional and integral gains of dc-link PI controller, respectively. The Ploss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given. Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change

$$i^*_{\mu gxa} = i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(p_1 + p_{loss})$$

$$i^*_{\mu gxb} = i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(p_1 + p_{loss})$$

$$i^*_{\mu gxc} = i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(p_1 + p_{loss})$$

2) Reference Current Generation for Main Inverter: The MVSI supplies balanced sinusoidal currents based on the available renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER (Pμg). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c)

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) p_{\mu g}$$

where Pμg is the available power at the dc link of MVSI. The reference currents obtained from above equations are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop, usually with a two-level comparator. This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation. A hysteresis controller is a high-gain proportional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed-loop system stability. The entire Control strategy is schematically represented in fig.4.

Applying Kirchhoff's current law (KCL) at the PCC

$$i_{\mu gxj} = i_{lj} - (i_{gj} + i_{\mu gmj}), for\ j = a, b, c$$

By using above equations an expression for reference grid current in phase-a (i∗ga) can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)[(p_1 + p_{loss}) - p_{\mu g}]$$

It can be observed that, if the quantity (Pl + Ploss) is greater than Pμg, the term [(Pl + Ploss) − Pμg] will be a positive quantity, and i∗ga will be in phase with v+ ta1. This operation can be called as the grid supporting or grid sharing mode, as the total load power demand is shared between the main inverter and the grid. The term, Ploss is usual very small compared to Pl. On the other hand, if (Pl + Ploss) is less than Pμg, then [(Pl + Ploss) − Pμg] will be a negative quantity, and hence i∗ga will be in phase opposition with v+ ta1. This mode of operation is called the grid injecting mode, as the excess power is injected to grid.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

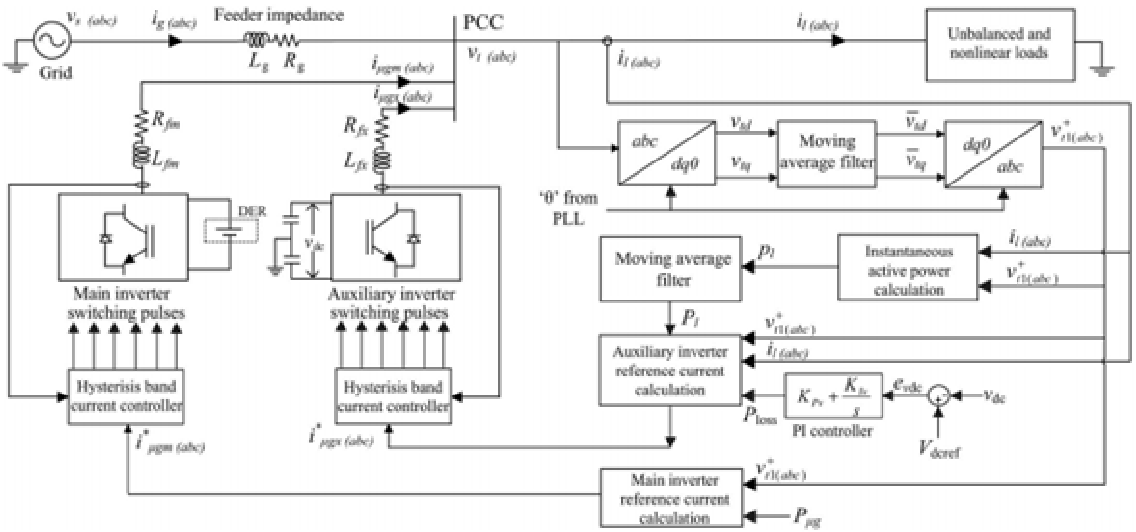

Fig.4 Schematic Diagram Showing the Control Strategy of Proposed DVSI Scheme

4. Simulation Results

The simulation model of DVSI scheme shown in Fig. 1 is developed in MATLAB to evaluate the performance. The simulation parameters of the system are given in Table I. The simulation study demonstrates the grid sharing and grid injecting modes of operation of DVSI scheme in steady state as well as in transient conditions.

TABLE I
SYSTEM PARAMETERS FOR SIMULATION STUDY

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 µF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	$Z_{la} = 35 + j19$ Ω $Z_{lb} = 30 + j15$ Ω $Z_{lc} = 23 + j12$ Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

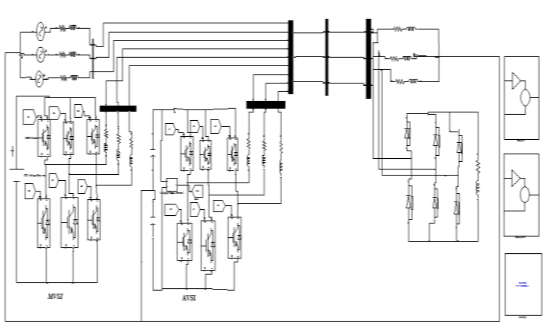
Fig. 5 Proposed simulation diagram

During this period, the microgrid is operating in grid sharing mode. At t = 0.4 s, the microgrid power is increased to 7 kW, which is more than the load demand of 6 kW. This microgrid power change is considered to show the change of operation of MVSI from grid sharing to grid injecting mode. Now, the excess power of 1 KW is injected to grid and hence, the power drawn from grid is shown as negative.

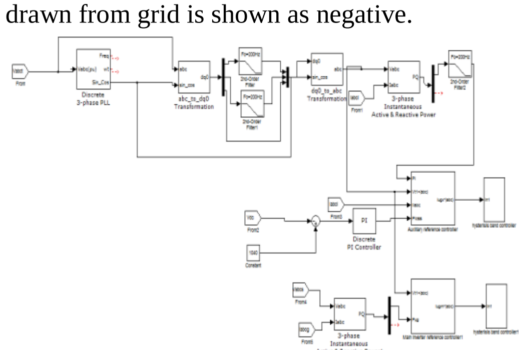
Fig. 6 Proposed Control Circuit

Figure 11-13 shows the load reactive power (Ql), reactive power supplied by AVSI (Qx), and reactive power supplied by MVSI (Qµg), respectively. It shows that total load reactive power is supplied by AVSI, as expected. Fig.14-18 shows the plots of load currents (il(abc)), currents drawn from grid (ig(abc)),currents drawn from MVSI (iµg(abc)), and currents drawn from the AVSI (iµx(abc)), respectively.

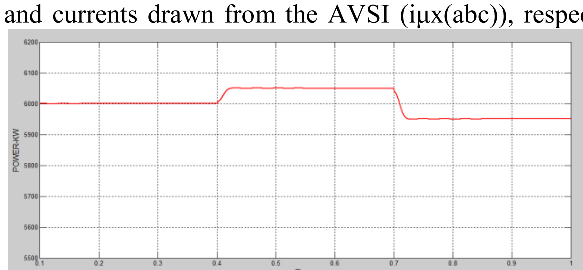
Fig.7 Active Power Sharing (a) Load Active Power

International Journal of Research
Available at https://edupediapublications.org/journals

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

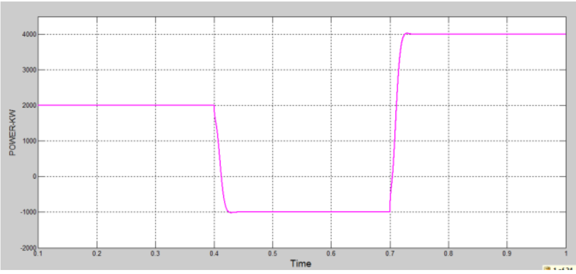

Fig.8 Active Power Sharing (b) Active Power Supplied by Grid

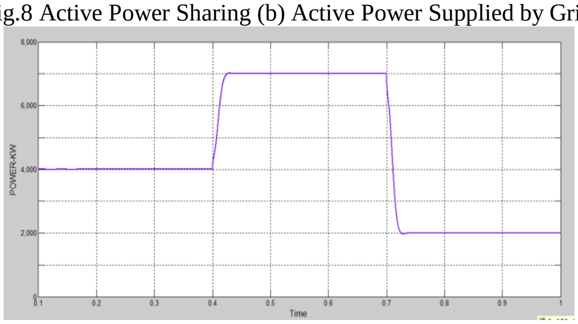

Fig.9 Active Power Sharing (c) Active Power Supplied by MVSI

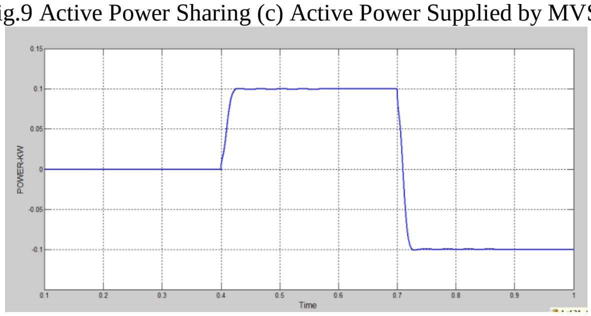

Fig.10 Active Power Sharing (d) Active Power Supplied by AVSI

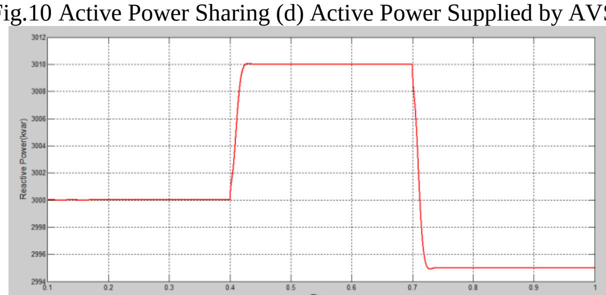

Fig.11 Reactive Power Sharing (a) Load Reactive Power

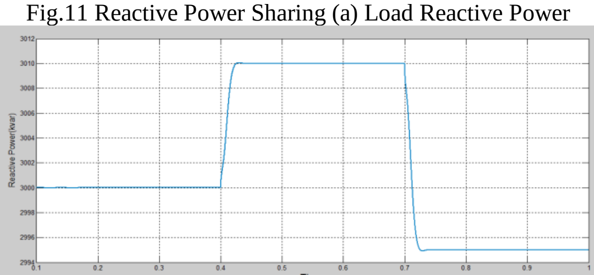

Fig.12 Reactive Power Sharing (b) Reactive Power Supplied by AVSI

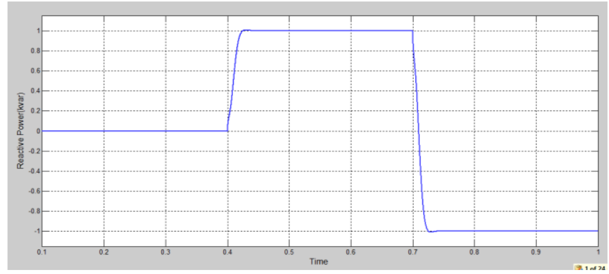

Fig.13 Reactive Power Sharing (c) Reactive Power Supplied by MVSI

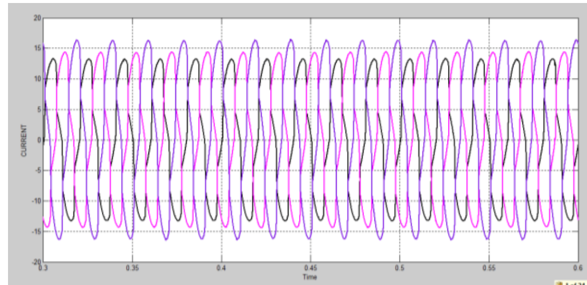

Fig.14 Simulated Performance of DVSI Scheme (a) Load Currents

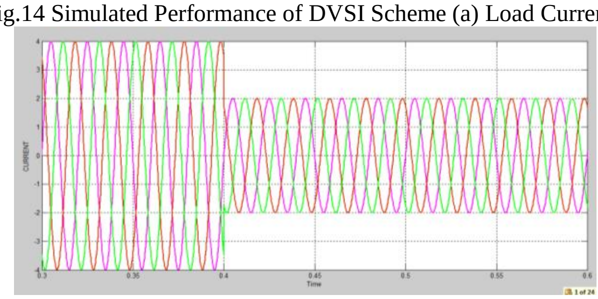

Fig.15 Simulated Performance of DVSI Scheme (b) Grid Currents

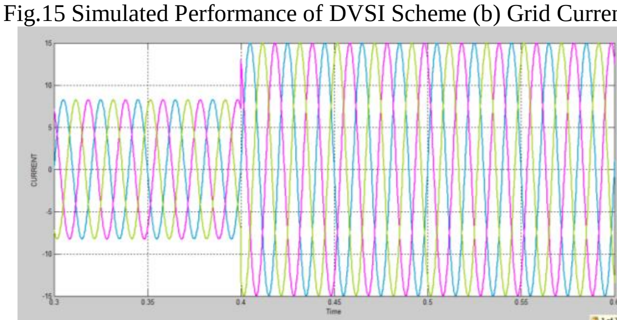

Fig.16 Simulated Performance of DVSI Scheme (c) MVSI Currents

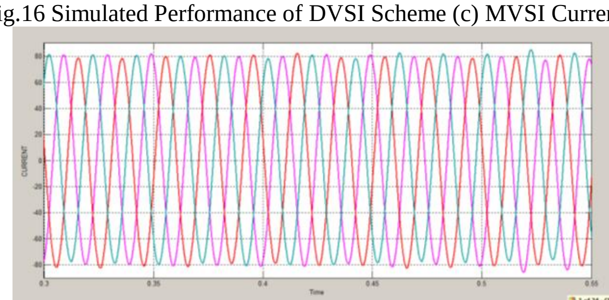

Fig.17 Simulated Performance of DVSI Scheme (d) AVSI Currents

International Journal of Research
Available at https://edupediapublications.org/journals

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

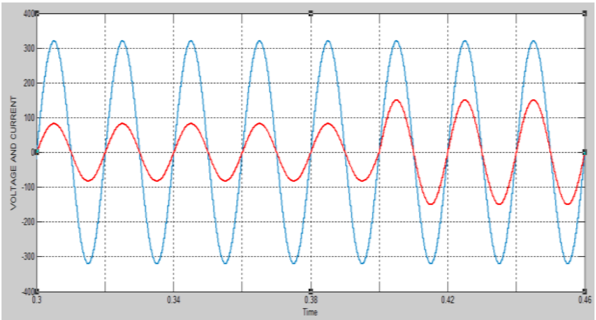

Fig.18 Grid Sharing and Grid Injecting Modes of Operation (b) PCC Voltage and MVSI Current (phase-α)

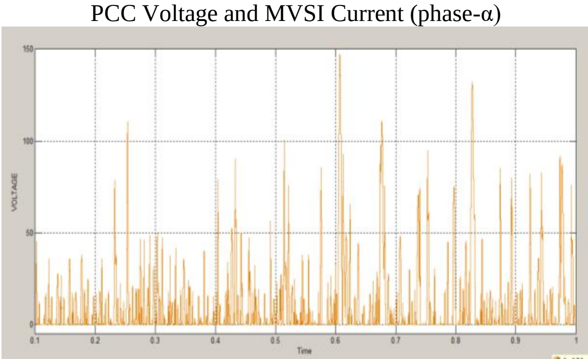

Fig.19 DC-Link Voltage of AVSI

The dc-link voltage is shown in Fig.5.9 (a) and (b). These figures indicate that the voltage is maintained constant at a reference voltage (Vdcref) of 1040 V by the PI controller. All these simulation results presented above demonstrate the feasibility of DVSI for the load compensation as well as power injection from DG units in a microgrid.

Table.2 System Parameters for Simulation Study

Parameters	Values
Source voltage	50 V L-N (rms), 50 Hz
Feeder impedance	$R_g = 0.5\,\Omega$, $L_g = 1.0$ mH
Reference DC-link voltage of AVSI	$V_{dcref} = 220$ V
DC-link capacitance of AVSI	$C_1 = C_2 = 4700$ μF
DC-link voltage of MVSI	$V_{dcm} = 150$ V
PI gains of DC-link voltage controller	$K_{Pv} = 80$, $K_{Iv} = 0.08$
Hysterisis band (h)	$\pm\, 0.15\, A$
Interfacing inductor (AVSI)	R_{fx}= 0.5 Ω, L_{fx}= 10 mH
Interfacing inductor (MVSI)	R_{fm}= 0.5 Ω, L_{fm}= 5 mH
Unbalanced linear load	$Z_{la} = 24 + j16\ \Omega$ $Z_{lb} = 36 + j16\ \Omega$ $Z_{lc} = 64 + j21\ \Omega$
Nonlinear load	3 ϕ diode bridge rectifier with a dc current of 2.4 A

5. Conclusion

Control calculations are developed to generate reference power for DVSI using ISCT. A DVSI plan is suggested for micro grid systems with enhanced power quality. Furthermore, using three-phase, three wire topology for that primary inverter cuts down on the electricity-link voltage requirement. The proposed scheme has got the capacity to switch power from distributed generators (DGs) also to compensate the neighborhood unbalanced and nonlinear load. The performance from the suggested scheme has been validated through simulation and experimental studies. As in comparison one inverter with multifunctional abilities, a DVSI has numerous advantages for example, increased reliability, less expensive because of the decrease in filter size, and more usage of inverter ability to inject real power from DGs to micro grid. Thus, a DVSI plan is really a appropriate interfacing option for micro grid offering sensitive loads.

References

[1] N. R. Tummuru, M. K. Mishra, and S. Srinivas, "Multifunctional VSCcontrolled microgrid using instantaneous symmetrical components theory,"*IEEE Trans. Sustain. Energy*, vol. 5, no. 1, pp. 313–322, Jan.2014.

[2] M. Singh, V. Khadkikar, A. Chandra, and R. Varma, "Grid interconnectionof renewable energy sources at the distribution level withpower-quality improvement features," *IEEE Trans. Power Del.*, vol. 26,no. 1, pp. 307–315, Jan. 2011.

[3] P. Rodriguez *et al.*, "A stationary reference frame grid synchronizationsystem for three-phase grid-connected power converters under adversegrid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 99–112,Jan. 2012.

[4] X. Yu and A. Khambadkone, "Reliability analysis and cost optimizationof parallel-inverter system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10,pp. 3881–3889, Oct. 2012.

[5] A. Ghosh and G. Ledwich, "Load compensating DSTATCOM in weakAC systems," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1302–1309,Oct. 2003.

[6] M. Hamid, A. Jusoh, and M. Anwari, "Photovoltaic plant with reducedoutput current harmonics using generation-side active power conditioner,"*IET Renewable Power Gener.*, vol. 8, no. 7, pp. 817–826, Sep.2014.