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Area Reduction Exclusive OR/NOR Design Using SCDM

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Abstract

The XOR/XNOR logic gates plays a crucial job in digital circuits which are full adders, compressors, parity generators and comparators. These logic gates are taken in critical path of these systems, which considerably influenced the system characteristics. An optimized layout is desired to neglect any degradation at the output voltage, devour much less power, and feature a less wide variety of transistors to implement the circuit. Two distinct approaches of three-input exclusive-OR (XOR) feature at transistor stage with a systematic cell design methodology (SCDM) are proposed in this paper. For low power and high speed (LPHS) applications, these approaches are well desirable. The proposed designs comprises low dynamic and short-circuit power consumption and their internal nodes scatter negligible leakage power, which ends up in low average power consumption. Those designs are used to improve the overall performance, voltage ranges, and the driving functionality and decreasing the quantity of transistors in the primary structure of the designs. By using MICROWIND/DSCH 180 nm technology two different approaches of 3-input XOR/XNOR circuits are designed and simulation results are generated by the usage of HSPICE 180 nm technology. In terms of speed, power consumption and transistor count the performance of proposed circuits are better than existing circuits.

Keywords: SCDM, leakage power, critical path, LPHS.

I. Introduction

Circuit realization for low power and low area has appeared as a paramount problem with the magnification of integrated circuit towards very excessive integration density and high running frequencies. Because of the paramount position performed through XOR and XNOR gate in specific circuits particularly in arithmetic circuits, optimized layout of XOR and XNOR circuit to gain low power, small size and delay is wanted. The most important challenge to design XOR/XNOR circuit is to gather complete yield output voltage swing and less variety of transistors to execute it. This paper makes use the concept of SCDM concept for the designs of 3 input XOR/XNOR gate.

[1]Based on our target the SCDM considers circuit accretion in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It ought to be noted that BDD can be applied for EBC creation of different 3-input functions. It stands as a honest overall performance metric, exactly regarding portable electronic system targets. The incentive to use this concept is the presence of a few precise capabilities and the potential to provide a few efficient circuits that enjoy these kinds of advantages.

1) The SCDM partitions the circuit structure into a major structure and optimization-correction mechanisms. In the essential structure, it considers capabilities including the least count of transistors in critical path, pretty balanced outputs, being power ground-free, and symmetry. The mechanisms have the obligation of completing the functionality of the circuits, fending off any degradation at the output voltage, and growing the driving functionality.

2) The least wide variety of transistors in critical path will increase the chances of the circuit to have better characteristics, as experimental outcomes have proven a mean saving of 10%–50% and 27%–77% in phrases of delay and energy-delay Product (EDP), respectively.

3) The dynamic consumption optimization comes from the reality of well-balanced propagation delay. This selection is effective for programs in which the skew between arriving signals is vital for proper operation,

and for cascaded applications to reduce the danger of creating system defects [3].

4) power-ground-free principal structure results in power reduction.

5) Symmetrical structure, high modularity, and normal association of designs deliver rise to sharing greater wells of connected transistors and in turn reducing the occupied area about 26%–32%.

6) The degradation in all output voltage swing can for this reason be completely eliminated, which makes the layout sustainable in low VDD operations and less static power dissipation.

The properly-prepared systematic method leads to automated drift, which can reduce design time and prices, provide consistency within the cell library generation process, growth the variety of simulation talents on the characteristics step, as well as reduce the danger of errors.

In this paper, new approaches of XOR-XNOR gate are suggested. The paper is prepared as follows: in segment II, previous work is reviewed. Eventually, in segment III, the proposed design of XOR-XNOR gate is provided. In segment IV, the simulation consequences are given and mentioned. Ultimately a conclusion will be made within the final segment.

II. Previous work

There are various approaches and designs of 3-input XOR which is discussed in various papers at state of the art level and process and circuit level. The SCDM concept was used in "ENERGY AND AREA EFFICIENT THREE 3 INPUT XOR/XNOR CIRCUITS" proposed by T.Nikoubin, M.Grailoo, C.Li. The three circuits are XO4, XO7, and XO10. XO4 consists of 16 transistors, and the avg_power is 2.9µw at 1.2 V. XO7 consists of 16 transistors, and the avg_power is 3.17µw. XO10 consists of 18 transistors, and the avg_power is 3.07µw [1]. By using BSIMv3 model in HSPICE based on the TSMC 0.13µm CMOS technology all the circuits are simulated and to an impartial evaluation sized using SEA for PDP in 0.8-1.6 V VDD. These circuits appreciate higher driving capacity, transistor density, noise invulnerability with low-voltage operation, and minimal probability to deliver glitches, as an interesting element, the critical path of the exhibited designs comprises of just two transistors, which causes low propagation delay. Based on TSMC 0.13µm technology they also exhibiting 27%-77% reduction in average energy-delay product in HSPICE simulation.

III. PROPOSED METHOD

Two different approaches for three input XOR/XNOR circuits are:

a) One approach gives full output voltage swing operation for all input combinations using HSPICE and MICROWIND simulation based on TSMC 0.18 µm technology.
b) Another approach gives minimum transistor count compared to previous circuits and also full output voltage swing using HSPICE and MICROWIND based on 0.18 µm technology.

a) New approach for full output voltage swing:

Initially, the design starts with the main structure of three input XOR gate logic. First, we design 2 input XOR gate.

$$Y=A \oplus B \qquad (1)$$

2-input XOR gate is designed using two NAND gates and one inverter. Two NAND gates are designed as 2-input XNOR gate. The output of 2-input XNOR gate is given to inverter then 2-input XOR gate is formed. This output is given to similar 2-input XOR gate.

Then third input is added to this expression.

$$Y= (A \oplus B) \oplus C \qquad (2)$$

The output will be

$$Y= \overline{A \oplus B \oplus C} \qquad (3)$$

To this structure an inverter is added to get XOR

$$Y= A \oplus B \oplus C \qquad (4)$$

In this type of design, main structure is reusable.

The following design shows three input XOR/XNOR circuit of proposed method.

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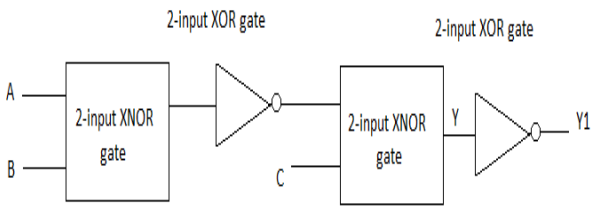

Fig. 1 Three input XOR/XNOR circuit diagram.

This Figure consists of A, B and C inputs and Y and Y1 outputs. In this figure, two outputs i.e. Y output indicates 3-input XNOR gate and Y1 output indicates 3-input XOR gate. The operation of block diagram can be explained through truth table of 3-input XOR/XNOR Gate.

Table: 1 Truth table of 3-input XOR/XNOR Gate is Seen in table.

A	B	C	Y	Y1
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

The table-1 mainly tales about basic operation of 3-input XOR/XNOR Gate. By using truth table, The basic operation of 3-input XOR Gate output is '1' when we can apply the odd number of input ones and output is '0' when we can apply the even number input ones and the basic operation of 3-input XNOR Gate output is '0' When we can apply odd number input ones and output is '1' when we can apply even number of input ones.

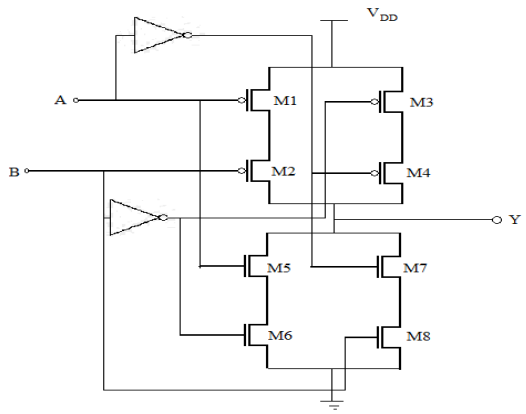

Fig: 2 Two-input XNOR Gate

The circuit diagram of 2-input XOR Gate is illustrated in fig 2.

b) New circuit design with less number of transistors:

In this proposed method we can design 3-input XOR/XNOR Gate by using 8 transistors so compare to existing method we reduce to half of the transistors. In Fig: 3 two outputs Y and Y1 are obtained. Y is the output of 3-input XOR Gate and Y1 is output of 3-input XNOR Gate.

Figure 3 shows the circuit diagram of proposed method

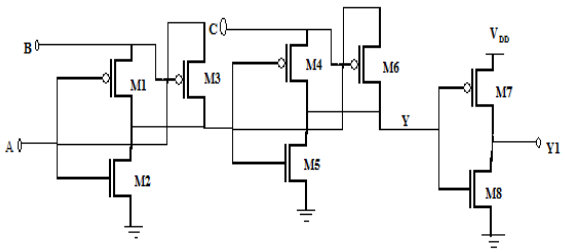

Fig: 3 Three-input XOR/XNOR Gate

See table: 2, which mainly explains how to operate the circuit depends on input sequence.

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Table: 2 proposed method Transistor ON/OFF conditions depend on input.

A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	Y	Y1
0	0	0	ON	OFF	ON	ON	OFF	ON	ON	OFF	0	1
0	0	1	ON	OFF	ON	ON	OFF	OFF	OFF	ON	1	0
0	1	0	ON	OFF	OFF	OFF	ON	ON	OFF	ON	1	0
0	1	1	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	0	1
1	0	0	OFF	ON	ON	OFF	ON	ON	OFF	ON	1	0
1	0	1	OFF	ON	ON	ON	OFF	OFF	ON	OFF	0	1
1	1	0	OFF	ON	OFF	ON	OFF	ON	ON	OFF	0	1
1	1	1	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	1	0

IV. SIMULATION RESULTS

Performance of the proposed designs can be examined in this section. Here simulation results of proposed designs are generated by using MICROWIND/DSCH tool based on 0.18µm CMOS technology and HSPICE tool based on 0.18µm technology.

The simulated outputs of 3-input XOR/XNOR gate as shown in below figures.

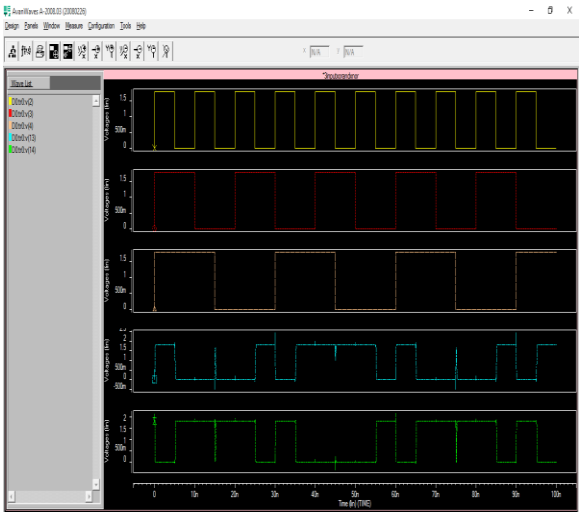

Fig.4 simulation results of 3-input XOR/XNOR gate for first approach.

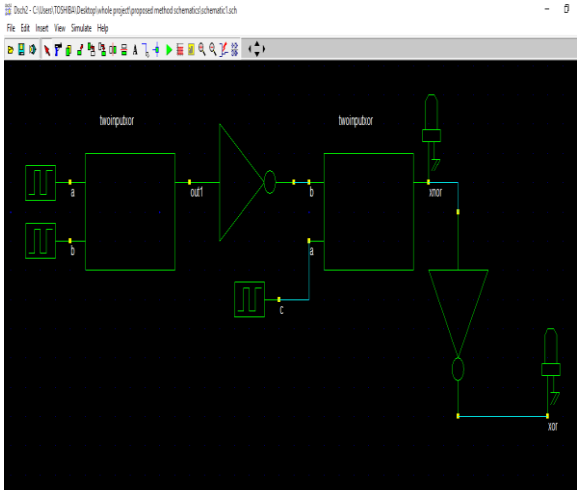

Fig.5 schematic diagram for first approach.

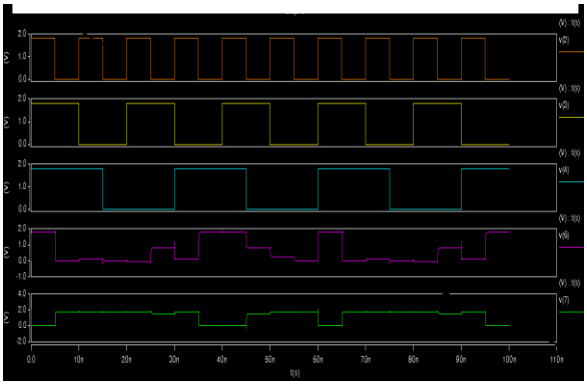

Fig.6 simulation results for 3-input XOR/XNOR gate for second approach.

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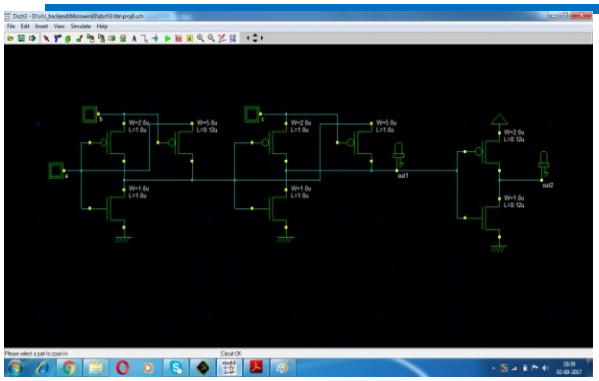

Fig. 7 schematic diagram for second approach

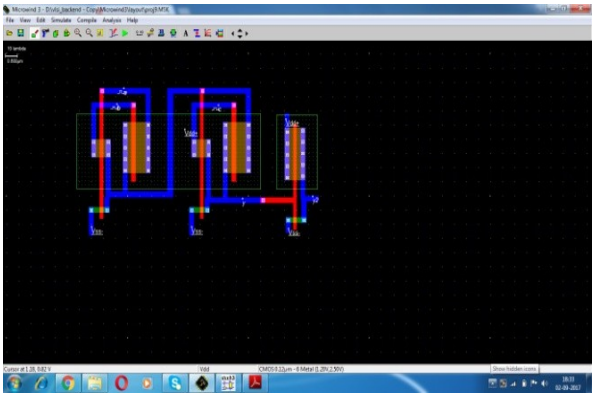

Fig. 8 layout for second approach

V. Conclusion

This paper comprises two new approaches of 3-input XOR/XNORs. First approach uses two 2-input XOR gates. Here 2-input XOR gate is reusable. This approach gives full output voltage swing. In this approach, transistors count is high comparatively. Second approach consists 8 transistors, in which output section contains inverter. These approaches are designed by using SCDM concept, which simplifies the circuit for better operation. The proposed designs have good signal level outputs and the best driving capability. By observing the simulation results of both the designs, these are better and more competitive than existing ones. Simulation results are compared by using HSPICE tool.

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