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Fuzzy Based Interline Unified Power Quality Conditioner Using Ten-Switch Topology

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ABSTRACT-*This paper proposes a new topological configuration for a unified power quality conditioner (UPQC) with fuzzy logic controller. The fuzzy controller is a rule based system with 0 and 1 operation with limited number of switches so it will reduce the power losses and maintain the better power quality. Here we are using the fuzzy logic controller. Such as, the fuzzy controller is the most suitable for the human decision – making mechanism , providing the operation of an electronic system with decisions of experts. Generally the structure of three-phase-three-wire UPQC consists of two back-to-back connected six switch inverters. But for this topology out of 12 switches, six of the series will be under-utilized most of the time. To improve the semiconductor utilization and consequently to reduce the total number of switches count, this topology proposes a new reduced switch topology for UPQC. This paper is realized using only ten switches and retains all the performance merits of the twelve-switch UPQC while minimizing its underutilization without increasing the switch VA rating. The paper provides a detailed analytical study and evaluation by comparing the proposed topology with the twelve and nine switches based UPQC system configurations. The feasibility of the proposed topology is validated through simulation investigation.*

Index Terms— Ten-switch converter, zero sequence, power quality, unified power quality conditioner (UPQC), voltage sag, fuzzy controller.

INTRODUCTION

THE ever increasing use of solid state technology in industrial and domestic applications is extensively contributing towards line current harmonics, leading to nonlinear voltage drops, cables overheating, poor power factor and additional power losses at distribution levels [1]-[2]. To mitigate these problems and maintain the reliability of the delivered power within acceptable margins, stringent power quality standards are put into practice [3].

A UPQC generally consists of two voltage source inverters (VSI), connected in shunt and series configuration with the grid, at the point of common coupling (PCC) and share a common dc link capacitor [4]. The series VSI protects the downstream loads from sags/swells in the PCC voltage whereas the shunt VSI reduces the upstream line losses by compensating the harmonic distortion and reactive component of the load current. When the voltage at PCC is distorted, the series VSI can be additionally controlled to mitigate and prevent the voltage harmonics from reaching the load [10]. There is an extensive literature available on UPQC and a detailed review can be found in [4].

This paper proposes a new reduced switch UPQC system topology that comprises of ten switches in total. The main objective is to reduce the overall switch count of the back-toback UPQC system while retaining its operational features without any performance tradeoff. To maintain the linear modulation range and uniform switching frequency for all the switches within the proposed topology, a carrier based double zero sequence injection scheme is also developed. An appropriate control algorithm is developed to achieve the seamless operation of the proposed UPQC topology under different operating conditions. An experimental study is carried out to validate the performance of the proposed topology.

THREE PHASE THREE WIRE UPQC SYSTEM CONFIGURATIONS

For three-phase-three-wire system, generally, the back-toback inverter based UPQC system is widely used and is shown in Fig. 1. It comprises of twelve power semiconductor switches in total. Switches $S_{A1}, S_{B1}, S_{C1}, S_{A2}, S_{B2}, S_{C2}$ constitute the shunt VSI which is connected at the PCC, where as,$S_{A1}{}^{1}, S_{B1}{}^{1}, S_{C1}{}^{1}, S_{A2}{}^{1}, S_{B2}{}^{1}, S_{C2}{}^{1}$, the switches constitute the series VSI and is connected between the PCC and load. Both inverters share the common dc link capacitor. As shown in Fig. 1, the twelve-switch UPQC deploys two dedicated inverters for performing the UPQC functionalities.

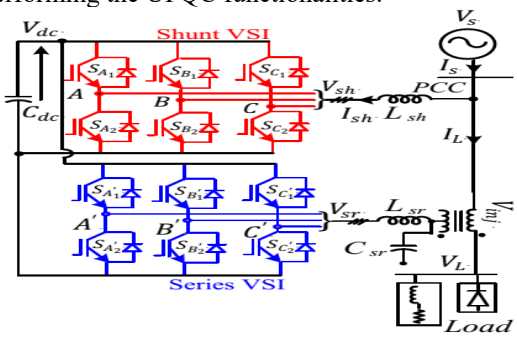

Fig. 1. Twelve-switch UPQC topology.

This feature allows UPQC to have shunt VSI connected at either the PCC or load with no effect on the compensation ability.

Recently, there has been an effort to reduce the total switch count of the UPQC. By merging the lower

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three switches of the shunt VSI and upper three switches of the series VSI in Fig. 1, the reduced nine-switch UPQC topology is achieved in . This configuration has a set of three shared switches as illustrated in Fig. 2.

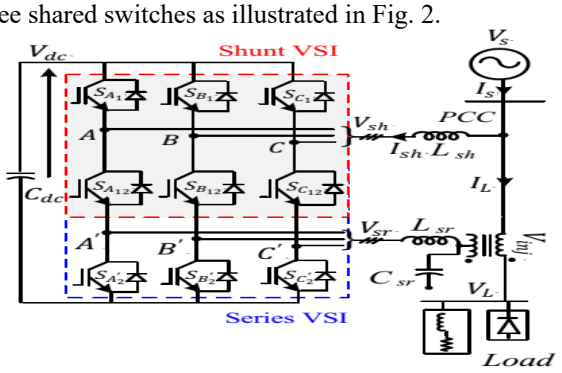

Fig. 2. Nine-switch UPQC topology.

The configuration features saving of three switches and performs satisfactorily under normal and sag conditions without an increase in the dc link voltage. However, it causes considerable rise in the switch current ratings of two switches per phase which is mainly attributed to the series connection of three switches in each leg.

PROPOSED TEN-SWITCH UPQC TOPOLOGY

In this paper, a new topology of UPQC, based on ten switches, is proposed for power quality enhancement applications. As depicted in Fig. 3, the proposed topology is realized by combining the phase C switches of shunt and series VSI { S_{C1}, S_{C2}, } and { $S_{C1}{}^{1} S_{C2}{}^{1}$} in Fig. 1, respectively, into a common leg with a shared set of two switches and . Until now the ten-switch structure has been utilized in drives applications with certain limitations.

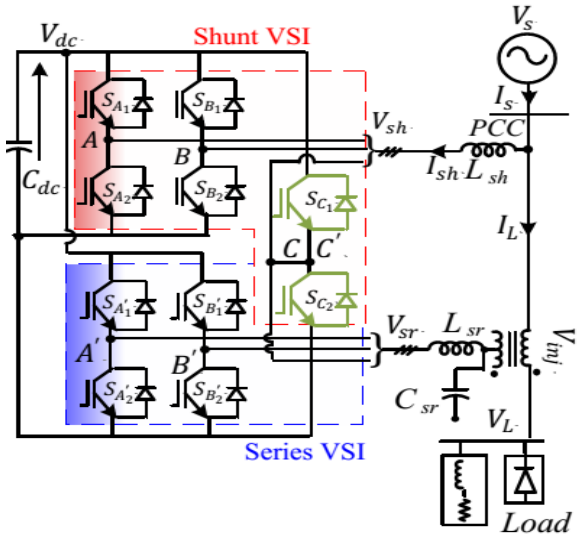

Fig. 3. Proposed ten-switch UPQC topology.

A.Existing constraints and background work related to tenswitch structure

Like most reduced semiconductor topologies, ten-switch structure faces restriction on its allowable switching states for the shared leg (phase C in Fig. 3). Table I and II reflects various switching states for the twelve and ten-switch configurations, respectively. It can be clearly seen from Table II that the output terminals for the shared leg "C" can be connected to either V_{dc} or ground.

TABLE I
SWITCHING STATES FOR PHASE "C" OF SHUNT AND SERIES VSI IN TWELVE-SWITCH CONFIGURATION

Voltage	Switching state
$V_{sh} = V_{sr} = V_{dc}$	$S_{C1}, S_{C}{}^{1}{}_{1} = ON\ S_{C1}, S_{C}{}^{2}{}_{1} = OFF$
$V_{sh} = V_{sr} = 0$	$S_{C2}, S_{C}{}^{1}{}_{2} = ON\ S_{C1}, S_{C}{}^{1}{}_{1} = OFF$
$V_{sh} = V_{dc} = V_{sr} = 0$	$S_{C1}, S_{C}{}^{1}{}_{2} = ON\ S_{C2}, S_{C}{}^{1}{}_{1} = OFF$
$V_{sh} = 0\ and\ V_{sr} = V_{dc}$	$S_{C2}, S_{C}{}^{1}{}_{1} = ON\ S_{C2}, S_{C}{}^{1}{}_{1} = OFF$

TABLE II
SWITCHING STATES FOR PHASE "C" OF SHUNT AND SERIES VSI IN TEN-SWITCH CONFIGURATION

Voltage	Switching state
$V_{sh} = V_{sr} = V_{dc}$	$S_{C1} = ON\ and\ S_{C2} = OFF$
$V_{sh} = V_{sr} = 0$	$S_{C1} = OFF\ and\ S_{C2} = ON$
$V_{sh} = V_{dc} = V_{sr} = 0$	Not Realizable
$V_{sh} = 0\ and\ V_{sr} = V_{dc}$	Not Realizable

Ten-switch configuration was earlier to replace twelve-switch back-to-back converter for dual induction machine drive system. Although the configuration allows independent control of both machines with a wide range of variation in load torque and rotational speeds, it imposes a limitation on the dc link voltage.

$$V_{DC} \geq max(U_{m1} + U_{m2})\ for\ ten - switch\ system$$
$$V_{DC} \geq max(U_{m1}, U_{m2})\ for\ twelve - switch\ system \quad (1)$$

Where V_{dc} is the voltage across the dc link capacitor. In the special case of $U_{m1} = U_{m2} = U$ following constraints can be established.

$$V_{DC} \geq 2U \text{ for ten} - \text{switch system}$$
$$V_{DC} \geq U \text{ for twelve} - \text{switch system} \quad (2)$$

Equation (2) implies that the dc link voltage must be doubled to achieve the maximum rotational speed for both machines simultaneously. Doubling of dc link voltage increases all the component stress by two folds, thus, offsetting the saving of two switches. For the same dc link voltage, the ten-switch structure leads to reduction in the terminal voltage and consequent speed range of both machines.

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Attempts to enhance the dc-bus utilization for the ten-switch architecture. The improvement is obtained at the expense of identical operating (speeding and loading) conditions for both machines. In the controller divides the dc link voltage by allocating predefined switching vectors to each machine.

B.Proposal

This paper proposes the use of ten-switch configuration as the most suitable candidate for shunt-series configuration, such as, UPQC. The rationale behind this recommendation is given below.

As shown in Fig. 3, the outputs of the upper VSI are connected to the PCC constituting the shunt configuration, whereas, the outputs of lower VSI are connected in series with the same PCC constituting the series configuration.

$$m_{res} = m_{sh} + m_{sr} \quad (3)$$

$$V_{sr} = V_L^* - V_{pcc} \quad (4)$$

Where m_{sh}, m_{sr} and are the amplitude of the modulating signal for shunt and series VSIs, respectively. is the resultant modulating signal for the shared set of switches. Fig. 4(a) shows these details within the bandwidth of the dc link voltage in per unit (p.u) where corresponds to $\{V_{dc}, O, -V_{dc}\}$. To maintain the linear range of modulation for and the maximum allowable limit for is -1 to +1. This limit can be further stretched by 15% using third harmonic injection extending the linear range from to as shown in Fig. 4(b) and 4(d). Thus, up to 15% THD in the PCC voltage can be compensated without increasing the dc-link voltage. For higher values of voltage THD, (i.e.> 15%), like all existing configurations, the proposed topology will also require a higher dc-link voltage.

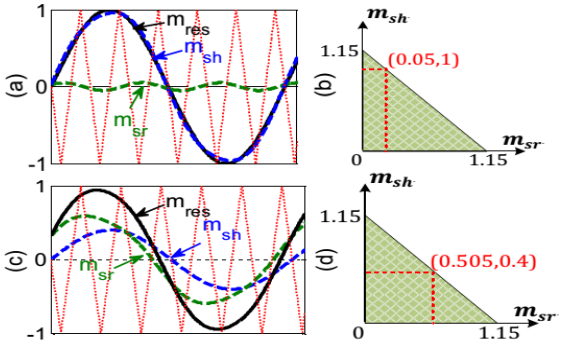

Fig. 4 Modulation references transition for shared leg during normal (upper) and sag (lower) mode of operation in proposed configuration

SWITCH RATING ANALYSIS

From Fig. 1, the per unit current flowing in the series and shunt VSI can be expressed as

$$i_{sr} = \frac{i_L < \theta_{La}}{n_t} = \sum_{h=1}^{\infty} I_L \cos(h_{wL} t + \varphi_{Lh}) = I_L < \theta_L = 1 < \theta_L$$

(5)

$$i_{sh} = \sum_{h=1}^{\infty} I_{sh} \cos(h_{wsh} t + \varphi_{sh-h}) = 1 < \theta_L - 1 \cos\theta_L + I_{1K}$$

(6)

Where h=1, 2, 3 is the harmonic order, i and i are the terminal currents of series and shunt VSIs, respectively. Considering the load current magnitude as the base and angle of the fundamental PCC voltage as the reference angle, transformer turns ratio as unity, the series VSI current i is 1p.u as shown in the first part of (5). The shunt VSI current i consists of fundamental reactive and harmonic portion of load current.

$$I_{1K} = \begin{cases} 0 & if\ k = 0 \\ \left(\frac{1}{1-K}\right) & if\ 0 \le k \le 1 \end{cases} \quad (6)$$

From (6) it is clear that I is a function of the load power factor and sag depth during off nominal conditions. Furthermore, it can be observed from (5) that i and i have different magnitudes and phase angles.

A.Switch rating of back-to-back UPQC

Using the derivations given in [22], the switch current for the back-to-back UPQC of Fig. 1 can be expressed as.

$$i_{SA1} = \sum_{\sigma=1\to f_{sw}} \{2(k_1)(T - T_1) i_{sh}\}\sigma$$

$$i_{SA1^1} = \sum_{\sigma=1\to f_{sw}} \{2(k_2)(T_2) i_{sr}\}\sigma$$

$$k_1 = \begin{cases} 1, i_{sh} \le 0 \\ 0 > 0 \end{cases} \quad k_2 = \begin{cases} 1, i_{sr} \le 0 \\ 0, i_{sr} > 0 \end{cases} \quad (7)$$

Where i_{SA1} andi_{SA1^1} are phase A switch currents of shunt and series VSIs, respectively. is the half switching period of the carrier waveform. is the time interval during which the amplitude of carrier is higher than the modulating signal A amplitude is the time interval during which the amplitude of modulating signal A is higher than the carrier. and are symbolic variables governing the unidirectional current through A and A .

B.Switch rating of nine-switch UPQC

In the nine-switch UPQC topology of Fig. 2, as shown can be expreesed as

$$i_{SA1} = \sum_{\sigma=1\to fsw} \{2(k_1)(T - T_1 - T_2) i_{sh} + (k_3) T_2\}(i_{sh} + i_{sh})\}_\sigma$$

$$i_{SA12} = \sum_{\sigma=1\to fsw} \{2(1 - k_1)(T_1) i_{sh} + (k_2) T_2\}(i_{sr})\}_\sigma$$

$$i_{SA1} = \sum_{\sigma=1\to fsw} \{2(1 - k_2)(T - T_1 - T_2) i_{sr} + (1 - k_3) T_1 (i_{sh} + i_{sr})\}\sigma$$

$$k_1 = \begin{cases} 1, i_{sh} \le 0 \\ 0, > 0 \end{cases} \quad k_2 = \begin{cases} 1, i_{sr} \le 0 \\ 0, i_{sr} > 0 \end{cases}$$

$$k_2 = \begin{cases} 1, i_{sh} + i_{sr} \le 0 \\ 0, i_{sh} + i_{sr} > 0 \end{cases} \quad (8)$$

Based on (8) and the derivation in, the maximum current handled by three upper switches of the shunt VSI

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$\{S_{A1}, S_{B2}, S_{C2}\}$ and three lower switches of the series VSI $\{S^1_{A2}, S^1_{B2}, S^1_{C2}\}$ is (p.u). The current rating of the shared set of switches will be max of (i_{sh}, i_{sr}).

C. **Switch rating of proposed ten-switch UPQC**

The instantaneous current for the shared set of switches and C in the proposed ten-switch UPQC of Fig. 3 can be as shown in fig.

The current rating of the above two shared set of switches will be The remaining four shunt VSI switch currents and four series VSI currents are identical to that of the twelve-switch shunt and series VSIs, respectively. Similar to nine-switch topology, the voltage rating of all the switches is p.u.value.

D. Comparative Analysis

Using the aforementioned expressions for the currents and dc-link voltage requirements, a comparative switch rating analysis is conducted for the three UPQC topologies. Table III provides a summary of the comparison.

TABLE III
PER UNIT COMPONENT RATING OF SEMICONDUCTORS AND OVERALL VA RATING FOR VARIOUS UPQC TOPOLOGIES

UPQC TOPOLOGY	No of switches	Maximum switch voltage rating			Overall UPQC VA Rating
		Dedicated shunt VSI switches	Dedicated series VSI switches	Shared switches	
Tweive –switch	12	$(1< \theta_L - \cos\theta_L) I_{1K}$	$1< \theta_L$	-	VA=6X $X = 2\sqrt{2}((2 < \theta L - \cos\theta L < 0 + I1K$
Nine – switch	9	$(2< \theta_L - \cos\theta_L) I_{1K}$	$(2< \theta_L - \cos\theta_L) I_{1K}$	Max(i_{sh}, i_{sr})	VA=6X+3Y $X = 2\sqrt{2}((2 < \theta L - \cos\theta L < 0 + I1K$ $Y = 2\sqrt{2}(\text{Max}(i_{sh}$
Propose d Ten - switch	10	$(1< \theta_L - \cos\theta_L) I_{1K}$	$1< \theta_L$	Max(i_{sh}, i_{sr})	VA=4X+2Y $X = 2\sqrt{2}((2 < \theta L - \cos\theta L < 0 + I1K$ $Y = 2\sqrt{2}(\text{Max}(i_{sh}$

For a better illustration, an analytical comparison of VA loading for the three UPQC topologies is conducted and given in Table IV. The sag depths of 0.2, 0.4 and 0.6 are considered with a linear inductive load of . It can be seen from Table IV that among all three topologies nine-switch topology requires highest VA loading whereas the proposed topology performs the same tasks with the least VA loading of the UPQC system.

TABLE IV
PER UNIT VA LOADING OF UPQC FOR VARIOUS SAG DEPTHS

SAG DEPTH / UPQC TOPOLOGY	Normal conditions			0.2			0.4			0.6		
	X	Y	total	X	Y	total	X	Y	total	X	Y	total
Twelve-switch ($VA = 6X$)	3.74	-	22.45	6.19	-	37.16	7.12	-	42.75	9.03	-	54.17
Nine-switch UPQC ($VA = 6X + 3Y$)	3.74	2.8	30.9	6.19	5.68	54.1	7.12	6.68	62.76	9.03	8.69	80.23
Proposed Ten-switch ($VA = 4X + 2Y$)	3.74	2.8	20.62	6.19	5.68	36.2	7.12	6.68	41.84	9.03	8.69	53.48

MODULATION SCHEME FOR TEN-SWITCH UPQC

Fig. 5 shows the developed modulation scheme to generate gate pulses for the proposed ten-switch UPQC topology. It involves dual stage zero sequence injection in the modulating references. The inputs to the modulator block are three reference signals each from the shunt and series VSI control blocks (further explained in section VI).

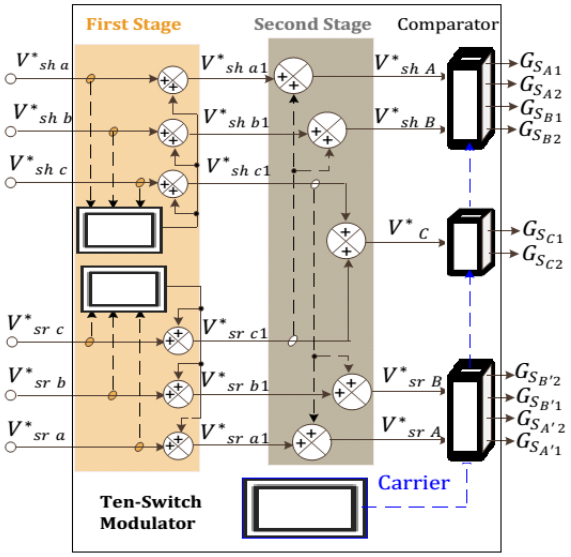

Fig. 5. Modulation scheme for the proposed ten-switch UPQC system

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The developed modulation technique has two stages that are explained below. In the first stage, to enhance the dc bus utilization, the third harmonic injection is carried out. Let, V and V be the reference signals determined by the shunt and series VSI control blocks, respectively.

$$V_{no-sh} = -0.5.\left[Max\left(V^*_{Sha,b,c}\right) + MinVsh\ a,b,c*\right] \quad (9)$$

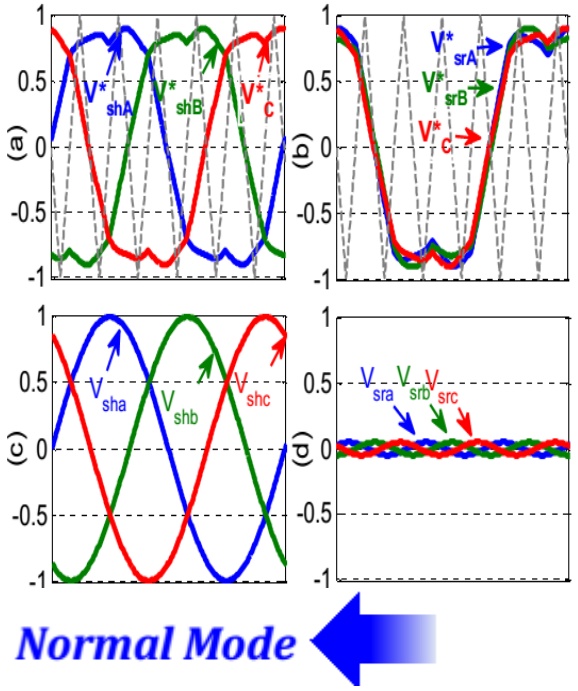
$$V_{no-sh} = -0.5.\left[Max\left(V^*_{Sra,b,c}\right) + Min\left(V^*_{sr\ a,b,c}\right)\right] \quad (10)$$

where

$$V^*_{sh-i1} = V^*_{sh-i} + V_{no-sr} \quad (11)$$

$$V^*_{sr-i1} = V^*_{sr-i} + V_{no-sr} \quad (12)$$

In the second stage, five modulating signals for each leg, from the six aforementioned references, are generated. The series VSI reference for the shared phase "C" is added to the three modified shunt VSI references of Similarly, the shunt VSI reference for the shared phase "C" is added to the three modified series VSI references of in this case, the shunt VSI requires the maximum dc-link voltage for load reactive power compensation. This infers that the peak magnitudes of the shunt reference modulation indices would be very close to unity which is given in Fig. 6(a).



The corresponding output voltages at the shunt VSI terminal are shown in Fig. 6(c). Nevertheless the effective contribution of these reference signals towards the injected voltage will correspond to only a small voltage as shown in Fig. 6(d) consisting of the voltage required to compensate the harmonics in the PCC voltage. This is due to the fact that the added zero sequence signals effectively cancel out in the injected line-line voltages.

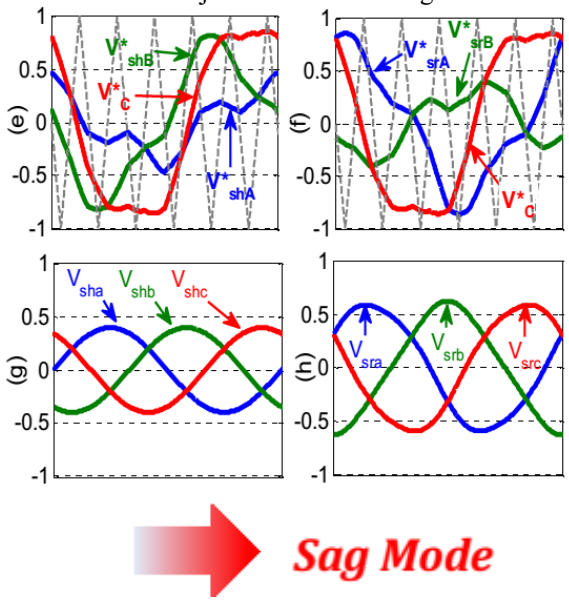


Fig. 6 Representation of modulation indexes and output voltages after second stage for (a),(c) shunt VSI during normal mode (b),(d) series VSI during normal mode (e),(g) shunt VSI during sag mode and (f),(h) series VSI during sag mode.

When there is a drop in the PCC voltage, the peak amplitude of the voltage at shunt VSI terminals decreases as shown in Fig. 6(g). To compensate the sag, the output voltage amplitude of the series VSI increases. Figs. 6(f) and (h) reflect the transition in series VSI reference and output voltage during sag condition.

CONTROL SCHEME FOR THE PROPOSED TEN-SWITCH UPQC

A.Control for Shunt-VSI

The task of the shunt VSI is to compensate the reactive and harmonic components of load current and regulate the dc link voltage during normal and sag conditions. To realize these objectives, the control scheme is shown in Fig. 7. The measured load current i is converted to the synchronous reference frame quantitates i and i which are given as.

$$i_{Ld} = \bar{I}_{Ld} + \tilde{I}_{Ld}$$
$$i_{Lq} = \bar{I}_{Lq} + \tilde{I}_{Lq} \quad (13)$$

where i_{Ld} and i_{Lq} correspond to the fundamental active and reactive components of load current, respectively. and

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reflect the harmonic components of i . The reference current of the shunt VSI can be expressed as

$$i_{ref-sh} = \widetilde{i_{Ld}} + i_{Lq} + i_{Loss} \quad (14)$$

Where i_{Ld} is obtained by passing i_{Ld} through a high-pass filter. i_{Loss} corresponds to the active component of the source current required to maintain the dc link voltage at rated value.

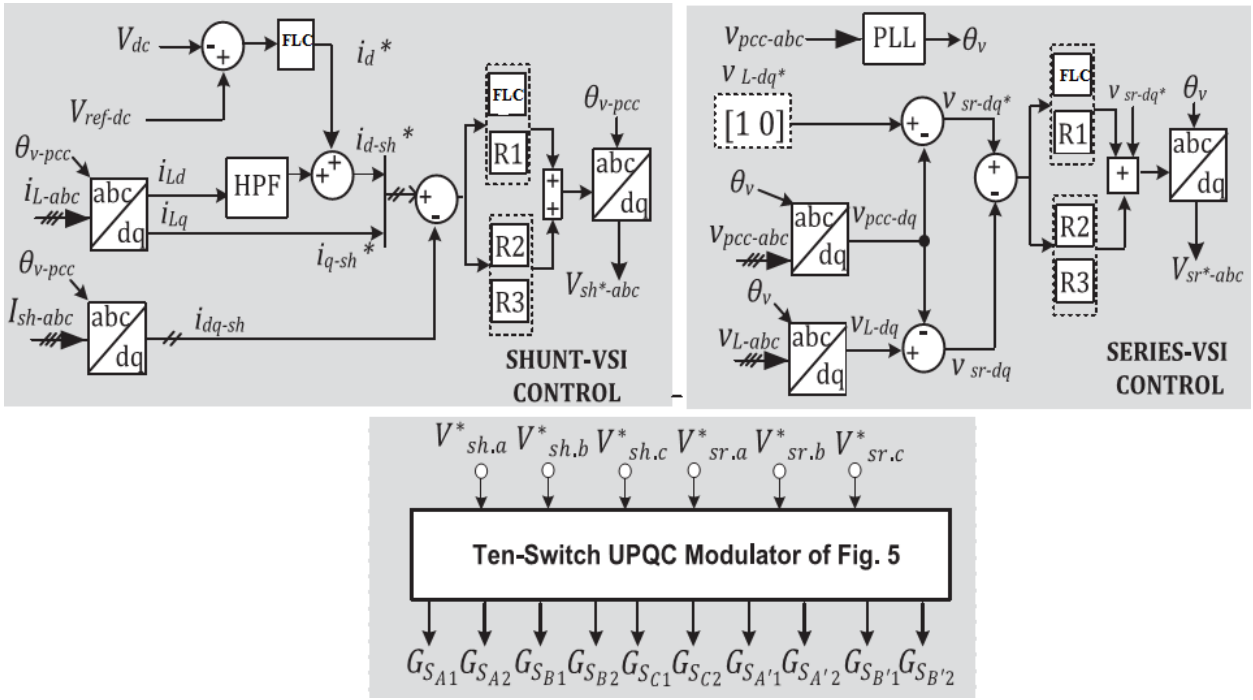

Fig. 7. Detailed control block diagram for the proposed ten-switch UPQC

B.Control for Series-VSI

The objective of the series VSI is to maintain the rated sinusoidal voltage at load terminals regardless of the voltage variation at the PCC. The overall series VSI control block is shown in Fig. 7.

The difference between the series VSI reference voltage $V\ V\ V$ and actual voltage $V\ V\ V$ is processed by a combination of fuzzy and resonant controllers in the synchronous reference frame. For sag detection the absolute error between PCC reference voltage (1 p.u.) and the actual PCC voltage magnitude (p.u.) in the synchronous reference frame is calculated as follows.

$$i_{ref-sh} = \tilde{I}_{Ld} + i_{Lq} + i_{Loss} \quad (15)$$

$$V_{error} = \left|1 - \sqrt{V_{pcc-d}^2 - V_{Pcc-q}^2}\right| \quad (16)$$

The controller continuously monitors V and as soon as it exceeds the threshold of zero p.u., sag is detected. Although $V_{Sr}^* - vsi - dq$can be directly used to control the series VSI in open loop by converting it into the stationary reference frame however it will not be able to compensate the drop across VSI switches, interfacing filter and series transformer. It is therefore added as a feed forward signal to the output o fuzzy to compensate for system losses. The resulting signal is converted into the stationary frame giving V which is the reference modulating signal for series VSI.

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

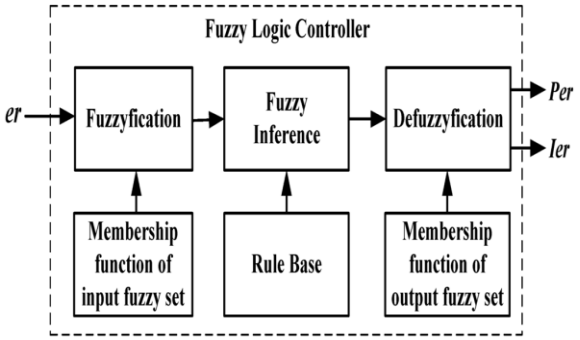

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Fig.8.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method

TABLE V: Fuzzy Rules

e / ė	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system.

The value of input error and change in error are normalized by an input scaling factor.In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (17)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (18)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter.

In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (19)$$

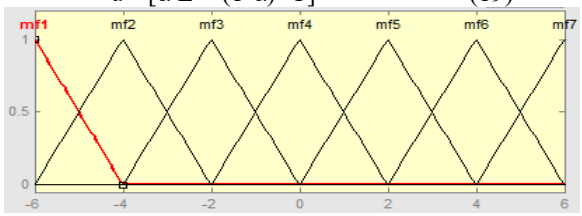


Fig 8 input error as membership functions

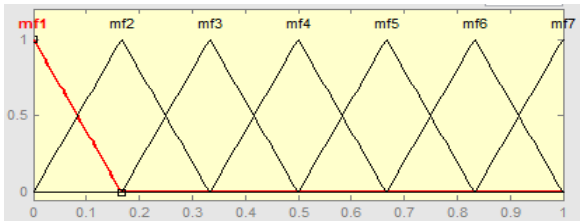


Fig 10 change as error membership functions

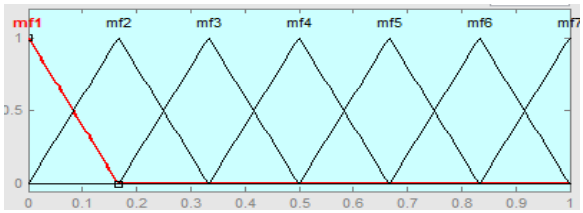
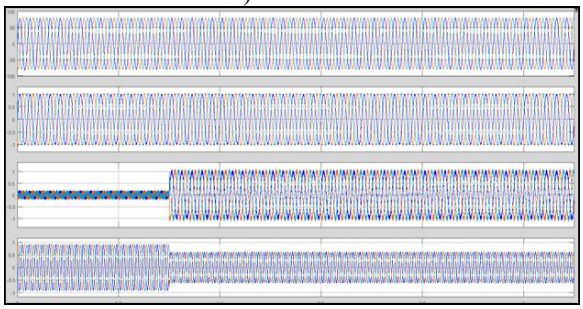


Fig.11 output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

SIMULATION RESULTS

To emulate the sag and harmonic distortion in the grid voltage, a three phase programmable source is used. Note that in all the simulation results the PCC and load voltages are shown as line to line voltages, whereas, the series injected voltages are shown as phase voltages across series transformer).



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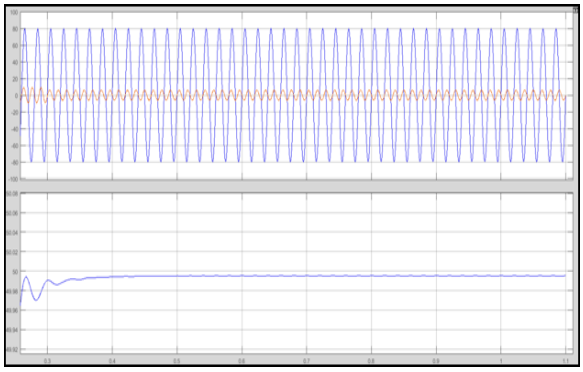

Fig. 12. Simulation result: power factor correction during steady state condition

Fig. 12 depicts the steady state performance of the proposed ten-switch UPQC system considering a linear RL load.Initially, the shunt VSI is maintaining the dc-link voltage by drawing a small current (Fig. 12(c)), whereas, the load reactive power is supplied by the grid. As seen from Fig 12(e), the grid current lags the grid voltage by . The reactive compensation starts at time . The shunt VSI injects the necessary current causing the grid to supply only the load active power (i.e. grid current being inphase with the grid voltage as shown in Fig. 12(e)).

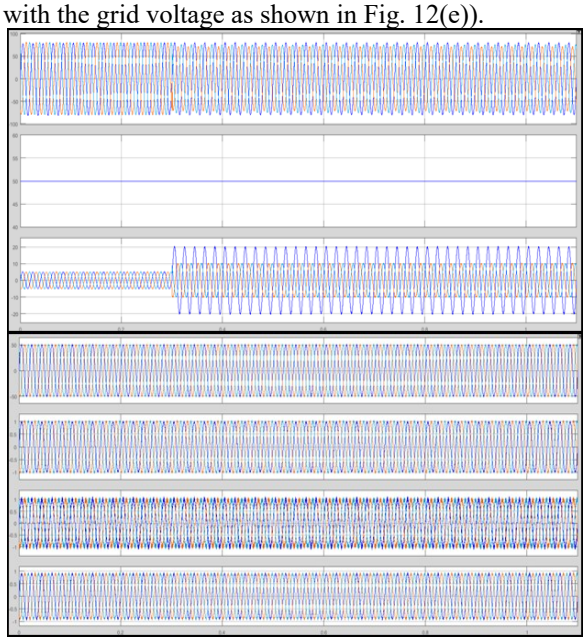

Fig.13. simulation result: transition from steady state to unbalanced voltage sag condition (with liner RL load)

A sudden sag condition is occurred in the proposed method, An unbalance voltage sag is introduced in the grid voltage as shown in Fig. 13(a). It can be seen from Fig. 13 that the proposed ten-switch UPQC effectively maintains the dc link as well as the load voltage at nominal values (Figs. 13(b) and (c)). As shown in Fig. 14 (c), the load voltage are maintained at rated value in this case as well.

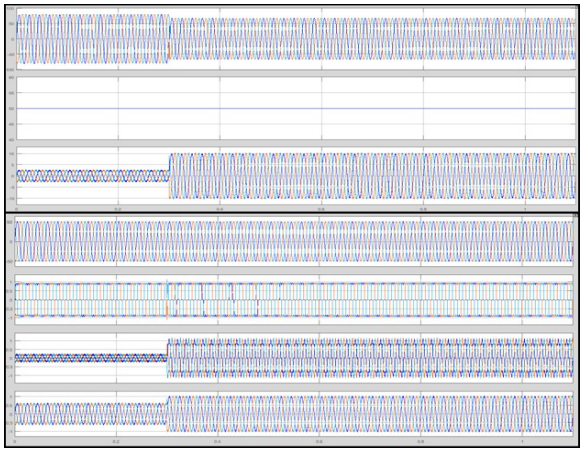

Fig.14. simulation result: transition from steady state to balanced voltage sag condition (with non-linear load).

Fig. 15 depicts the performance of proposed ten-switch UPQC when the PCC voltage and load current are distorted. A combination of linear (RL) and nonlinear load is considered with the combined load current THD of 18%. The 5 th and 7th harmonic voltages are added in the grid voltage to achieve a THD of 10%.

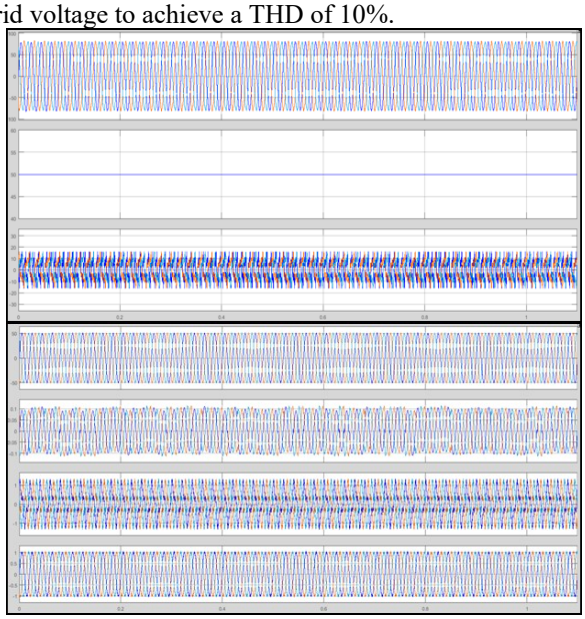

Fig. 15. simulation result: distorted supply and unbalanced nonlinear load condition.

The series part effectively mitigates the harmonics in the grid voltage. The improved load voltage profile can be noticed from Fig. 15(d) wherein the THD is reduced to 3%. Simultaneously, the shunt controller effectively compensates the load current harmonics achieving sinusoidal grid currents with the THD of 2.1%. Thus, the above experimental study verifies the feasibility of the proposed ten-switch UPQC topology Wapplications to improve the power quality.

CONCLUSION

A novel proposes this paper for eliminating of the drawbacks of the nine switch based reduced switch power conditioner with fuzzy logic controller using UPQC ten switch topology. For this fuzzy controlled based UPQC has to maintain power quality enhancement with limited switches and without increasing the switch VA rating for avoiding the losses of devices. The simulation results of this paper compare with the nine switch topology the proposed paper achieve the same power quality with the least VA loading of the UPQC system. The performance of the proposed topology has been validated with simulation results under various operating conditions.

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