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An Innovative of Dynamic Voltage Renovator for Consideration of Voltage Sag by Induction Motor

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ABSTRACT

The increment of voltage sensitive load equipment has made the industrial process must more susceptible to degradation in the power quality. Voltage deviation, often on the form of voltage sag, can cause severe process, result in economical loss. Among the Custom Power Device (CPD), the application of Dynamic Voltage Restorers (DVRs) in the distribution system is the recent invention. DVR's are used to protect sensitive loads from the effects of voltage sags on the distribution feeder. DVR normally installed between the source voltage and critical or sensitive load. The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by the following: 1) reducing the amplitude of the injected voltage or 2) optimizing the dc bus energy support. In this paper, an enhanced sag compensation strategy is proposed, which mitigates the phase jump in the load voltage while improving the overall sag compensation time. simulations are performed using Matlab/Simulink's SimPowersystem Toolbox.

Index Terms: *Power Quality, Voltage Sag, Dynamic voltage restorer (DVR), voltage source inverter (VSI).*

I.INTRODUCTION

In industrial distribution systems, the grid voltage disturbances (voltage sags, swells, flicker, and harmonics) are the most common power quality problems. Sag, being the most frequent voltage disturbance, is typically caused by a fault at the remote bus and is always accompanied by a phase angle jump. The phase jump in the voltage can initiate transient current in the capacitors, transformers, and motors [2]. It can also disturb the operation of commutated converters and may lead to glitch in the performance of thyristor-based loads [3]. It is therefore imperative to protect sensitive loads, especially from the voltage sags with phase jump [4]. To protect sensitive loads from grid voltage sags, custom power devices (such as SVC, D-STATCOM, dynamic voltage restorer (DVR), and UPQC) are being widely used.The system configuration of a DVR is shown in Fig. 1. It consists of a dc link capacitor (serving as an energy reserve for DVR), a series injection transformer, a six-switch voltage source inverter (VSI), and an LC filter for removing switching harmonics from the injected voltage.

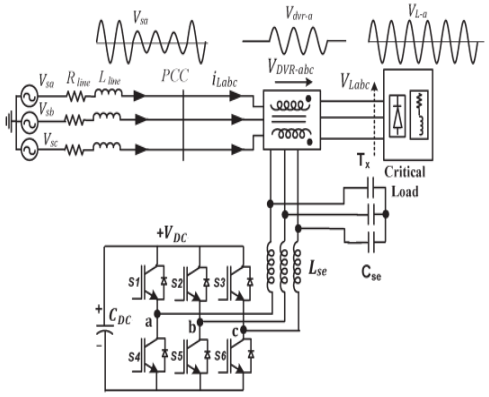

Fig.1. Basic DVR-based system configuration

The primary function of the DVR is to inject a voltage with certain magnitude and phase in series with the upstream source voltage such that the load connected downstream always sees the pure sinusoidal voltage at its terminals. Numerous control strategies for DVR have been reported in the literature.

However, the phase jump compensation using the pre-sag method requires a significant amount of

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active power from the dc link capacitor. Thus, this method will require a larger size capacitor or will result in shorter sag support time. An interesting technique is proposed to increase the compensation time while mitigating the voltage phase jump. In this method, once the dc link voltage drops to the threshold limit, the magnitude of the injected voltage is reduced by synchronizing the phase-locked loop (PLL) to the grid voltage. This allows further utilization of the dc link capacitor energy and extends the compensation time by some extent. However, it continues to consume the energy in the dc link capacitor throughout the duration of compensation and imposes limitation on compensation time enhancement. This paper proposes a new control strategy in which the main objective is to enhance the sag compensation time while mitigating the voltage phase jump. The proposed method aims at regulating the contribution of active power to the least possible value.

II. DVR OPERATION

In this section, different sag compensation approaches [12]–[15] are briefly discussed. The phasor representations of these methods are given in Fig. 2. The phasors $\vec{V}_G$ and $\vec{V}_G'$represent the rated and sagged grid voltages, respectively, whereas $\vec{V}_L$ and $\vec{V}_L'$ are the load voltages before and after the sag. To effectively highlight the differences among these methods, P_{DVR} and Q_{DVR} are also incorporated in the phasor diagrams. This is mainly to illustrate the amount of active and reactive powers demanded by each method. All of the quantities are drawn considering the load current ($\vec{I}_L$) as reference phasor.

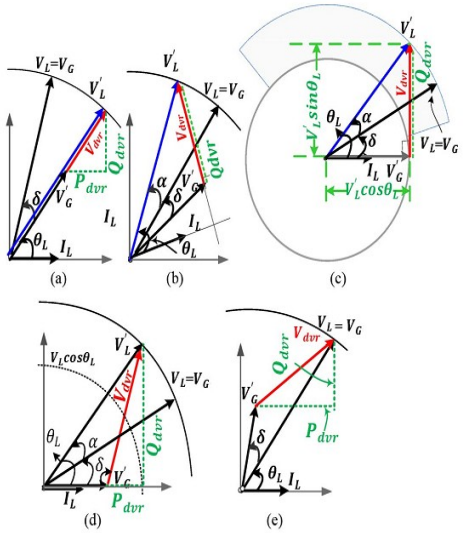

Fig. 2. Per-phase phasor representation of the basic compensation topologies for DVR. (a) In-phase injection. (b) Quadrature injection. (c) Quadrature injection limiting case. (d) Energy-optimized injection. (e) Pre-sag injection.

A. In-Phase Compensation

In this type of compensation, DVR injects the smallest possible voltage magnitude in phase with the sagged grid voltage. However, as seen from Fig. 2(a), this method cannot correct the phase jump. The DVR-injected voltage magnitude and angle are given as

$$V_{DVR} = \sqrt{2}(V_L - V_G') \quad (1)$$

$$\angle V_{DVR} = \theta_L. \quad (2)$$

B. Quadrature Injection (Reactive Compensation)

In this method, the DVR injects voltage in quadrature with the load current, i.e., it corrects the sag with only reactive power. Using Fig., the injected voltage magnitude and angle are given as

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$$V_{DVR} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\alpha + \delta)} \quad (3)$$

$$\angle V_{DVR} = \frac{\pi}{2} \quad (4)$$

Where δ is the phase jump in the grid voltage due to the sag and α is the phase jump induced due to reactive power compensation. As reported in [12], the maximum sag depth ($\Delta V_{sag,max}$) that can be compensated using quadrature injection is closely related with the load power factor and can be expressed as

$$\Delta V_{sag-max} \leq (1 - \cos\theta_L). \quad (5)$$

The corresponding maximum injected voltage is given as

$$V_{DVR-max} = \frac{V_G'}{1 - \Delta V_{sag,max}} \sin\theta_L. \quad (6)$$

Fig. 2(c) shows the limiting case for quadrature injection where DVR supports the full load reactive power whiles the grid operates at unity power factor.

C. Energy-Optimized Injection

This method is developed in [15] to enhance the performance of the quadrature injection method for the sag depth deeper than the limit in (5), where the DVR injects certain active power. The DVR voltage magnitude and injection angle can be calculated from Fig. 2(d)

$$V_{DVR} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\theta_L)} \quad (7)$$

$$\angle V_{DVR} = \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_G'}\right). \quad (8)$$

D. Pre-sag Compensation

In this method, both load voltage magnitude and phase are restored to pre-sag values. Unlike the previous methods in Fig. 2(a), (b), and (d), the pre-sag method in Fig. 2(e) can successfully compensate the phase jump. Using Fig. 2(e), the injected voltage magnitude and angle can be written as

$$V_{DVR} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\delta)} \quad (9)$$

$$\angle V_{DVR} = \tan^{-1}\left(\frac{V_L \sin\theta_L - V_G' \sin(\theta_L - \delta)}{V_L \cos\theta_L - V_G' \cos(\theta_L - \delta)}\right). \quad (10)$$

III.ANALYSIS OF POWER FLOW AND MAXIMUM COMPENSATION TIME

As explained earlier, the pre-sag method is the most energy intensive method, and the injected power can be quite high even for shallow sag depths. Based on the phasor diagram of Fig. 2(e)[(9) and (10)], the active power associated with the pre-sag method can be expressed in terms of sag depth, phase jump, and load power factor as given in the following:

$$P_{presag} = \sqrt{3}V_L I_L(\cos(\theta_L) - (1 - \Delta V_{sag})\cos(\theta_L - \delta). \quad (11)$$

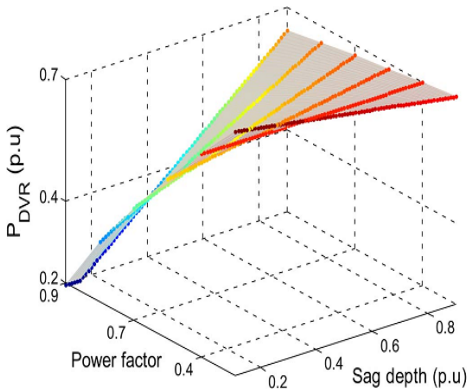

Fig.3. Active power associated with the pre-sag compensation method for different sag depths (phase jump=25◦).

A detailed derivation of (11) is given in Appendix A. Fig. 3 shows the DVR active power for a range of variation in sag depth (0.1≤ΔVsag ≤0.9)and power factor(0.4≤cosθL≤0.9). The phase jump δ is fixed

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at+25◦. As seen from the graph of Fig. 3, the active power supplied by DVR is relatively high (>0.4 p.u.) for the pre-sag method. The theoretical power flow analysis conducted previously holds true as long as there is a significant amount of energy in the dc link capacitor. The following relationship should be satisfied at all time in order to achieve the adequate operation of DVR-VSI :

$$\frac{V_{dvr}}{n_t} \leq \frac{m_{i-max} V_{dc}}{2} \qquad (12)$$

Where n_t is the turns ratio of the series transformer and m_{i-max} is the maximum modulation index of VSI. V_{dvr} is the injected phase to neutral voltage. V_{dc} is the dc link voltage. As soon as the dc link voltage decreases below V_{dc-min}, i.e., the limit set by (12), the DVR controller must stop the compensation process to avoid harmonics contamination in the load voltage.

The energy stored in the dc link capacitor is equal to

$$E_{c-dc} = \frac{1}{2} C_{dc} V_{dc}^2. \qquad (13)$$

The power flow out of the dc link capacitor in the steady state is given as

$$P_{c-dc} = \frac{1}{2} C_{dc} \frac{d}{dt} V_{dc}^2. \qquad (14)$$

Considering a lossless DVR system, the dc power can be equated with the ac power to find the capacitor size. This limitation restrains the DVR operation even though there is sufficient amount of stored energy in the dc link capacitor as shown in Fig. 4. Furthermore, the gradient of the dc link voltage d_{vdc}/d_t is directly proportional to the DVR-injected active power, i.e., P_{dvr}. The lower the value of P_{dvr}, the smaller is the slope of the dc link voltage and the higher will be the time for which $V_{dvr}/n_t \leq (m_{i-maxVdc})/2$. This leads to the following two hypotheses.

1) The energy stored in the dc link capacitor can further be utilized.

2) The rate of change (fall) of the dc link voltage can further be optimized.

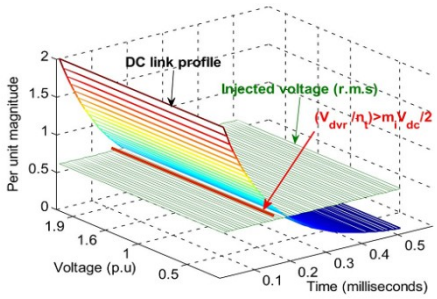

Fig.4. DC link capacitor voltage profile during pre-sag injection.

IV.PROPOSED COMPENSATION SCHEME

A. Phase Jump Detection and Pre-sag Restoration

For detecting the phase jump, two PLLs are employed (one over the load voltage and another over the source voltage), giving θVL and θVg, respectively. As soon as the sag is detected, the first step is to determine the DVR initial injection angle that avoids the phase jump at the load side. This is done by freezing the load voltage PLL that gives the pre-sag angle (θVLp).On the other hand, the unrestricted grid voltage PLL gives the grid voltage phase (θVg). The difference between these two angles gives the initial angle of injection

$$\left.\begin{aligned} \theta_{init} &= \theta_L + (\theta_{VLp} - \theta_{Vg}) \\ &= \theta_L + \delta \end{aligned}\right\}. \qquad (16)$$

Note that, in the steady state, both angles will be identical, and thus, the difference will be zero. For sag detection, the absolute difference between the reference load voltage (1 p.u.) and the actual grid voltage (p.u.) in synchronous reference frame is calculated as follows

$$\Delta V_{sag} = \left| 1 - \sqrt{V_{gd}^2 + V_{gq}^2} \right|. \qquad (17)$$

As soon as ΔVsag >0.1, it is recognized as a voltage sag.

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B. Controlled Transition toward the MAP Mode

Once the pre-sag voltage is successfully restored, after one cycle, a smooth transition toward the MAP mode is initiated and completed over the next one to two cycles. The final injection angle of DVR (θfin)is given as

$$\theta_{\text{fin}} = \begin{cases} \frac{\pi}{2}+\gamma, & \text{if } \Delta V_{\text{sag}} \le (1-\cos\theta_L) \\ \pi - \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_g'}\right), & \text{if } \Delta V_{\text{sag}} > (1-\cos\theta_L) \end{cases} \quad (18)$$

A detailed derivation of (18) is given in Appendix C. The first part of (18) represents the self-supporting mode of operation in which the DVR absorbs active power (relatively very small amount) from the grid to overcome the system losses and thus maintains a constant voltage across the dc link capacitor. To ensure a smooth changeover, a transition ramp is defined between the initial and final operating points, as given in the following:

$$\theta_{\text{trans}} = \theta_{\text{init}} + \frac{\theta_{\text{fin}} - \theta_{\text{init}}}{\Delta T}(t) \quad (19)$$

Where ΔT determines the slope of the transition curve and is chosen as 30 ms.

C. Iterative Decrement in Injection Angle

In self-supporting mode, the DVR can compensate the sag for an indefinitely long time. However, for deeper sag depths, there is certain nonzero active power injected by DVR. This causes a reduction in the energy stored in the dc link capacitor, and consequently, its voltage reduces (gradually). To avoid this over modulation condition, an iterative control loop is used, which constantly monitors the dc link voltage and decreases θfin in (18) to keep Vdc>Vdc−min and is given as

$$\theta_{\text{fin}} = \theta_{\text{fin}} - \epsilon \quad (20)$$

Where €is chosen as 0.01 rad.

D. Operation Sequence

Fig.depicts the overall operation sequence of the proposed phase jump compensation scheme. The transition from high active power mode (pre-sag) to MAP mode is shown in three steps. The illustration is for the case where the sag depth is more than the limit in (5) and there is a positive phase jump associated with the sag. As discussed previously and shown in Fig. 5(a), DVR initiates the compensation by supplying high active power to the load (Vr1≫Vx1) and restores both magnitude and phase of the load voltage to pre-sag values.

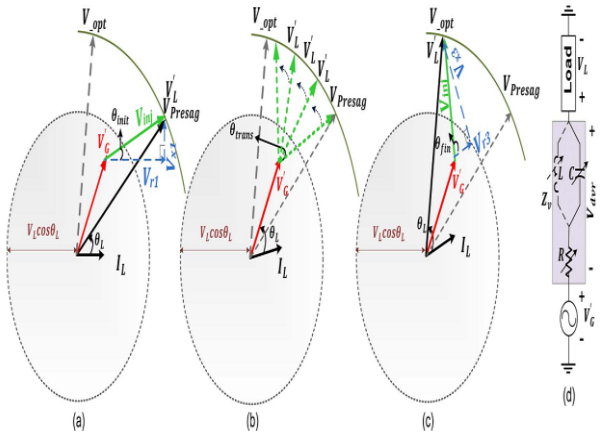

Fig. 5. Phasor diagram for the proposed sag compensation method. (a) Pre-sag restoration, (b) intermediate transition, (c) final load voltage with MAP injection, and (d) DVR visualization as the variable virtual impedance changes from resistive to dominant capacitive (for sag) or inductive (for swell).

After one cycle, the transition toward the MAP mode is initiated, and DVR gradually increases the contribution of reactive power. As seen from Fig. 5(b) and (c), the injected voltage magnitude and its phase angle are gradually increasing until V_L' reaches V_{L-opt}. Note that at the final operating point Vr1≪Vx1. The aforementioned DVR operation can be viewed as an equivalent variable impedance Zv where the operation begins with dominant resistive impedance Zv=R (high active power) and completes as dominant capacitive impedance Zv≈XC (high reactive power).

V.ANALYTICAL STUDY ON COMPENSATION TIME WITH DIFFERENT APPROACHES

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In this section, a comparative study is presented to determine the maximum compensation time achieved using the aforementioned phase jump compensation methods. These include the following: 1) the pre-sag; 2) the method given in [16], named as pre-sag–in-phase in this paper; and 3) the proposed method. Table I shows the various design parameters used for the comparison. Analytically computed DVR-injected magnitude and maximum compensation times are provided in Fig.

TABLE I
DVR SYSTEM PARAMETERS (BOUNDARY CONDITIONS)

Parameter	Value
Grid voltage (L-L) (rms) V_{base}	415 V
Line frequency	50 Hz
Nominal Power (Base kVA)	10 kVA
Nominal Load power factor	0.7 Lagging
Maximum compensation time	10 cycles
Maximum sag depth	0.5 p.u
Maximum phase jump	$\pm 45^0$
Maximum injected voltage	0.7 p.u
Transformer turns ratio	1:1
DC link Capacitance value	9000 μF

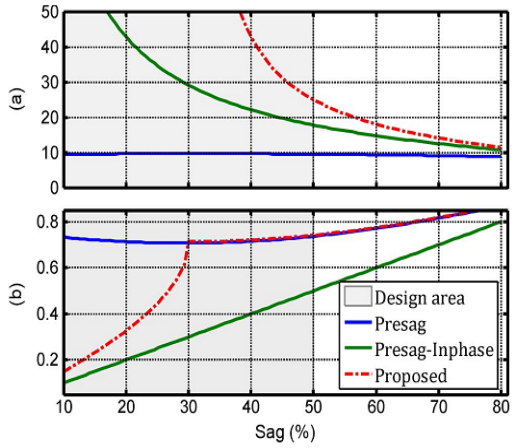

Fig. 6. Maximum compensation time and DVR-injected voltage for various sag depths with different methods. (a) Compensation time cycles. (b)V_{DVR} p.u.

Note that the DVR voltage magnitudes are shown after the first one cycle of compensation as all of the three methods perform identically for the first cycle. As seen from Fig. both the pre-sage and proposed methods have the same V_{DVR} magnitude for a sag depth greater than the limit in (6), i.e., 30%. However, as noticed from Fig. tc−maxis highest for the proposed method for all values of sag depths.

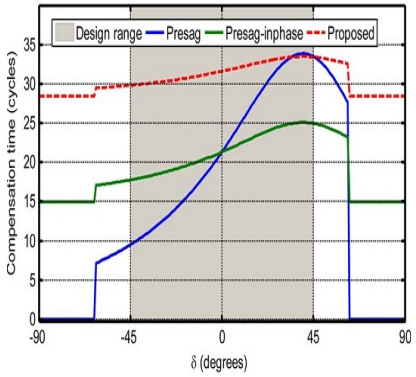

Fig.7. Maximum compensation time for a range of variation in phase jump

Fig. 7depicts the scenario where the phases jump is varied from −90◦ to +90◦ for a sag depth of 0.5 p.u.

VI.OVERALL DVR SYSTEM CONTROL SCHEME

Fig. 8depicts the detailed block diagram of the proposed phase jump compensation method. A logic unit is employed to constantly monitor the grid voltage for sag detection using (17). To obtain the reference load voltage, the control system is divided into two sub modules: 1) phase jump detection plus DVR injection angle calculation and (2) MAP injection.

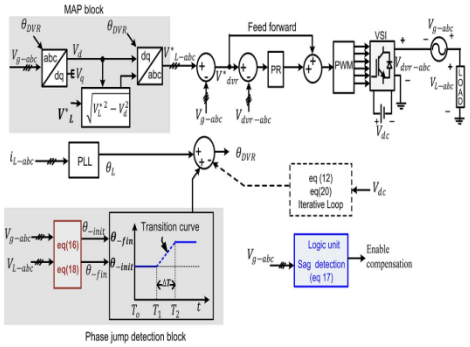

Fig.8. Detailed block diagram of the proposed phase jump compensation method with MAP injection

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VII.SIMULATION RESULTS

A simulation model for the DVR system, with the parameter given in Table I, is developed and simulated for the performance evaluation. The dc link capacitor of 9000μF, as computed in the previous section, is used for this study.

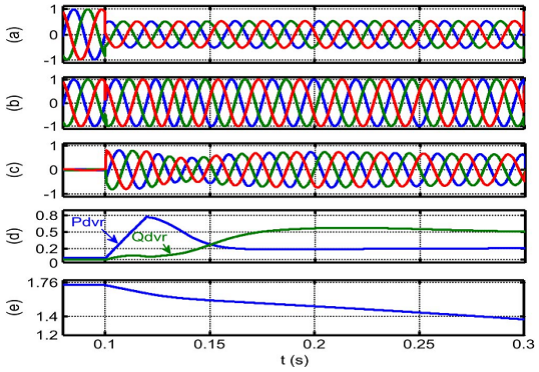

Fig. 9. Simulation results for the proposed sag compensation method for 50%sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage. (d) DVR active and reactive power. (e) DC link voltage.

The simulation results for two different scenarios are given in Figs.In the first scenario, a sag depth of 50% [higher than the limit in (5)] is considered with a phase jump of+25◦.

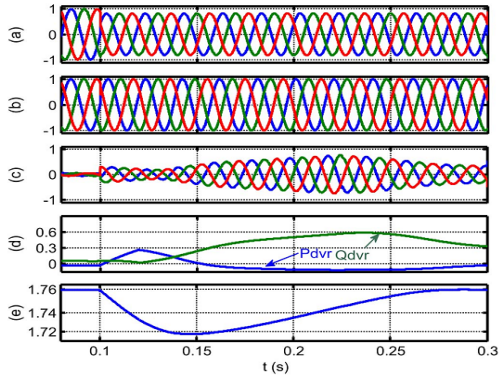

Fig.10. Simulation results for the proposed sag compensation method for 23% sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage. (d) DVR active and reactive power. (e) DC link voltage.

In the second scenario, a sag depth of 23% [lower than the limit given in (5)] is considered with a phase jump of +25◦. As seen from the results in Fig.

TABLE II
DVR SYSTEM DATA FOR THE EXPERIMENTAL STUDY

Source Chroma 61703	Supply voltage: 50 V-rms, 50 Hz Source Impedance: R_g = 0.047 Ω and L_g = 160 μH
DVR	DC link capacitors, C_{dc} = 1100 μF Reference DC link voltage = 55 V Filter inductor, L_f = 5 mH C_f =50 μF Transformer turns ratio 1:1
Load	R = 11 Ω and L = 80 mH Nominal Load voltage = 50 V Rating = 250 W
Compensation time	10 cycles (200 ms)

CONCLUSION

In this paper, an enhanced sag compensation scheme has been proposed for the capacitor-supported DVR. The proposed strategy improves the voltage quality of sensitive loads by protecting them against the grid voltage sags involving the phase jump. It also increases compensation time by operating in MAP mode through a controlled transition once the phase jump is compensated. To illustrate the effectiveness of the proposed method, an analytical comparison has been carried out with the existing phase jump compensation schemes. It is shown that the compensation time can be extended from 10 to 25 cycles (considering pre-sag injection as the reference method) for the designed limit of 50% sag depth with 45◦ phase jump. Further extension in compensation time can be achieved for intermediate sag depths. This extended compensation time can be seen as a considerable reduction in dc link capacitor size (for the studied case more than 50%) for the new installation. The effectiveness of the proposed method has been evaluated through extensive simulations in MATLAB/Simulink and validated on a scaled laboratory prototype experimentally.

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