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High Performance Multiple Constant Multiplier Using Modified Booth Algorithm

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ABSTRACT: *Over the many years, various techniques have been developed for the efficient realization of constant multiplications by a network of add/subtract-shift operations. Radix-2^r arithmetic is applied to the multiple constant multiplication (MCM) as nonnegative constants which are denoted by M with a bit length N. Multiple constant Multiplication can detect the analytic formulas for the maximum number of additions, and the maximum number of cascaded additions, the average number of additions forming the critical path. A high performance 32*32 bit modified booth multiplier has been designed in the proposed system. Therefore, modified booth encoding(MBE) permits carry-free addition and adaptability. It has been used in 32*32 bit high-performance modified booth multiplier design for summation of partial product terms. The modified Booth multiplier also reduces redundant partial product accumulation stage when eliminating the error correcting word(ECW) which improves the complexity and the critical path delay.*

KEY TERMS: Multiple constant multiplication (MCM), Modified booth encoding(MBE), Error correcting word(ECW)

I.INTRODUCTION

Multiplier influenced applications like computer applications, wireless communications, and digital signal processing, conventional high speed multiplier are no longer capable of producing the high speed computational needs at low power requirements of the portable devices. Thus to accelerate the overall performance of the systems, designing high performance multipliers has always been one of the main objectives for system designers.

The multiplication process has been achieved more efficiently by numerous high performance algorithms and architectures. Generally, multiplication of two operands can be done in three steps. In the initial step partial product terms are generated. In the next step pair wise summation of partial product rows is performed till only two partial product rows are remain. In the third step the two remaining rows are added up by fast carry-propagate adder for generating the final product. In the Initial step, Radix-4 Modified Booth Encoding (MBE) is utilized to great extent for reduction of the total number of partial product rows to half.

Partial product reduction schemes like compressor trees or Wallace trees are involved for fast summation of partial product rows in the second step. In the third step, from partial product summing tree the two rows are added by fast carry-look ahead or carry select adders to acquire the final multiplication product. To obtain an efficient multiplier, numerous approaches have been proposed in the past years to develop the above three steps. Modified Booth encoding scheme reduces the total partial product terms to half and thus asset the multiplier design by reducing the size and enhancing the speed of the summing tree. The advance predominant multiplier design employs compressors in partial product summing tree for high-speed parallel computation.

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This method is useful in eliminating the intermediate carry propagation, but still there is a possibility of carry propagation from the least significant bit (LSB) position to the most significant bit (MSB) position in the final addition stage, which needs a speedy, complicated, and high power adder.

II.EXISTED SYSTEM

The multiple-constant multiplication (MCM) problem is to determine a shift-and add network that can realize multiplication of a single input x(n) with a set of coefficients, Here It is sufficient to only consider odd integer coefficients, since even and fractional coefficients can be obtained by an appropriate shift operation. The sign of the coefficient can also in most cases be compensated for in other parts of the implementation. Hence, the coefficient set, C, which is the input to the MCM algorithm, as illustrated in Fig. 1, is assumed to only contain unique positive odd integers. The shift- and-add networks are often illustrated using the directed acyclic graph representation of multiplication introduced.
Each node, except for the input node, corresponds to an addition/subtraction and each edge corresponds to a shift operation, i.e., a multiplication by a power-of-two. The nodes are assigned values, which are referred to as fundamentals.

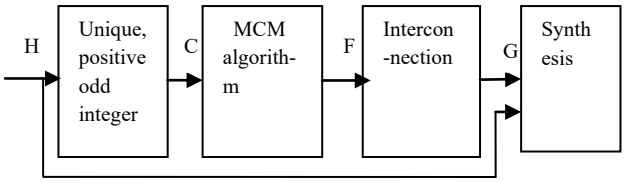

FIG 1. EXISTED SYSTEM

We propose hereafter a new MCM algorithm, called RADIX-2r, for it is essentially based on the radix-2r arithmetic.

III.PROPOSED SYSTEM

In the proposed system, a high performance 32*32 bit Booth multiplier has been designed, as shown in Fig.2. Booth encoder and decoder has been used to reduce the number of partial product terms to half.

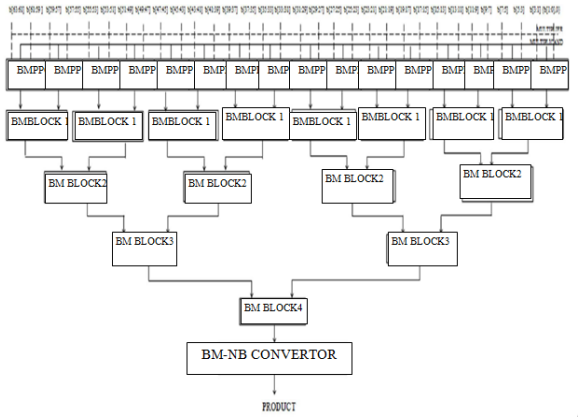

FIG 2. BLOCK DIAGRAM OF HIGH PERFORMANCE MULTIPLIER USING MODIFIED BOOTH ALGORITHM

Also, the proper alignment of the NB partial product rows is achieved by corresponding sign bit extension. The sign bits of each properly aligned NB row pairs is bit inverted before modified booth encoding. The RBPPR are generated, simply by inverting one of the NB partial product rows from each pair. The elimination of error correction vector (extra partial product row) is achieved by using Modified Partial Product generator. The selection of this technique is made, since it is one of the most useful methods for designing an area efficient RB MBE multipliers with power-of-two word length.

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The BMPP rows thus generated are added up pair wise in modified booth Multiplier summing tree by means of fast RBAs as a unit cell as proposed. Prior to its computation in modified booth multiplier summing tree, each bit pairs of modified booth multiplier rows with values (1, 1) are converted to (0, 0). The two partial product terms obtained at the output of the modified booth multiplier summing tree, is then added up by means of the High-Speed 128 bit Parallel- Prefix VLSI Ling Adders as proposed which also facilities the required RB-NB conversion at the final stage of the multiplier design. There are 5 stages in conventional Booth multiplier however by using 32 bit modified booth Multiplier using designed RBMPPG reduces the number of accumulation stage from 5 to 4 (i.e. a 25% reduction).This reduction shows improvement in delay, area & power.

IV.RESULTS

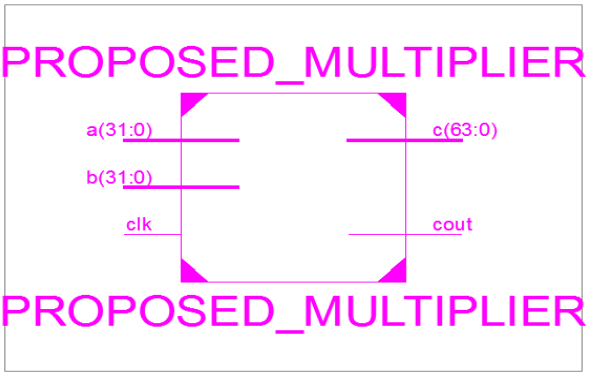

FIG 3. RTL SCHEMATIC

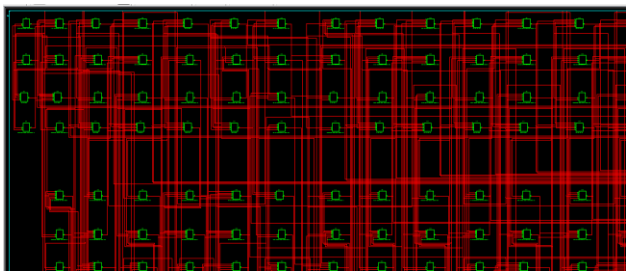

FIG4. TECHNOLOGY SCHEMATIC

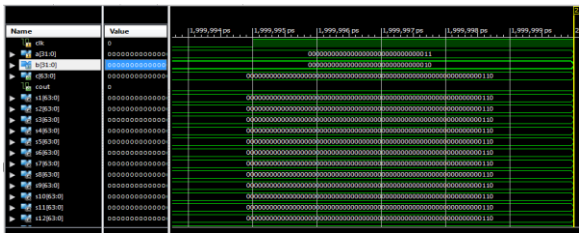

FIG.5 OUTPUT WAVEFORM

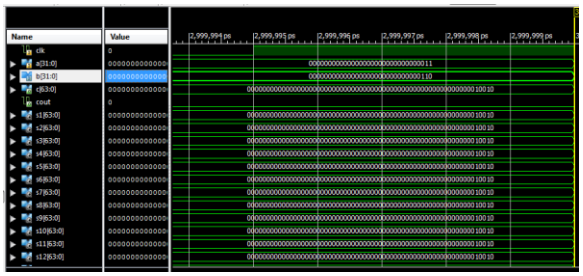

FIG 6. OUTPUT WAVEFORM

V.CONCLUSION

The high performance 32*32 bit modified booth multiplier architecture has been designed in this paper, by considering a tradeoff between area, power and delay. This design eliminates ECW that is introduced by the proposed design. Therefore RBPP accumulation stage is saved. The new multiplier using modified booth encoding technique can be applied to proposed design to reduce the number of BMPP rows from [N/4 +1] to [N/4]. An area efficient Modified Booth multiplier introduces delay in our architecture which has been minimized by means of delay

efficient BM-NB converter to some extent. The designed approach for 32*32 bit MBE multiplier shows improved performance over multiplier in terms of area and delay.

VI.REFERENCES

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