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Enhanced Fault Tolerant Parallel FFTs UsingParseval Checks and Error Correction Codes: A Study

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Abstract:*Reliability of mission critical systems is aweighty criterion for any system and is achieved by suitablefault detection techniques. Digital filters are most oftenintegrated in modern digital signal processing systems for theprocessing of signals.In few utilizations, apossible activity is that use of algorithmic based fault tolerance(ABFT) approaches that are endeavor and action of recursivequalities in identify as well as rectify faults. Communicationsand Signal processing utilities are more compatible toalgorithmic based fault tolerance. A few key building blocks indevices are FFTs. Numerous secured techniques recommended forrecognize as well as rectify faults in FFTs. Amidst of techniques,most probable utilization of Sum of squares or parseval check is themost generally glorious. At a recent time, one method employsthat put into effect of fault tolerance projected over similarfilters. During irregularity, the system first implemented forlookout Fast Fourier Transforms.*

Index Terms:Fast Fourier Transforms, Error CorrectionCodes, Alogarithmic Based Fault Tolerance, Soft errors

I. INTRODUCTION

Electronic circuits are increasingly present in automotive,medical, and space applications where reliability is critical.In those applications, the circuits have to provide somedegree of fault tolerance. This need is further increased bythe intrinsic reliability challenges of advanced CMOStechnologies that include, e.g., manufacturing variations andsoft errors. A number of techniques can be used to protect acircuit from errors. Those range from modifications in themanufacturing process of the circuits to reduce the numberof errors to adding redundancy at the logic or system level toensure that errors do not affect the system functionality [1].

To add redundancy, a general technique known as triplemodular redundancy (TMR) can be used. The TMR, whichtriplicates the design and adds voting logic to correct errors,is commonly used. However, it more than triples the areaand power of the circuit, something that may not beacceptable in some applications. When the circuit to beprotected has algorithmic or structural properties, a betteroption can be to exploit those properties to implement faulttolerance. One example is signal processing circuits forwhich specific techniques have been proposed over the years[2].Digital filters are one of the most commonly used signalprocessing circuits and several techniques have beenproposed to protect them from errors. Most of them havefocused on finite-impulse response (FIR) filters. Forexample, in [3], the use of reduced precision replicas wasproposed to reduce the cost of implementing modularredundancy in FIR filters.In [4], a relationship between the memory elements ofan FIR filter and the input sequence was used to detecterrors. Other schemes have exploited the FIR properties at aword level to also achieve fault tolerance [5]. The use ofresidue number systems [6] and arithmetic codes [7] has alsobeen proposed to protect filters. Finally, the use of differentimplementation structures of the FIR filters to correct errorswith only one redundant module has also been proposed [8].In all the techniques mentioned so far, the protection of asingle filter is considered. However, it is increasinglycommon to find systems in which several filters operate inparallel. This is the case in filter banks [9] and in manymodern communication systems [10]. For those systems, theprotection of the filters can be addressed at a higher level byconsidering the parallel filters as the block to be protected.This idea was explored in [11], where two parallel filterswith the same response that processed different input signalswere considered. It was shown that with only one redundantcopy, single error correction can be implemented. Therefore,a significant cost reduction compared with TMR wasobtained. In this brief, a general scheme to protect parallelfilters is presented. As in [11], parallel filters with the sameresponse that process different input signals are considered.The new approach is based on the application of errorcorrection

codes (ECCs) using each of the filter outputs asthe equivalent of a bit in and ECC codeword.

II. BACKGROUND WORK

[12] In this paper, Triple Modular Redundancy (TMR) andHamming Codes have been utilized to secure distinctivecircuits against Single Event Upsets (SEUs). In this paper, theutilization of a Novel Hamming approach on FIR Filters isexamined and actualized to give low many-sided quality,decrease deferral and region productive security methods forhigher bits information.

A novel Hamming code is proposed in this paper, to build theeffectiveness of higher information bits. In this paper, theyhave proposed system used to illustrate, how the parcel ofoverhead because of scattering the repetition bits, theirresulting expulsion, cushion to cushion postpone in thedecoder and utilization of aggregate range of FIR channel forhigher bits are lessened. These depend on the novel hammingcode implementation in the FIR channel rather than traditionalhamming code used to ensure FIR channel. In this planHamming code utilized for transmission of 7-bit informationthing.

[13] In this paper, the outline of a FIR channel with selfchecking abilities in view of the buildup checking isdissected. Normally the arrangement of deposits used tocheck the consistency of the consequences of the FIR channelare based of theoretic contemplations about the dynamicrange accessible with a picked set of buildups, the mathattributes of the blunders caused by a blame and on thenormal for the channel execution.

This investigation is regularly hard to perform and to acquireadequate blame scope the arrangement of picked buildups isoverestimated. Acquired outcome and thusly requires thatInstead, in this paper they have demonstrated how utilizing athorough blame infusion crusades permits to proficientlychoose the best arrangement of buildups.Test comes about originating from blame infusion crusades ona 16 taps FIR channel exhibited that by observing thehappened blunders and the location modules relating tovarious buildup has been conceivable to lessen the quantity ofdiscovery module, while paying a little decrease of the levelof SEUs that can be distinguished. Paired rationale rules theequipment execution of DSP frameworks.

[14] In this paper they have proposed engineering for theexecution of blame - tolerant calculation inside a highthroughput multirate equalizer for a deviated remote LAN.The range overhead is limited by abusing the mathematicalstructure of the Modulus Replication Residue Number System(MRRNS). They had exhibited that for our framework theterritory cost to redress a blame in a solitary computationalThe protection of parallel filters was done using ErrorCorrection Codes basically hamming code channel is 82.7%. Adaptation to internal failure insideMRRNS design is executed through the expansion ofrepetitive channels. This paper has introduced a nitty grittyinvestigation of the cost of actualizing single blamerectification capacity in a FIR channel utilizing the MRRNS.

Table I: Relation between information bits and paritybits.

Information Bits	Parity Bits
4	3
8	4
12	5
27	6

Hamming codes are mainly used to locate whether anytransmitted bit is in error and to correct it, so that error freebits are received at the receiver. To protect information bitsto be transmitted from errors Hamming codes transmit somenumber of parity bits along with the information bits. Thenumber of parity bits to be added is based on the Hammingrule

$r+p+1>=2^p$

So according to these observations to protect four informationbits from errors three parity bits have to be added. It isexplained in Table 1.With the same concept of hammingcodes erroneous outputs and faulty filter can be corrected.

Table II: Relation between Filters to be protected and filtersadded as redundant filters for Fault tolerance

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Filters to be protected	Redundant Filters
4	2
8	2
12	2
27	2

III. PROPOSED FRAMEWORK

The aim of error tolerant design is to protect parallelFFTs from errors. Various schemes have been proposed forerror detection and correction in FFTs. One of the basic andsimple methods is error correction using hamming codes.

Unlike parity code which can detect only odd bit error, thehamming code can detect two bit errors and correct oneerror. Similar to other error correction codes, hammingcodes also utilizes the parity bit which is generated for thecorresponding input sequence for detecting errors [14]. Itachieves higher code rate with minimum distance of three.The number of parity bits depends on the total number ofdata bits.

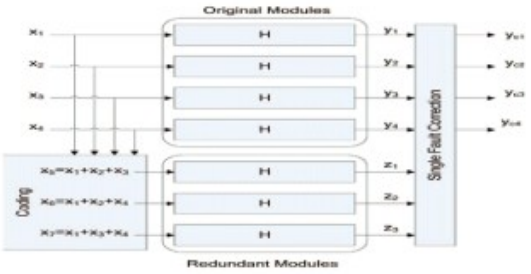

Fig.1 ECC-Based Scheme for Four Filters and a Hammingcode

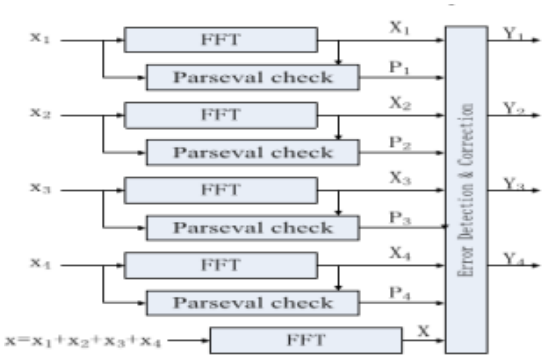

Fig. 2 Parity-SOS (first technique) Fault-TolerantParallel FFTs.

The place to begin for our work is that the protection themebased on the utilization of ECCs that was for digital filters.This theme is shown in Fig.1. In this example, astraightforward single error correction playacting code isemployed. The initial system consists of 4 FFT modules and 3redundant modules is value-added to sight and correct errors.The inputs to the 3 redundant modules area unit linear combosof the inputs and that they area unit used to check linearcombos of the outputs. For example, the input to the primaryredundant module is

$x5 = x1 + x2 + x3.$

And since the DFT is a linear operation, its output *z5* can beused to check that

$Z5 = Z1 + Z2 + Z3.$

This will be denoted as c1 check. The same reasoning appliesto the other two redundant modules that will provide checks*c2* and *c3*. For example, for an error affecting z1, this can bedone as follows:

$Z1C[n] = Z5[n]-Z2[n]-Z3[n].$

Similar correction equations can be used to correct errors onthe other modules. More advanced ECCs can be used tocorrect errors on multiple modules if that is needed in a givenapplication. For example, to protect four FFTs, threeredundant FFTs are needed, but to protect eleven, the numberof redundant FFTs in only four. This shows how the overheaddecreases with the number of FFTs.

$X1C = X-X2-X3-X4.$

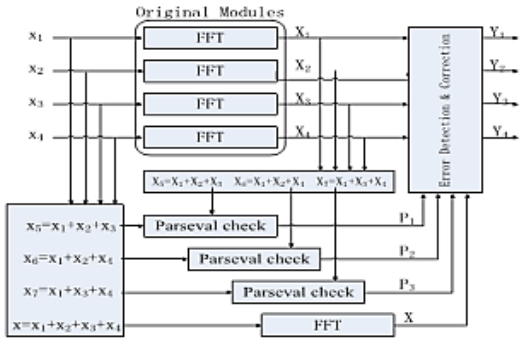

Fig. 3 Parity-SOS-ECC (second technique) Fault-TolerantParallel FFTs.

Another possibility to combine the SOS check and the ECCapproach is instead of using an SOS check per

FFT, use anECC for the SOS checks. Then as in the parity-SOS scheme,an additional parity FFT is used to correct the errors. Thissecond technique is shown in Figure 3

The main benefit over the first parity SOS scheme is to reducethe number of SOS checks needed. The error location processis the same as for the ECC scheme in Figure.1 and correctionis as in the parity-SOS scheme. In the following, this schemewill be referred to as parity-SOS-ECC (or second proposedtechnique)

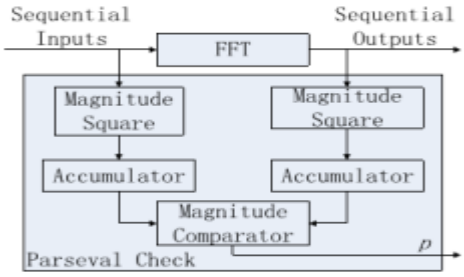

Fig. 4 Implementation of the SOS check

Results and discussion mainly includes the behaviouralsimulation and RTL schematic implementation of the design.RTL schematic describes the logic utilization in a FPGA.

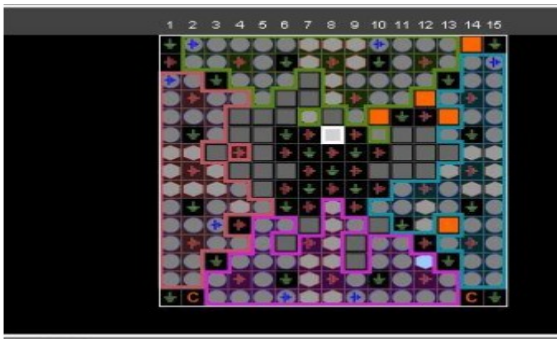

Fig.5 Input Output Pin Diagram of Proposed SchemeUsing

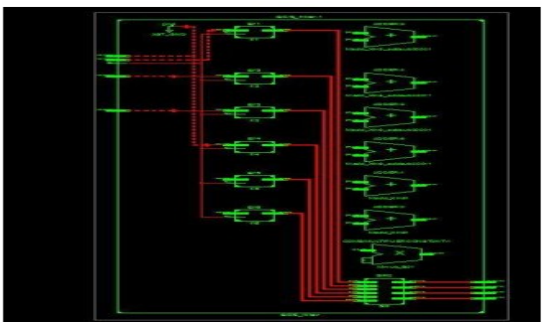

Fig.6 RTL Schematic of Proposed scheme Using Xilinx ISE

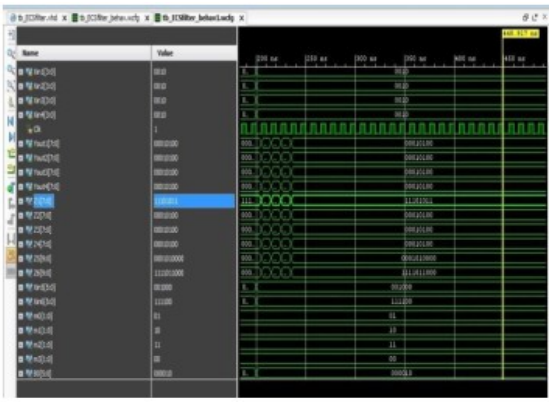

Fig. 7 Behavioral Simulation of Parallel Filters with FaultInjected at Z1 Using Xilinx ISE.

IV. CONCLUSION

Detecting and correcting errors like imperative consistency aretroublesome in signal process that will increase the utilizationof fault tolerant implementation.The previously proposedTechnique was based on the use of Error Correction Codes(ECCs). This method considers each filter as a bit in the ECC.The proposed scheme beats the ECC technique (similar faulttolerant capability with lower cost). Therefore, the proposedscheme can be useful to implement fault tolerant parallelfilters.Proposed is a part economical technique todiscover and correct single errors. The approach is based onapplying SOS-ECC check to the parallel FFT outputs todiscover and proper errors. The SOS checks ar unit
accustomed discover and find the errors and an easy parityFFT is employed for correction.

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