International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue-01
January 2018

Trustworthy Low-Power Multiplier Design using Fixed-Width Replica Redundancy Block: A Review

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Abstract:A reliable low-power multiplier design by adoptingalgorithmic noise tolerant (ANT) architecture with truncatedbinary multiplier to build the fixed width reduced precisionreplica redundancy block (RPR).The proposed ANT architecture canmeet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with errorcompensation circuit via analyzing of probability and statistics. Using the partial product terms of input correction vector and minorinput correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified.

Index Terms:Algorithmic Noise Tolerant (ANT), Low-Power Multiplier.

I. INTRODUCTION

In recent years, the rapid growth for portablewireless computation devices enhances the requirement forultralow power devices. To reduce the power dissipation,voltage scaling is heavily used as an accurate low-powertechnique because the power consumption in CMOS circuitsis directly related to the square of voltage [1]. However, indeep-submicrometer process technologies, noise problemshave faced difficulty to design the reliable and accuratemicroelectronics systems; hence, these designs aredeveloped to intensify noise tolerance. [2]–[12].A hostile low-power technique, called voltageoverscaling (VOS), was introduced in [4] to lower voltagebeyond critical supply voltage without surrendering thethroughput. However, VOS degrades signal-to-noise ratio(SNR). A novel (ANT) technique [2] combined VOS blockwith reduced-precision replica (RPR), which removes softerrors accurately and saves energy Some ANT deformationdesigns are proposed in [5]–[9] and the ANT design isfurther extended to system level in [10]. Whereas, the RPRin the ANT designs of [5]–[7] are designed in a organizedmanner, which are not easily versatile.The RPR designs in the ANT designs of [8] and [9] canoperate with high speed, but their hardware complexity ishigh.

However, the RPR styles within thehymenopterous insect styles of are designed in avery customized manner, that aren't simplyadopted and perennial. The RPR styles within thehymenopterous insect style will operate in a veryin no time manner, however their hardwarecomplexness is simply too advanced. As a result,the RPR style within the hymenopterous insectstyle of remains the foremost common style due toits simplicity. However, adopting with RPR inought to still pay further space overhead andpower consumption. In this paper, we have atendency to additional projected a straightforwardmeans victimization the fixed-width RPR toswitch the full-width RPR block. victimization thefixed-width RPR, the computation error will becorrected with lower power consumption andlower space overhead. we have a tendency to takeuse of chance, statistics, and partial product weightanalysis to seek out the approximate compensationvector for a lot of precise RPR style. so as to notincrease the crucial path delay, we have atendency to prohibit the compensation circuit inRPR should not be set within the crucial path. As aresult, we will notice the hymenopterous insectstyle with smaller circuit space, lower powerconsumption, and lower crucial provide voltage.

II. LITERATURE SURVEY

The fixed-width RPR to replace the full-width RPR blockin the ANT design, as shown in Fig. 2[5], which can not onlyprovide higher computation precision, lower power consumption,and lower area overhead in RPR, but also perform with higherSNR, more area efficient, lower operating supply voltage, andlower power consumption in realizing the ANT architecture[7].The fixed-width designs are usually applied in DSP applications toavoid infinite growth of bit width. Cutting off n-bit leastsignificant bit (LSB) output is a popular solution to construct afixed-width DSP with n-bit input and output function. Thehardware complexity and power consumption of a fixed-widthDSP is usually about half of the full-length one. However,truncation of LSB part results in rounding

error, which needs to becompensated precisely[6]. Many literatures have been presented toreduce the truncation error with constant correction value or withvariable correction value. The circuit complexity is to compensatewith constant corrected value can be simpler manner that ofvariable correction value; however, the variable correctionapproaches are usually more precise.

In their compensation method is to compensate thetruncation error between the full-length multiplier and the fixedwidth multiplier. However, in the fixed-width RPR of an ANTmultiplier, the compensation error we need to correct is the overalltruncation error of MDSP block. Unlike the compensation methodis to compensate the truncation error between the full-lengthMDSP multiplier and the fixed-width RPR multiplier. Innowadays, there are many fixed-width multiplier designs appliedto the full-width multipliers. However, there is still no fixed-widthRPR design applied to the ANT multiplier designs[8]

To achieve more precise error compensation, compensatethe truncation error with variable correction value. We constructthe error compensation circuit mainly using the partial productterms with the largest weight in the least significant segment. Theerror compensation algorithm makes use of probability, statistics,and linear regression analysis to find the approximatecompensation value[9]. To save hardware complexity, thecompensation vector in the partial product terms with the largestweight in the least significant segment is directly inject into thefixed-width RPR, which does not need extra compensation logicgates . To further lower the compensation error, also consider theimpact of truncated products with the second most significant bitson the error compensation[10]. In this method propose an errorcompensation circuit using a simple minor input correction vectorto compensation the error remained. In order not to increase thecritical path delay, locate the compensation circuit in thenoncritical path of the fixed-width RPR. As compared with thefull-width RPR design, the proposed fixed-width RPR multipliernot only performs with higher SNR but also with lower circuitryarea and lower power consumption[12].

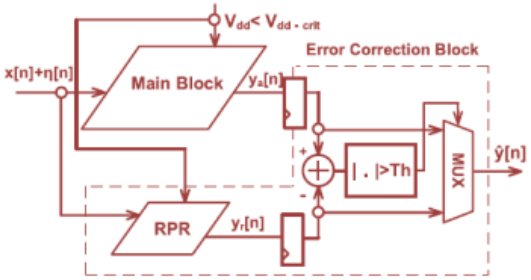

Fig. 1. ANT architecture

The ANT technique includes both main digital signalprocessor (MDSP) and error correction (EC) block, as shown inFig. 1. [2]To meet ultralow power demand, VOS is used in MDSP.However, under the VOS, once the critical path delay Tcp of thesystem becomes greater than the sampling period Tsamp, the softerrors will occur. It leads to severe degradation in signal precision.In the ANT technique, a replica of the MDSP but with reducedprecision operands and shorter computation delay is used as ECblock.

III. PROPOSED FRAMEWORK

In this paper, we further proposed the fixed-width RPR toreplace the full-width RPR block in the ANT design,as shown inFig.2, which can not only provide higher computation precision,lower power consumption, and lower area overhead in RPR, butalso perform with higher SNR, more area efficient, loweroperating supply voltage, and lower power consumption inrealizing the ANT architecture. We demonstrate our fixed-widthRPR-based ANT design in an ANT multiplier. The fixed-widthdesigns are usually applied in DSP applications to avoid infinitegrowth of bit width. Cutting off n-bit least significant bit (LSB)output is a popular solution to construct a fixed-width DSP withn-bit input and n-bit output. The hardware complexity andpower consumption of a fixed-width DSP is usually about halfof the full-length one. However, truncation of LSB part resultsin rounding error, which needs to be compensated precisely.

Many literatures have been presented to reduce the truncationerror with constant correction value or with variable correctionvalue. The circuit complexity to compensate with constantcorrected value can be simpler than that of variable correctionvalue; however, the variable correction approaches are usuallymore precise. Their compensation method is to compensate

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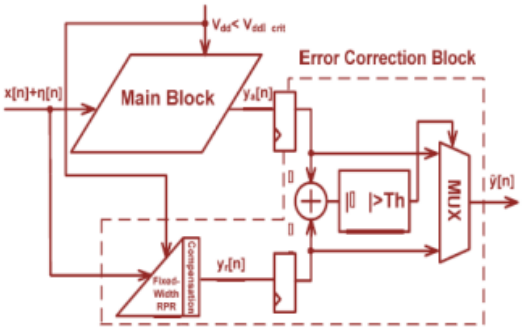

Fig. 2. Proposed ANT architecture with fixed-width RPR

To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm makes use of probability, statistics, and linear regression analysis to find the approximate compensation value. To save hardware complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates. To further lower the compensation error, we also consider the impact of truncated products with the second most significant bits on the error compensation. We propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the noncritical path of the fixed-width RPR. As compared with the full-width RPR design, the proposed fixedwidth RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

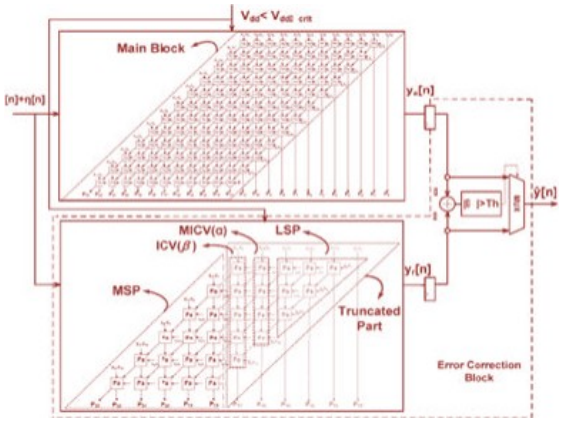

Fig.3. 12 × 12 bit ANT multiplier is implemented with thesix-bit fixedwidth replica redundancy block.

In the ANT design, the function of RPR is to correct theerrors occurring in the output of MDSP and maintain the SNRof whole system while lowering supply voltage. In the case ofusing fixed-width RPR to realize ANT architecture, we not onlylower circuit area and power consumption, but also acceleratethe computation speed as compared with the conventional fulllength RPR. However, we need to compensate huge truncationerror due to cutting off many hardware elements in the LSB partof MDSP. In the MDSP of n-bit ANT Baugh–Wooley arraymultiplier.

The(n/2)-bit unsigned full-width Baugh–Wooley partial productarray can be divided into four subsets, which are mostsignificant part (MSP), input correction vector [ICV(β)], minorICV *[MICV(α)],* and LSP, as shown in Fig3. In the fixed widthRPR, only MSP part is kept and the other parts are removed.Therefore, the other three parts of *ICV(β)*, *MICV(α)*, and LSPare called as truncated part. The truncated *ICV(β)* and *MICV(α)*

are the most important parts because of their highest weighting.Therefore, they can be applied to construct the truncation errorcompensation algorithm. To evaluate the accuracy of a fixedwidth RPR, we can exploit the difference between the (n/2)-bitfixed-width RPR output and the 2n-bit full-length MDSPoutput, which is expressed as

$$\varepsilon = P - Pt$$

where P is the output of the complete multiplier in MDSP andPt is the output of the fixed-width multiplier in RPR.

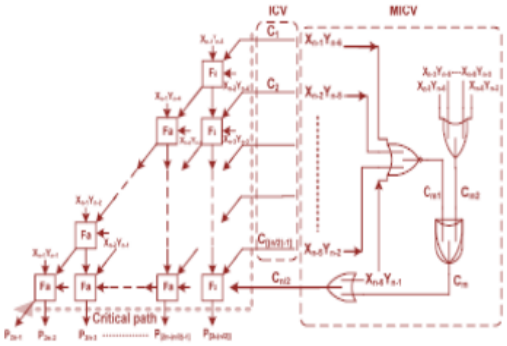

Fig.4. Proposed high-accuracy fixed-width RPR multiplierwith compensation constructed by the multiple truncationEC vectors combined ICV together with MICV.

To realize the fixed-width RPR, we construct one directlyinjecting ICV(β) to basically meet the statistic distribution andone minor compensation vector MICV(α) to amend theinsufficient error compensation cases. The compensation vectorICV(β) is realized by directly injecting the partial terms of*Xn−1Yn/2, Xn−2Y(n/2)+1, Xn−3Y(n/2)+2, . . . , X(n/2)+2Yn−2*.

These directly injecting compensation terms are labeled *as C1,C2,C3, . . . ,C(n/2)−1* in Fig. 4. The other compensationvector used to mend the insufficient error compensation case isconstructed by one conditional controlled OR gate. One input ofOR gate is injected by *X(n/2)Yn−1*, which is designed to realizethe function of compensation vector β.

IV. CONCLUSION

A Low error and area efficient fixed width RPR based ANT multiplier design is presented.In this paper, a low-error and area-efficient fixed-widthRPR-based ANT multiplier design is presented. The proposed12-bit ANT multiplier circuit is implemented. In the presented 12-bit by 12-bitANT multiplier, the circuitry area in our fixed-width RPR canbe saved by 45%, the lowest reliable operating supply voltage inour ANT design can be lowered to 0.623 VDD, and powerconsumption in our ANT design can be saved by 23% ascompared with the state-of-art ANT design.

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