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Low power 16 bit ALU design using Full adder and Multiplexer

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Abstract: *This project describes the techniques for fabricating a high speed ALU using pass transistor logic. Double pass transistor logic is shown to improve the circuit performance at reduced supply voltage. Using DPL technique a 16 bit ALU is designed with the help of multiplexers and full adder. In the existing method full adders and multiplexers were designed using PTL method. The main component in the ALU is full adder. In CMOS method eight transistor full adder and CMOS based multiplexers are used. By reducing area and by using DPL based multiplexers low power ALU is attained. In the implementation of ALU using DPL method, the power and area are reduced compared to PTL method. With the increase in the bit size there are a number of uses, Speed of the processor increases as it can accommodate large bit size and number of applications increases. Results are observed using Microwind and Digital Schematic.*

***Index Terms*— 8-bit ALU, DPL (Double Pass transistor logic), Full Adder.**

I. INTRODUCTION

The Arithmetic Logic Unit is essentially the heart of a CPU. It has more applications in DSP and micro-processors. In the past, VLSI designers concentrated more on area, performance, cost and reliability. The least importance was given to power. Now a day's power is given primary importance than area and speed. The two low power logic styles used in ALU are CMOS logic and PTL logic. Two important characteristics of CMOS logic are high noise immunity and low static power consumption. Since the one transistor of the complementary pair is always turned off. For high density logic functions CMOS logic is best. Pass transistor logic reduces transistor count by eliminating redundant transistors. By reducing transistors we can reduce area and then power. Here transistors are used as a switch to pass logic levels between nodes of a circuit, instead of connecting switches directly to supply voltages. This reduces number of active devices. With the increase in usage of portable devices, need for low power is increased greatly. Designers are always giving more importance to power rather than speed, because there is a reliability problem in high performance system. High performance systems often turns hot, and high temperature tends to exacerbate several silicon failure mechanisms. Every 10 degrees Celsius increase in operating temperature roughly doubles a component failure rate. From the environment point of view, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence the lower the impact on global environment. There is always a tradeoff between power, area and delay. Depending upon requirement, the designer will selects the low power logic techniques.

II. RELATED WORK

ARITHMETIC LOGIC UNIT

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. This is in contrast to a floating-point unit (FPU), which operates on floating point numbers. An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). A single CPU, FPU or GPU may contain multiple ALUs. The inputs to an ALU are the data to be operated on, called operands, and a code indicating the operation to be performed and, optionally, status information from a previous operation; the ALU's output is the result of the

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performed operation. In many designs, the ALU also exchanges additional information with a status register, which relates to the result of the current or previous operations.

ALU DESIGN USING CMOS LOGIC.

The adder is one of the most important components of a CPU, Arithmetic logic unit (ALU) and address generation like cache. In addition, full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. In the CMOS method 8-T full adder is used. Fig.1 shows the circuit level diagram of 8-T full adder. Eight transistor Full adder is designed using two 3T XOR gates. The Full adder inputs are three and the outputs of the Full adder are six namely, SUM, CARRY, AND, EXOR, EXNOR, OR. Additional OR circuit is used to perform OR operation. We can get EXNOR operation by giving output of EXOR to inverter circuit. Additional AND circuit was used to perform AND operation. The multiplexers have been used in the ALU design for input and output signal selection. In CMOS method multiplexer is designed using CMOS logic. Inputs to 4:1 multiplexer are logic1, logic0, B0 and B0‟. S0 and S1 are select signals. Depending upon select signals input will be selected as output. In CMOS method multiplexers are designed with the help of CMOS logic.

ALU is designed by using 4x1 multiplexer, 2x1 multiplexer and Full adder. The input and output sections consist of 4x1 and 2x1 multiplexers and the main logic is implemented by using full adder. In the first design multiplexers and full adder are implemented using the CMOS logic. A set of three select signals have been used in the design to determine the operation being performed and the inputs and outputs being selected. Ripple carry adder is used in ALU. Here the carry bit cascaded from input to output stage. The 4-bit ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders

The 4-bit ALU is designed in 180nm, n-well CMOS technology. For the INCREMENT operation logic “0” is applied as an input. For DECREMENT operation logic1 applied as input. The complement of B is used for SUBTRACTION operation. The full adder performs the SUBTRACT operation by two’s complement method. An INCREMENT operation is analyzed as adding “1” to the addend and DECREMENT is seen as a subtraction operation.

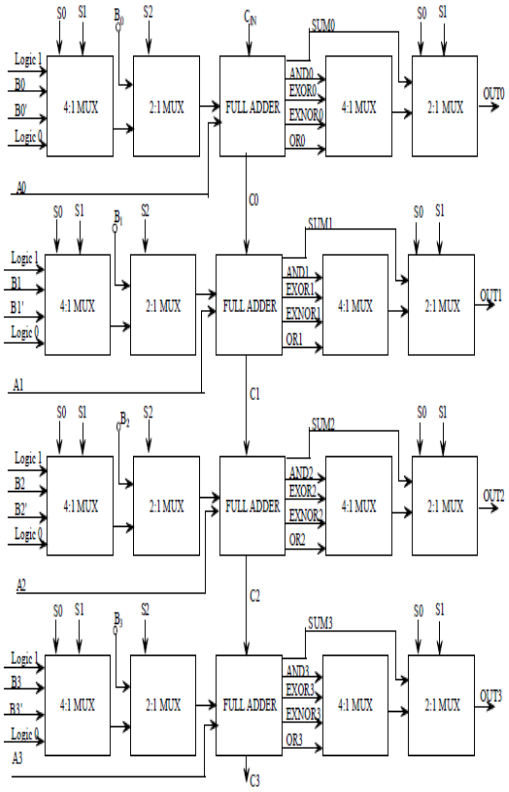

Fig.1 Block Diagram of 4-bit ALU

III. ALU DESIGN USING PTL

Full adder Design: In PTL method Full adder is designed using six transistors. Six transistor Full adder is designed using 2T XOR gate. In PTL method two transistor XOR gates can be designed using general logic implementation. The circuit operation is as follows when A=0 and B=0 both the pmos transistors ON and it will produce the output low. When either one of the transistor is ON it produces output as high, when A=1 and B=1 both the pmos transistors are OFF and it will produces output as low. The six transistor Full adder is shown in the Fig. 2.

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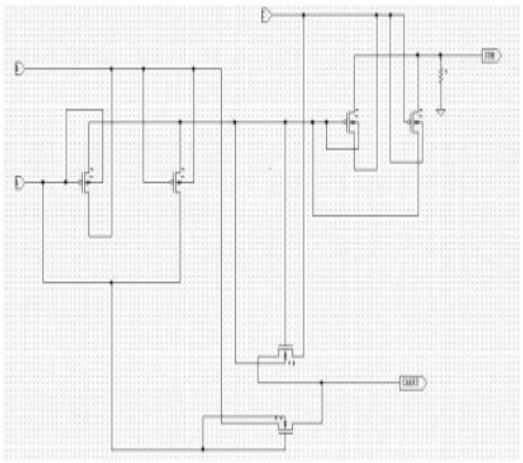

Fig. 2 Schematic of 6-T Full Adder

MULTIPLEXER DESIGN:

Here the multiplexer is implemented using pass transistors. This design is simple and efficient in terms of area and timing. The pass transistor design reduces the parasitic capacitances and results in fast circuits. There are two kinds of multiplexers implemented: 2 to 1 multiplexer and 4 to 1 multiplexer. Schematic of 4 to 1 Multiplexer and 2 to 1 Multiplexer is shown in the Fig.3 and Fig.4 respectively.

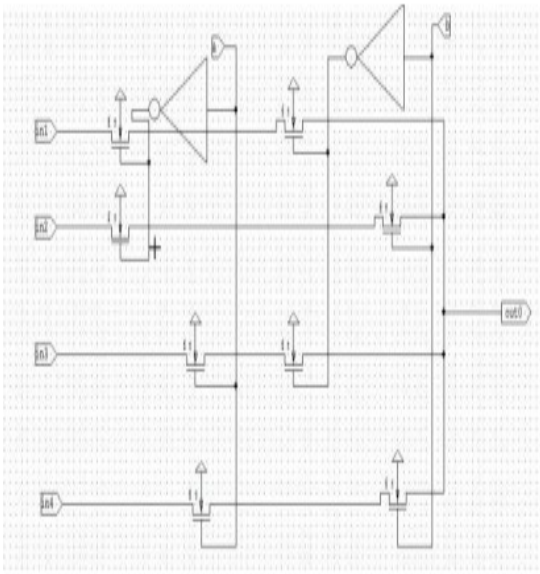

Fig 3: 4:1 Multiplexer

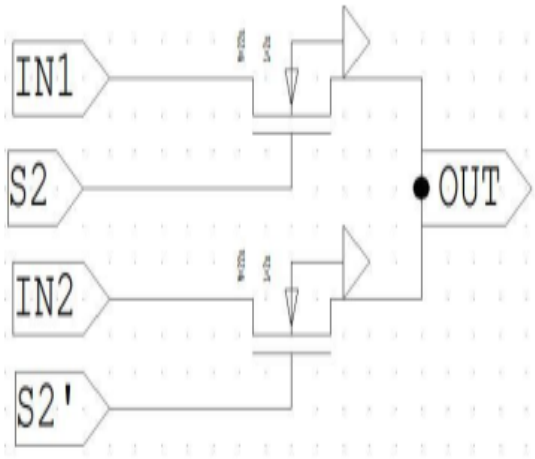

Fig 4: 2:1 Multiplexer

ALU DESIGN:

Here ALU is designed using 6 transistor full adder and pass transistor logic based multiplexers. The pass transistor design reduces the parasitic capacitances and results in fast circuits. ALU operation depends upon select signals s0, s1 and s2. If s2=0 then it performs arithmetic operations. If s2=1 then it performs logical operations.

METHOD FOR ALU DESIGN.

In Central Processing Unit (CPU) of a computer, Arithmetic and Logic Unit (ALU) is a fundamental building block and even the simplest microprocessors contain ALU. It is responsible for performing arithmetic as well as logical operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR. Eight 4x1 multiplexers, eight 2x1 multiplexers and four full adders are present in 4bit ALU. The 4-bit ALU is designed in 250 nm, n-well CMOS technology. An INCREMENT and DECREMENT operations takes place when logic „1" and logic „0" are applied as an input. An INCREMENT operation is analyzed as adding „1" to the addend and DECREMENT is seen as a subtraction operation. For SUBTRACTION operation two's complement method is used in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR. Fig. 1 shows the 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit.

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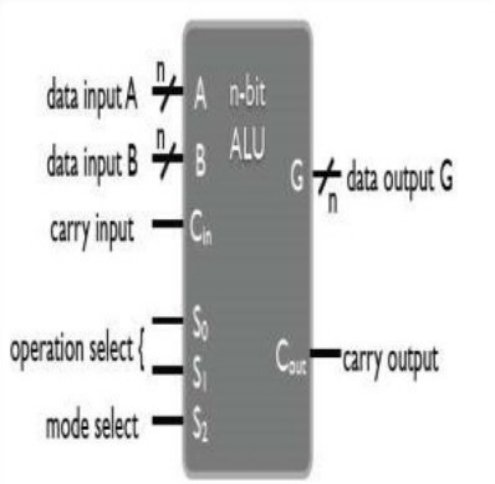

Fig. 5 An n-bit Arithmetic and Logic Unit

Based on the condition of the select signals, the multiplexer selects the appropriate input and gives it to the full adder which then computes the results. At the output of the multiplexer stage selects the appropriate output and route it to output port. Table 1 shows the truth table for the operations performed by the ALU based on the status of the select signal .The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig. 6 shows multiplexer logic at input port and Fig. 7 shows multiplexer logic at output port. By using schematic editor of Tanner EDA the schematic of 4-bit ALU is designed. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

Table 1: Truth table of ALU

Selection Lines			Operations
S2	S1	S0	
0	0	0	AND
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBSTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

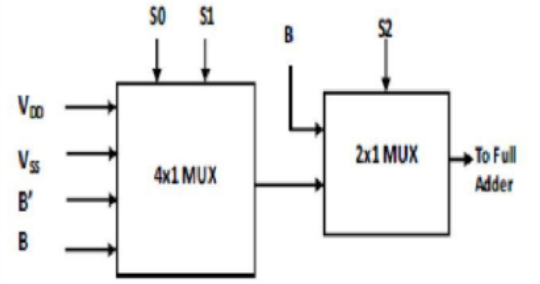

Fig. 6 Multiplexer logic at the input stage

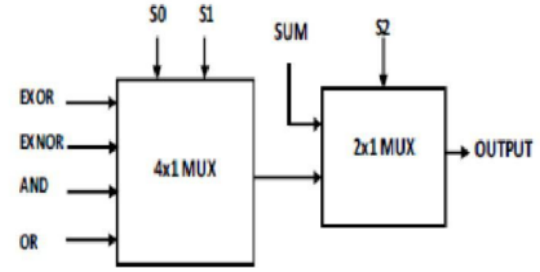

Fig. 7 Multiplexer logic at the output stage

ALU Design Using DPL Technique.

In the extension a 16 bit ALU is designed in three different ways by using multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and logic is implemented by using full adder. A set of three select signals have been incorporated in the design to determine the operation being performed and the inputs and outputs being selected. Figure 4 shows the block diagram of 4-bit ALU with the CARRY bit cascading all the way from first stage to fourth stage. The ALU consists of eight 4x 1 multiplexers, four 2x 1 multiplexers and four full adders. The 4-bit ALU is designed in 180nm, n-well CMOS technology. For the INCREMENT and DECREMENT operations logic '1' and logic '0' are applied as inputs respectively. The complement of B is used for SUBTRACTION operation. The full adder performs the SUBTRACT operation by two's complement method. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation.

The outputs from the full adder are SUM, EXOR, EXNOR, AND & OR. Based on the condition of the select signals, the multiplexer stage selects the appropriate inputs and gives it to the full adder. The full adder computes the results. The multiplexer at the output stage selects the appropriate output and sends it out. Table

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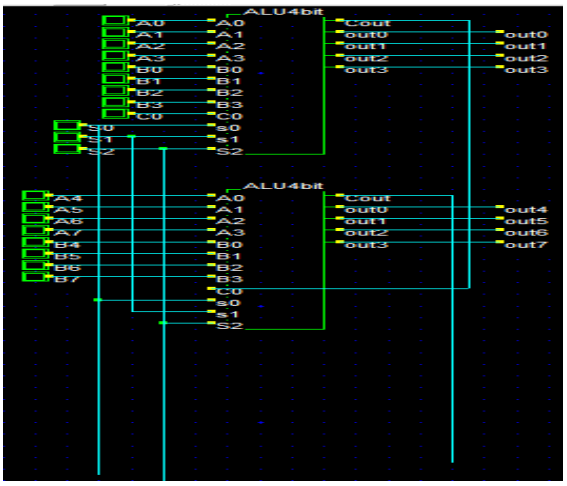
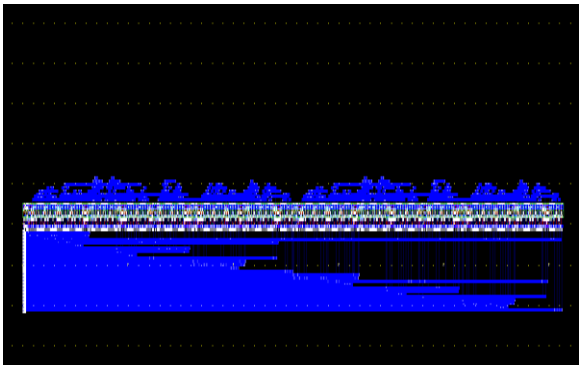
I shows the truth table for the operations performed by the ALU based on the status of the select signals. The schematic view of ALU describes the transistor level or higher abstraction levels of the circuit. It also can be drawn connectivity between the components and describes aspect ratios of the transistor can be modified along with the design.

IV. EXPERIMENTAL RESULTS

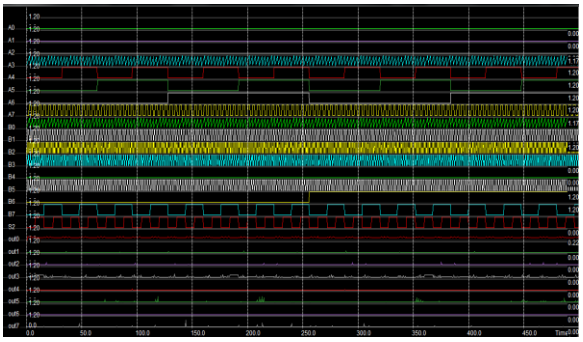
8 bit ALU Schematic.



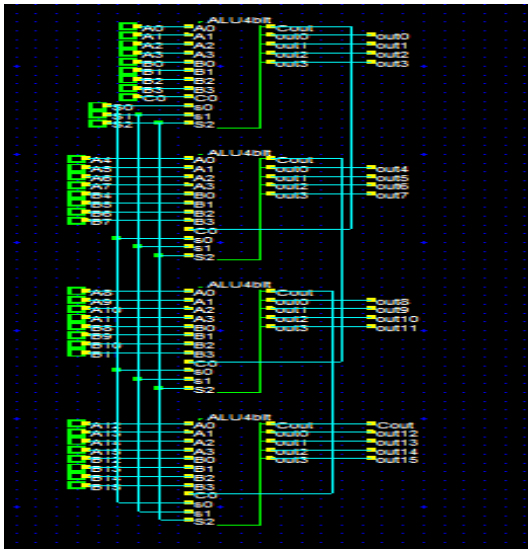
Layout Design.



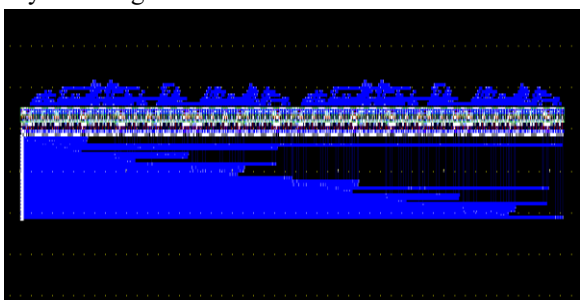
Simulation.



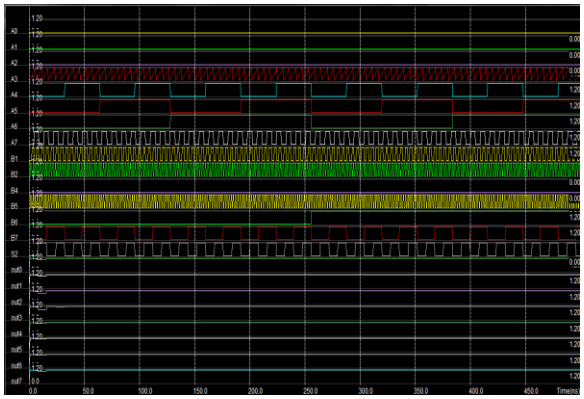
16 bit ALU Schematic.



Layout Design.



Simulation.



COMPARISION Table.

Design	Power
8 bit ALU	7.947mw
16bit ALU	1.409mw

V. CONCLUSION

A 16 bit ALU designed using DPL method with the help of multiplexers and full adder. Results show that an average power consumed in an 16 bit ALU using DPL logic is much better when compared with PTL logic. It is observed that the number of transistors in DPL method is less than PTL method by which, Power consumption is reduced. So area is reduced and power also reduced.

REFERENCES

[1]. R. Shalem, E. John, and L.K.John, "A novel low-power energy Recovery full adder cell," in Proc. Great Lakes Symp. VLSI,Feb.1999, pp.380–383.

[2]. A.Sharma, RSingh and R. Mehra, " Low Power TG Full Adder Design Using CMOS Nano Technology"

[3]. T. Esther Rani, M. Asha Rani, Dr. Rameshwar Rao, "Area Optimized Low Power Arithmetic And Logic Unit", 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[4]. K. Nehru, A. Shanmugham, Dr. Dharmila Thenmozhi, " Design Of Low Power ALU Using 8T FA and PTL Based MUX Circuits", IEEEInternational Conference On Advances In Engineering, Science And Management (ICAESM - 2012) March 30, 31, 2012.

[5]. Pakkiraiah chakali, Adilakshmi Siliveru, Neelima Koppala " Design of High speed Six transistor Full adder using a Novel Two Transistor XOR gates", 2012 International journal of Advanced Research in computer science and Electronics Engineering.

[6].Chandra srinivasan thesis "Arithemetic Logic Unit (ALU) Design Using Reconfigurable CMOS Logic" in the department of electrical and computer engineering, ,page no 55, 2003.