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Design a high speed fft using carry skip adder for communication

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ABSTRACT: *A carry skip adder (CSKA) structure is presented which has lower power consumption with a higher speed. The performance of the conventional CSKA is improved by achieving the speed enhancement by applying concatenation and incrementation schemes. The existed structure utilizes AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates for the skip logic. The existed system is complex in area. The Fast Fourier Transform (FFT) is an efficient algorithm to compute the DFT and its inverse. The FFT plays a key role in the field of communication systems like Digital Video or Audio Broadcasting, Wireless LAN with Standards of IEEE 802.11, High Speed Digital Subscriber Lines. This paper utilizes the implementation of folding technique using radix-2 DIT FFT algorithm. The proposed algorithms are used in radix-2 butterfly in all stage. The proposed algorithm is area efficient and consumed delay in previous algorithm. The all design are implementation vertex-6 device family Xilinx software.*

KEYTERMS: Fast Fourier Transform (FFT), AND-OR-INVERT (AOI), OR-AND-INVERT (OAI), CSKA.

I. INTRODUCTION

The Fourier Transform is an efficient approach in signal processing, particularly for applications in Orthogonal Frequency Division Multiplexing (OFDM) systems. The Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT.

The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations.

The FFT hardware can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture consists of a single processing element and various units of memory. The merits of memory architecture include low power and low cost when compared to that of other styles. The specific demerits are greater latency and lower throughput.

The above demerits of the memory architecture are totally eliminated by pipeline architecture at the expense of extra hardware in an acceptable way. The various types of pipeline architecture include Single delay feedback (SDF), Single delay commutator (SDC) and multiple delay commutator (MDC). The pipeline architecture is a regular structure which can be adopted by using hardware description language in an easy manner. In the recent years, the communication systems need to transmit voice and video signals of high quality in an efficient manner. In present day the efficient module is a high speed, reliable technology of communication.

High-speed FFT architectures are necessary to implement several communication systems, signal processing systems. The FFT blocks are also used in mechanical engineering and civil engineering applications. FFT has been considered as the most efficient way of implementing the discrete Fourier transform (DFT) and it was first implemented in 1965. The efficiency of the FFT algorithm lies in its reduced number of arithmetic operations. DFT has the order O (N * N) of arithmetic operations whereas FFT has the order of O (N log N) arithmetic operations. If the architecture is designed for complex inputs, the number of arithmetic

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operations becomes approximately double when compared to those which are designed for real inputs.

II.EXISTED SYSTEM

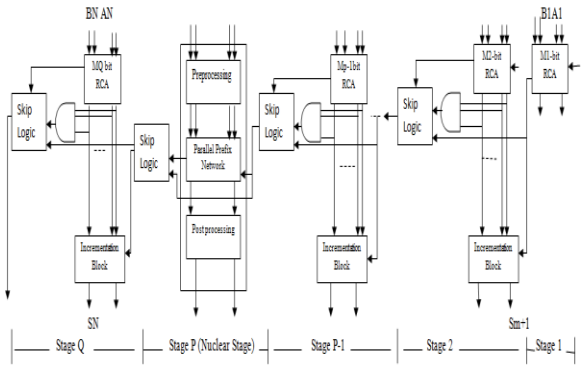

FIG. 1 STRUCTURE OF THE EXISTED HYBRID VARIABLE LATENCY CSKA

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, it is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the existed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

III.PROPOSED SYSTEM

Proposed method are used in binary input is going to the serial input serial output (SISO) shift register as shown in Figure 2. In proposing algorithm consist of SISO, and carry skip adder (CSKA), adder, Subtractor, Single path Delay Feedback (SDF) Pipeline, Folding architecture.

SISO: - SISO technique depends on the binary input. Suppose the binary input of the system is 8 word length, then eight delay flip flops are used in SISO register.

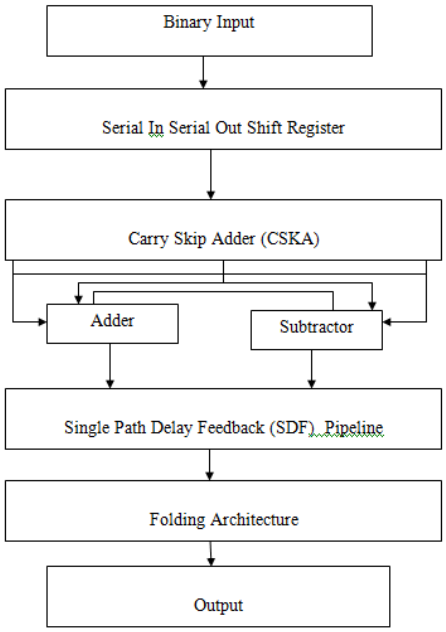

FIGURE 2: FLOW CHART OF PROPOSED ALGORITHM

The algorithm specifies that all possible AND terms are created white cell and all possible NAND terms are created gray cell. The white cell consists of full adder and AND gate, but the gray cell consists of full adder and NAND gate.

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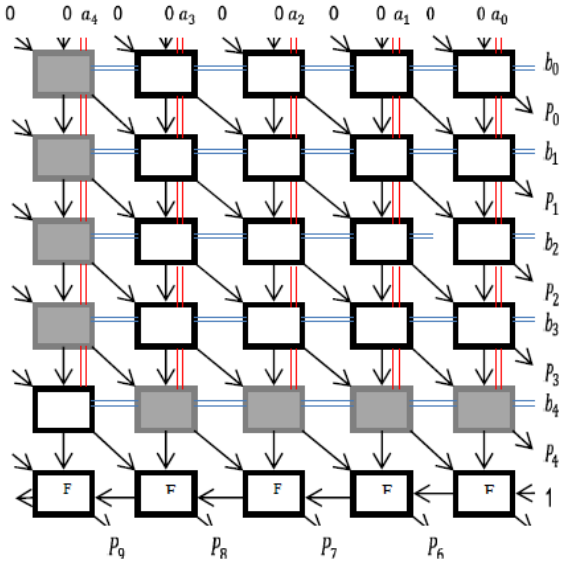

FIGURE 3: BLOCK DIAGRAM OF SIGN MULTIPLIER

The multiplication is consisting of 4 multiplications, 2 adders and 1 subtraction. But in the existed complex multiplication is consisting of 3 multiplications, 1 adder and 1 subtraction in shown in figure 4.

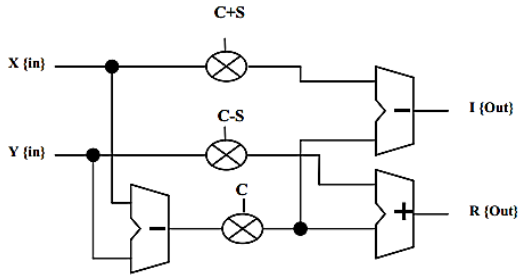

FIGURE 4: BLOCK DIAGRAM OF COMPLEX MULTIPLICATION

Subtractor:- Subtractor is consist of half subtractor and full subtractor depends on word length in algorithm. Single-path Delay Feedback Pipeline Architecture:- Herbert L. Groginsky and George A. Works introduced a feedback mechanism in order to minimize the number of delay elements. In the proposed architecture one half of outputs from each stage are fed back to the input data buffer when the input data are directly sent to the butterfly.

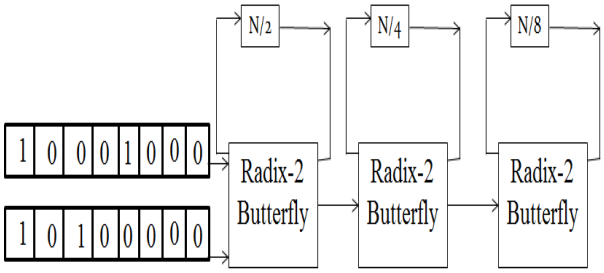

FIGURE 5: FLOW GRAPH OF THE RADIX-2 SDF PIPELINE ARCHITECTURE

IV.RESULTS

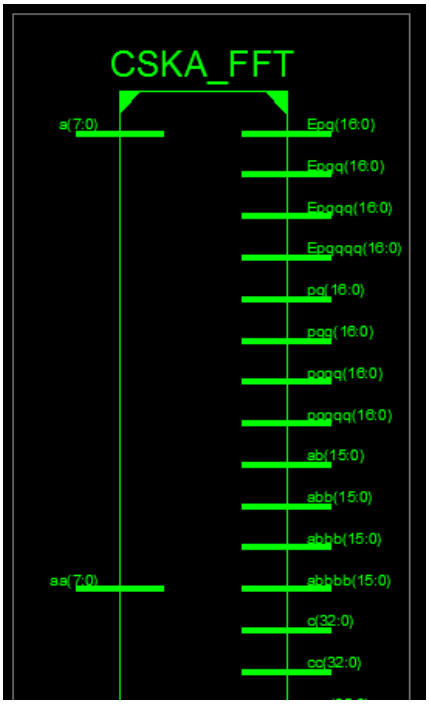

FIG 6. TECHNOLOGY SCHEMATIC DIAGRAM

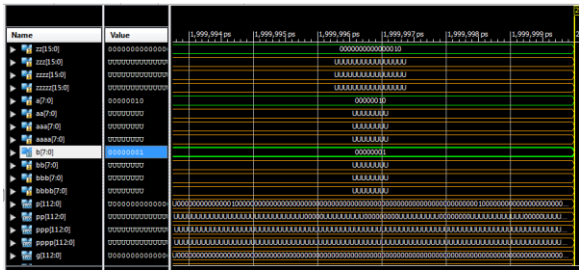

FIG.7 INPUT WAVEFORM OF FFT

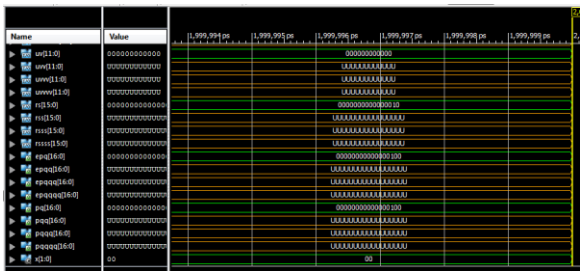

FIG 8 OUTPUT WAVEFORM OF FFT

V.CONCLUSION

The Fast Fourier transformation (FFT) is a frequently used Digital signal processing (DSP) algorithms for the Orthogonal Frequency Division multiplexing (OFDM). The combination of Orthogonal Frequency Division Multiplexing (OFDM) with Multiple Input Multiple Output (MIMO) signal processing is an approach for enhancing the data rates of various communication systems such as Wireless LAN, e Mobile, 4G etc. Since FFT processor is a complex module in OFDM, it is implemented to design the processor in an efficient way. The proposed system is the implementation of a low delay and area efficient N-point pipelined FFT processor using radix-2 algorithm.

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