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Design A High Speed FFT Using SISO-CSKA For Communication

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Abstract: *In this paper we are using an carry skip adder which gives low power consumption and high speed operation. By the both methods of concatenation and incrementaion we can enhance speed by the performance of covetional carry skip adder (CSKA). For the purpose of skip logic the both AND-OR and OR-AND inverter is used. Basically the existed system occupies more area and it is complex. So to overcome that an algorithm is used that is fast fourier transform (FFT) which an efficient algorithm to compute the DFT and inverse DFT. In thye fields of digital vedio and audio broadcasting and wireless LANS fast fourier transform is most widely used. In this paper we are implementing the folding techniques by using radix-2 DIT FFT algorithm. Fro all stages in proposed algorithm we use the radix-2 butterfly stages. From this the propsed algorithm will occupy less area and consumes the delay. By using xilinx software we can implemet these all designs.*

KEY WORDS: CSKA, FFT, DIT-FFT

I.INTRODUCTION

Basically, in signal processing systems we use an efficient method for faster operation that is fast fourier tyransform (FFT). In the orthogonal frequency division multiplexing (OFDM) systems this FFT technique is most widely used. For the purpose of mainipulation of DFT the efficient technique is fast fourier transform. The design of fast fourier transform is proposed by the cooley and tukey. This designs main intent is to decrease trhe number of computations. Coming to hardware implementation, it is done by using two classifications. One is memory architecture and another one is piupeline archirtecture. Coming to the memory architecture, it consists of signal processing element and various units of memory. The memory architecture gives low power and low cost compared to the other architecture. But this memory architecture have some disadvantages that are greater latency and lower throughput.

Now this disadvantages of memory architecture are overcome by using pipeline architecture. There are different types of pipeline architecture they are single delay feed back (SDF), single dealy commutator (SDC) and multiple delay commutator (MDC). This pipeline architecure adopts the hardware description language more fastly. In present generation we need high speed and relaible technology of communication.

So for that purpose we should implement the high speed FFT architectures for better communication compared to the past. Generally FFT blocks are used in the both civil and mechnaical engineering. One of the efficient method to implemet the discrete fourier transform is fast fourier transfrom. Coming to DFT, it has the order O (N log N) operations. Here in this if the architecture is designed with complex inputs then the operation becomes double compared to the design of real inputs.

II. EXISTED SYSTEM

The below figure (1) shows the structure of existed hybrid variable latency CSKA. Here the entire strcuture depends up on the concatenation and incrementation schmes. This existed system is known as conventional carry skip adder which is denoted as CI-CSKA. Now we are repalcing the 2:1 multiplexer by AND-OR and OR-AND compound gates. This gates consists of few transistors and gives low delay and occupier low area.

By using skip logic the carry is propagated. But this method becomes more complicated. To get more easily, complement of carry is generated. Compared to the conventional one this existed system has lower delay. The AOI gates occupy low power consumption compared to the multiplexers. But the existed CI-CSKA architecture consumes meore power compared to the conventional one. This is obtained due to the increase of number of gates.

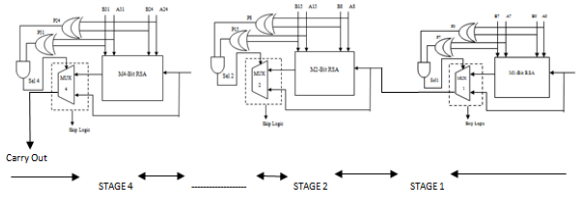

FIG.1. EXISTED SYSTEM

III. PROPOSED SYSTEM

The below figure (2) shows the flow chart of the proposed system. This proposed method is used mainly in binary input. This binary input is transmitting to the serial input serial output (SISO) shift register. From the below flow chart we can say number of elements are use which are given as SISO, carry skip adder (CSKA), adder, subractor, single path delay feedback pipeline and folding architecure. Here the SISO mainy depends upon the binary input. For example the binary input is about 8 word length then in SISO register we use the eight delay flip flops.

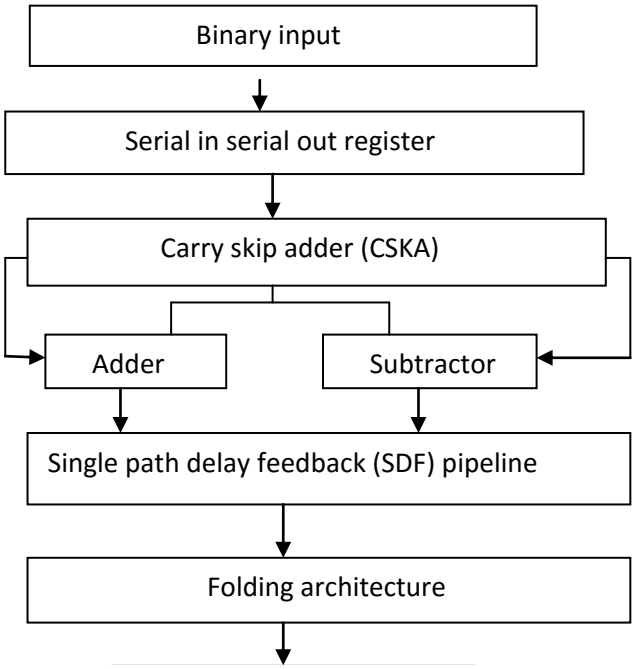

FIG. 2. FLOW CHART OF PROPOSED ALGORITHM

From algorithm we can say that all the AND gates are created by the white cell and all NAND gates are created by the gray cell. Coming to white cell it consists of full adder and AND gate. In the same way gray cell consists of full adder and NAND gate. Upto now we have discussed about the algorithm let us discuss about the multiplication process involved in the proposed system. The below figure (3) shows the block diagram of SIGN multiplication and the below figure (4) shows the block diagram of complex multiplication.

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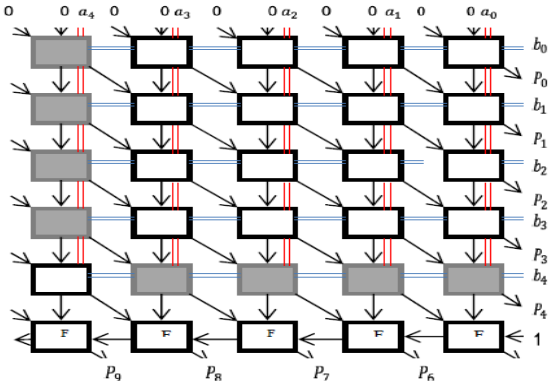
But in complex multiplication consists of 3 multiplications, 1 adder and 1 subraction which can be observed fron figure (4). This is about multiplication, now let us discuss about the subtractor. Basically, subtractors are two types half subtractor and full subtractor. The both full and half subtractors are depend on the word length in the propsed algorithm.



Fig, 3. BLOCK DIAGRAM OF SIGN MULTIPLIER

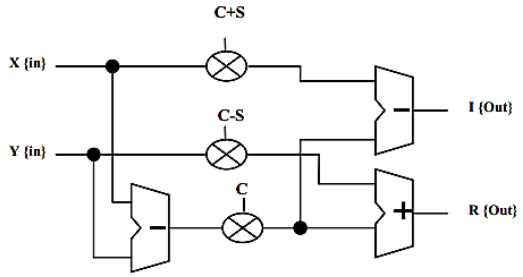


FIG. 4: BLOCK DIAGRAM OF COMPLEX MULTIPLICATION

Coming to single path delay feedback architecture, irt is used to imnimise the number od delay elements. In the proposed architecture the input data is directly send to the butterfly when half of the outputs from each stage are fed back to input data buffer. From figure (5) we can observe the flow grapgh of pipeline architecture.

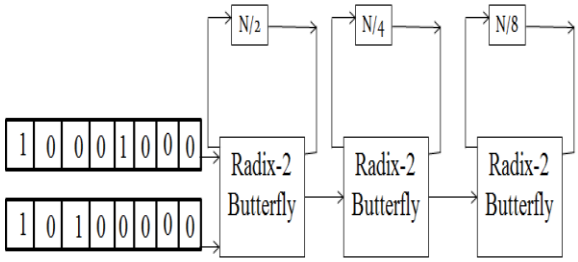


FIGURE 5: FLOW GRAPH OF THE RADIX-2 SDF PIPELINE ARCHITECTURE

IV. RESULTS

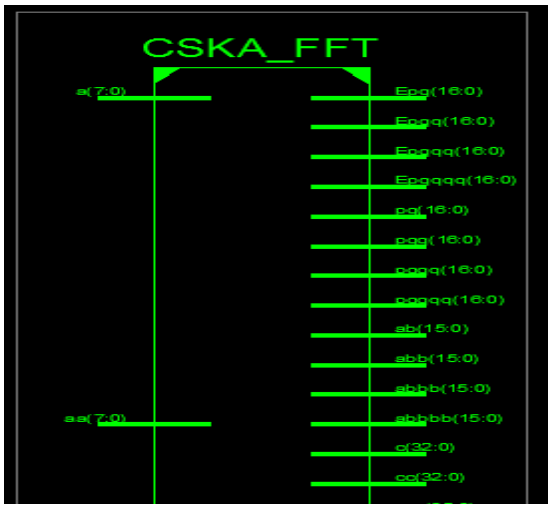


FIG 6. TECHNOLOGY SCHEMATIC DIAGRAM

V. CONCLUSION

Basically, the fast fourier transform is most efficiently used in digital signla processing algorithm for the purpose of orthogonal frequency division multiplexing (OFDM). To enhace the data rates for various communication systems like LAN, 4G,….etc we are combining the orthogonal frequency division multiplexing with multiple input and multiple output processing. Coming to the FFT processor, it is an complex module in OFDM. The main intent of this FFT processor is to design the processor

in an efficient way. At last we can conclude that the proposed system gives lower delay and produces low power consumption.

VI. REFERENCES

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