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Effects of Potential Induced Degradation on Solar PV Module based on temperature and humidity

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ABSTRACT

Due to the increased demand for renewable energy sources, the manufacturing of solar cells and photovoltaic arrays has advanced considerably in recent years. Photovoltaic (PV) is considered to be one of the most committed source of renewable energy technologies after hydro and wind power. PV is one method to generate electrical power by converting the solar radiation into DC voltage by using semiconductors that exercise the photovoltaic effect by using solar panels which composed of number of solar cells containing photovoltaic materials, for example mono-crystalline, poly-crystalline and amorphous silicon as well as cadmium telluride (CdTe) and copper indium gallium selenite/sulfide (CIGS). Till now, nearly 100 countries use photovoltaic as a main source of renewable energy, done by various ways of installation, e.g. on the roof top or walls of buildings or as a power plant string arrays.

This paper is focusing on PID of wafer based standard p-type silicon technologyaiming on increasing life times for solar panels onceexposed to external potentials in the field. A test setup ispresented for simulation of the PID in the lab and theinfluence of cell properties on PID is demonstrated inorder to reveal the cell being the precondition for the PID.However, PID can also be stopped or minimized on paneland system level as shown in the paper.

INTRODUCTION

Solar PV modules are made up of PV cells, which are most commonly manufactured from silicon but other materials are available. Cells can be based on either wafers (manufactured by cutting wafers from a solid ingot block of material) or “thin film” deposition of material over low cost substrates [1]. In general, silicon-based crystalline wafers provide high efficiency solar cells but are relatively costly to manufacture, whereas thin film cells provide a cheaper alternative but are less efficient [2]. Since solar energy generation is getting more and more important worldwide PV systems and solar parks are becoming larger consisting of an increasing number of solar panels being serially interconnected [3]. As a consequence panels are frequently exposed to high relative potentials towards ground causing High Voltage Stress (HVS). The effect of HVS on long term stability of solar panels depending on the leakage current between solar cells and ground has been first addressed by NREL in 2005. This potential degradation mechanism is not monitored by the typical PVS tests [4]. Differences of up to one thousand volts occurbetween the ends of a string. For safety reasons, all metallicframes of the modules have to be grounded at a fixedpotential. This leads to a voltage bias of the individual stringunits with respect to their frames. This bias can cause aleakage current flow between the frame and the solar cells andcan have negative impact on the longtime performance of PVpanels and systems. This degradation mechanism is calledpotential induced degradation (PID)[5].Potential-induced degradation (PID)

can be understood as a designation for aging effects whicharise due to the potential difference between cells and earth. Inthe past, a form of PID which canlead to a decrease in power has been observed for crystalline PV modules, without the modulehaving externally visible damage[3]. Due tothe voltage between cells and earth (frame / front glass cover), positive ions can migrate into the solar cell, for example, reducing the output power. At present, we areinvestigating this effect on live solar panels in the field[4].

EXPERIMENTAL

Potential induced degradation (PID) of crystalline silicon modules, if the cells are on negative potential against ground [4]. Worst case would then be -1000V for grounding thepositive pole of the inverter. High rates of PID were observed when the outer surface of the module became electrically conductive forming the ground electrode against negative cellbias. This effect is caused by surface humidity in real operation and can be simulated in climatic cabinets, by applying wet cloth, or highly conducting layers on the glasspanes (aluminium foils). The high potential causes a leakage current that might be a measure for the degradation rate [5].

EXPERIMENTAL RESULTS

System level

As mentioned before as it has been found in any string array that the effect of PID occurs due to the high voltage of the solar system. It depends on the type of grounding of the frame which determines the potential between cell and frame of a module in a string [6]. Figure 1 shows 20 modules connected in string array. 10 modules are exposed to a positive voltage potential (between cell and frame) and 10 modules to negative voltage potential. It has been found that the most affected p-type solar modules in the above string array are the 10 modules which exposed to the negative potential voltage as shown in figure 2 [6].

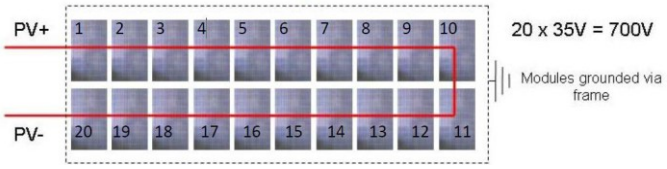

Figure 1: 20 modules string array grounding relative to the frame. [6]

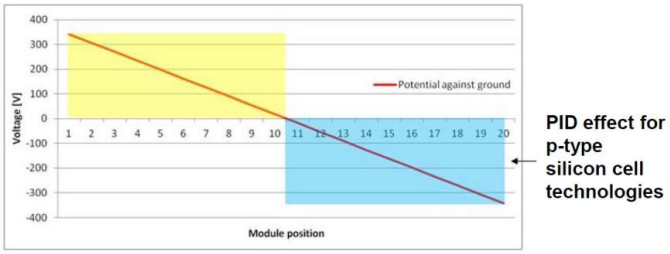

Figure 2: Cell to frame potential showing the PID affected modules. [6]

It has been found that the best way to prevent from PID effect is to avoid the negative potential relative to ground for the p-type standard cells. This could be done by using special inverters using transformers. Since the last few years mainly inverters without transformers were used, this resulted in free floating grounding and a higher risk of PID.

Panel level

Taking a closer look at the PID effect on the panel level as done in case of prone solar cells in a standard panel – see the following EL images before and after the PID test with 1000V for 100hr. First in general the brightness of the picture is decreasing (not visible here) and second single cells are not uniformly affected. Some cells degrade heavily and seem to be short circuited while others appear to be stable. The

reasons for this variation must be investigated on cell level as will be done in the next topic.

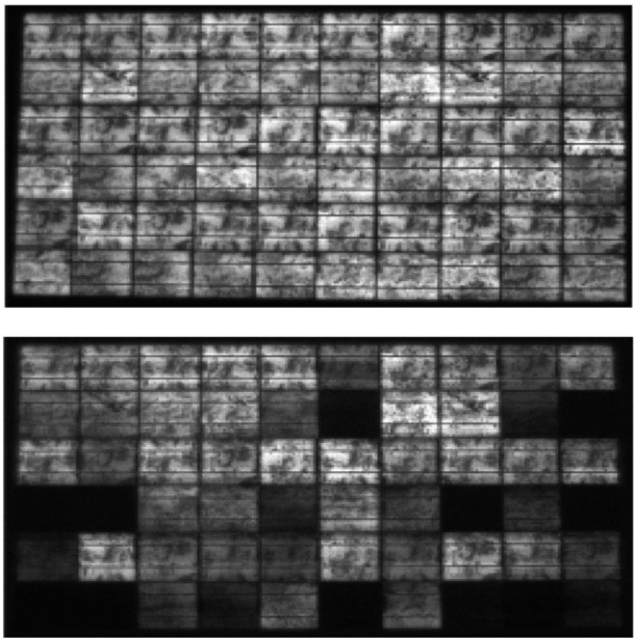

Figure 3: EL image of a panel before (upper) and after(lower) 96 hr 1000V PID test - power loss was 87% [5].

Celllevel

The following two graphs show the evolution of the IV curve with ongoing PID and the corresponding power degradation over time

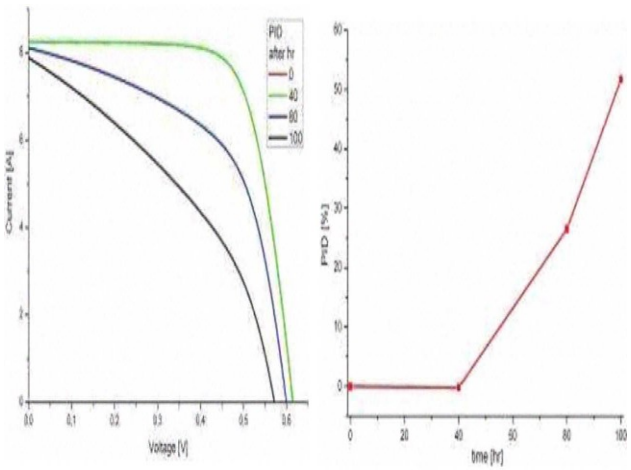

Figure 4: PID IV curve evolution (left) and corresponding power degradation (right). [3]

In case of PID shunt resistance as well as the reverse bias current is affected first followed by FF. Finally Voc decreases reflecting the junction to be less capable ofseparating holes and electrons.

Test methodology adopted:

As per IEC 62804 - System voltage durability qualification test for crystalline silicon modules, One module was tested for PID at below conditions:
Chamber air temperature: 85 ± 2 ˚C
Chamber Humidity: 85 ± 5%
Exposure Time: 96 hours

TABLE 1.1: Maximum Power Determination (Pre PID Test)

Test Date:			12-05-2016			
Irradiance (W/m2)			1000			
Module Serial No	Voc [V]	Vmp [V]	Isc [A]	Imp [A]	Pmp [W]	FF [%]
WS051590000 92124	38.4	29.7	8.678	8.117	241.5	72.5

TABLE 1.2: Insulation test – Initial (Pre PID Test)

Test Date:		12-05-2016
Test Voltage Applied[V]:1000		Time[Sec]:120
WS05159000092124	Measured Value GΩ)	11.25

Potential Induced Degradation Test	**12-05-2016 to 16-05-2016**
Voltage across the terminal & frame……..	1000 V
Chamber Temperature……	85 ± 5 ºC

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Chamber RH (%)…….	85 ± 5 %
Hours of exposure……..	96 Hrs.

Table:1.6	Insulation test (Post PID Test)	
Test Date……		16-05-2016
Test Voltage applied [V]:1000		Time[Sec]:120
WS0515900009212 4	Measured Value(MΩ)	892

TABLE 1.3: Wet leakage current test (Pre PID

Test)

Test Date:		16-05-2016
Test Voltage applied [V]:1000		Time[Sec]:120
WS05159000092124	Measured Value(MΩ)	205

TABLE 1.4: Maximum Power Determination-

(Pre PID Test)

Test Date:	12-05-2016					
Irradiance (W/m2)			1000			
Module Serial No	Voc [V]	Vmp [V]	Isc [A]	Imp [A]	Pmp [W]	FF [%]
WS0515900009 2124	15	7.6 2	7.6 39	4.0 04	30. 5	26. 6

TABLE 1.5: Visual Inspection By – Initial

(Pre Pid Test)

WS051590000 92124	4 Initial Examinatio n	No Visual Defect s	Resul t	Pass

TABLE 1.6: Insulation Test (Post PID Test)

Serial No of Module	Degradation
WS05159000092124	87.3 %

After 96 Hours Total Degradation Observed:

The ISC is the parameter that is least affected but with advancing PID Isc also degrades. Depending on the degree of PID the junction is losing its blocking characteristic under reverse bias or totally breaks down(ohmic shunt).This phenomenon can be visualized by EL images taken during a PID test that are shown in the upper row. After 40hr local shunts appear along the edge of the cell that degrade further from diode to ohmic behaviour, as can be seen in the reverse bias image in the lower row. First shunted areas appear bright but afterfurther PID evolution these areas do not emit any more breakdown light [10]. Finally after 100hr both images are dark because of dominating ohmic shunts.

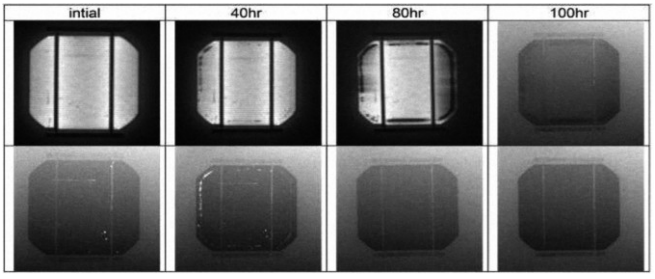

Figure 5: EL image of a cell during PIO test (upper row) and reverse bias (-12V) image (lower row).[7]

The leakage current in form of electrons or ions is resulting in an increased charge concentration above the solar cell in the ENG. These charges interact with theemitter and depletion layer and disrupt their function. Fromsemiconductor

industry similar effects are known as (timedependent) dielectric breakdown or surface inversion [8].The electric field of these charge carriers is influencing the p-n junction in that way that junction gets more conductiveand the local shunt resistance drops. Sunpower applied atransistor model to the polarization effect [9] on their ntype back contact cell. In the case of standard p-type cellsthis model also works but the configuration needs to be switched from npn- to pnp-transistor. There are numerous factors on cell level being important in respect to PID. In the following we present theparameters identified to have a significant impact [13].

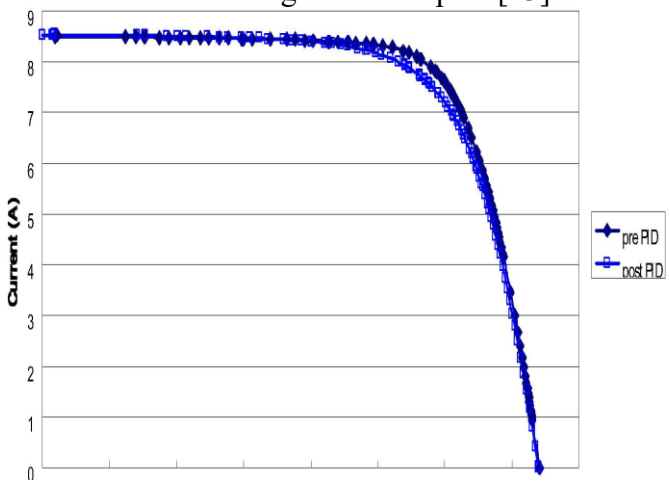

Figure 6: IV curve pre PID and post PID test.[14]

CONCLUSION

This paper presented a degradation mechanism called Potential Induced Degradation (PID) that is getting moreimportant with growing PV system sizes going along with higher system voltages. It was shown that - although the origin of PID is on cell level - it can be minimized or avoided on all levels - system, panel and cell. The solution on system level is choosing an appropriate grounding scheme of the string poles while on panel levelthe properties of the encapsulation material determine the height of leakage currents that can in case of prone solar cells lead to PID. On cell level many parameters influence the PID stability of solar cells. Besides base material resistivity and emittersheet resistance the most important parameter was found to be the anti-reflective coating since adaption of this layer can avoid the effect of PID. The PID effect can be reversed by switching the polarity and also high temperatures support regeneration. Also use of PV offset box or a galvanically isolating inverter and a negative earthing set is highly effective to overcome PID. Taking these findings into account long term stability of solar panels can be significantly improved by adapting processes on all levels in order to minimize PID andtherefore optimize the energy output of the PV systemover a 25+ year life time.

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