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Design a Cryptography Algorithm Using Shiftrow Mixcolun Technique

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ABSTRACT–One of the most efficient system in encryption is public key encryption system. This public key encryption method is based on the Rijndae algorithm. The main intent of this algorithm is to create faster and efficient cryptographic keys. At first to generate the AES keys we use the conventional method but for faster operation we use Rijnadel algorithm properties. generation of AES keys are obtained from the properties of Rijndael algorithm. By using the xilinx software many number of encryption algorithms are implemented for the purpose of cryptographic processors. The proposed technique provides high security compared to existed technique.

Keywords: Cryptography, Rijndael, Encryption, Decryption, Cypher, Inverse cypher.

I.INTRODUCTION

Several techniques, such as cryptography, steganography, watermarking, and scrambling, have been developed to keep data secure, private, and copyright protected [1], [2]. Cryptography is an essential tool underlying virtually all networking and computer protection, traditionally used for military and espionage. However, the need for secure transactions in ecommerce, private networks, and secure messaging has moved encryption into the commercial realm [3].

Advanced encryption standard (AES) was issued as Federal Information Processing Standards (FIPS) by National Institute of Standards and Technology (NIST) as a successor to data encryption standard (DES) algorithms. In recent literature, a number of architectures for the VLSI implementation of AES Rijndael algorithm are reported [4], [5], [6], [7], [8]. It can be observed that some of these architectures are of low performance and some provide low throughput. Further, many of the architectures are not area efficient and can result in higher cost when implemented in silicon.

In this paper, we propose a high performance, high throughput and area efficient VLSI architecture for Rijndeal algorithm that is suitable for low cost silicon implementation. The proposed architecture is optimized for high throughput in terms of the encryption and decryption data rates using pipelining. Polynomial multiplication is implemented using XOR operation instead of using multipliers to decrease the hardware complexity. In the proposed architecture both the encryption and decryption modes use common hardware resources, thus making the design area efficient. Selective use of look-up tables and combinational logic further enhances the architecture's memory optimization, area, and performance. An important feature of our proposed architecture is an effective solution of online (real-time) round key generation needing significantly less storage for buffering.

II.EXISTED SYSTEM

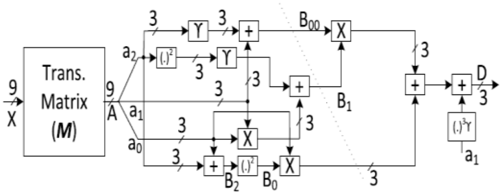

FIG. 1 EXISTED SYSTEM

The substitution box is part of a unit in Pomaranch cipher which implements a key-dependent filter function, containing a 9-to-7-bit box and a balanced nonlinear Boolean functionof seven variables. The 9-bit output of the substitution box isconverted into a 7-bit one with deletion of the most significant and the least significant bits, as shown in Fig 1.

The operations are done in composite fields to achieve the inverse which is then retransformed tobinary field using an inverse transformation matrix (*M*–1).Eventually, the two most and least significant bits are discardedto get to the uneven structure of the substitution box of Pomaranch.

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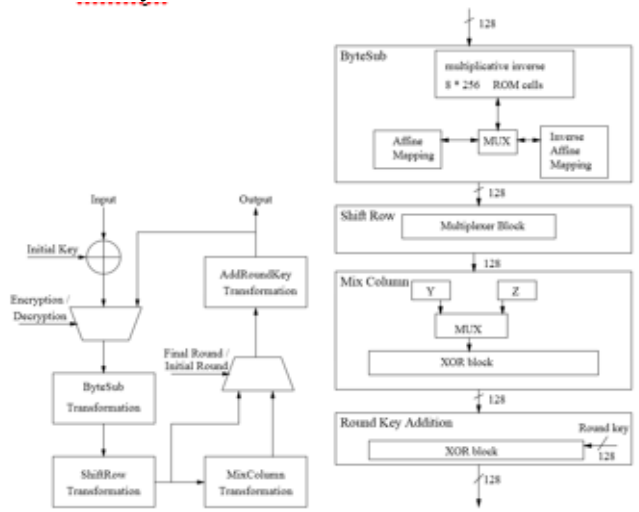
III.PROPOSED SYSTEM

The data unit consists of: the initial round of key addition, $N_r - 1$ standard rounds, and a final round. The architecture for a standard round composed of four basic blocks is shown in Fig. 1(b). For each block, both the transformation and the inverse transformation needed for encryption and decryption, respectively are performed using the same hardware resources. This implementation generates one set of subkey and reuses it for calculating all other subkeys in real-time.



(a) Rijndael Algorithm Data and Con- (b) Architecture for the Standarc

Fig. 2. Top Level View of the Rijndael

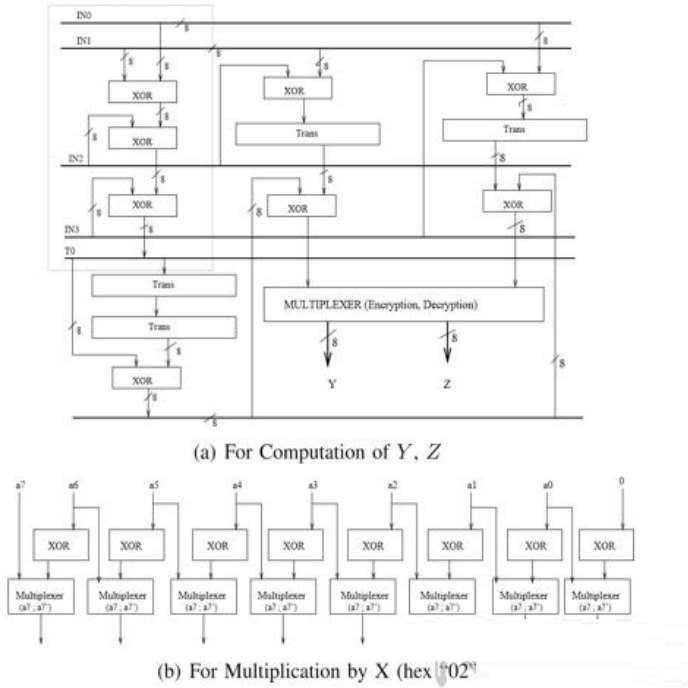
1) ByteSub: In this architecture each block is replaced by its substitution in an S-Box table consisting of the multiplicative inverse of each byte of the block state in the finite field $GF(2^8)$. In order to overcome the performance bottleneck,control Flow Round in the Data Unitthe implementation of multiplicative inverses is carried out using look-up tables (stored in a table of 8 × 256). The implementation includes the affine mapping of the input in both encryption and decryption processes as follows:

2) ShiftRow: In this transformation the rows of the block state are shifted over different offsets. The amount of shifts is determined by the block length. The proposed architecture implements the shift row operation using combinational logic considering the offset by which a row should be shifted.

3) MixColumn: In this transformation each column of the block state is considered as a polynomial over $GF(2^8)$. It is multiplied with a constant polynomial $C(x)$ or $D(x)$ over a finite field in encryption or decryption, respectively. In hardware, the multiplication by the corresponding polynomial is done by XOR operations and multiplication of a block by X. This is implemented using a multiplexer, the control being the MSB is 1 or 0. The equations implemented in hardware for *MixColumn* in encryption and decryption are as follows.

In encryption process,

*In*0 is the least significant 8 bits of a column of a matrix. Architecture of different units are shown in Fig. 2 and the architecture of *MixColumn* transformation is shown in the Fig. 3.



(a) For Computation of Y, Z

(b) For Multiplication by X (hex [illegible]02)

Fig. 3. Architecture for Units used in Mix Column Transformation

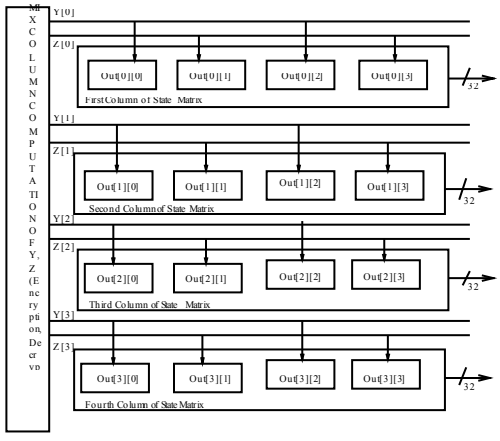


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Fig. 4. Architecture for Mix Column Transformation for 128 bits

4) AddRoundKey: In this transformation (architecture represented in Fig. 4), the round key obtained from the key scheduler is XORed with the block state obtained from the *MixColumn* transformation or *ShiftRow* transformation based on the type of round being implemented. In the standard round, the round key is XORed with the output obtained from the *MixColumn* transformation. In the final round the round key is XORed with the output obtained from the *ShiftRow* transformation. In the initial round, bitwise XOR operation is performed between the initial round key and the initial state block.

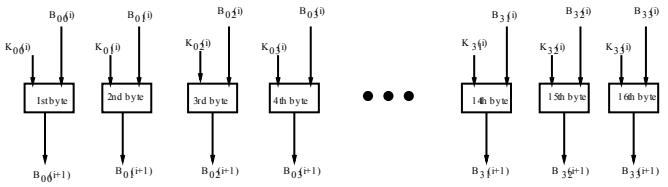


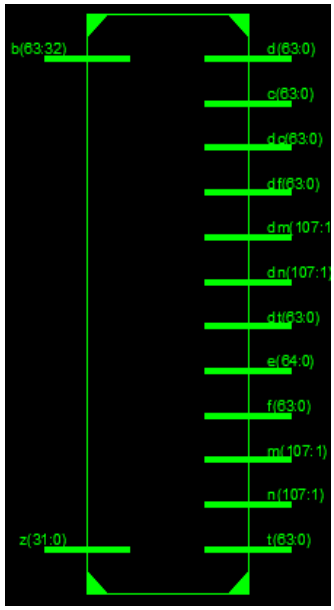
Fig. 5 Architecture for Round Key Addition Transformation

B. Memory Optimization

Since the design is based on one clock cycle for each encryption round, the memory modules had to be duplicated. For example, in the *ByteSub*, the S-boxes need to be duplicated 16 times. Consequently, the choice of memory architecture is very critical. Since all the table entries are fixed and defined in the standard, the usage of ROM is preferred. Specifically, the architecture requires several small ROM modules instead of one large module, since each lookup will only be based on a maximum of 8-bit address, which translates to 256 entries. We implemented the multiplicative inverse function using the look-up table of size 8×256. We have a total of 20 copies of the S-boxes in our design; 16 of them in encryption module and 4 in the key scheduling module.

D. Performance Evaluation

An AES-128 encryption / decryption of a 128-bit block was done in 11 clock cycles using the feedback logic. In each clock cycle, one transformation is executed and, at the same time, the appropriate key for the next round is calculated. The whole process concludes after 10 rounds of transformations. The outputs is shown in below figure 5 RTL and waveform.



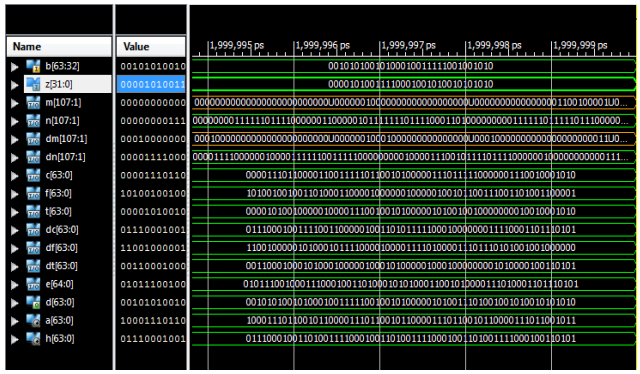


Fig.6RTL, output wave form

IV. DISCUSSIONS AND CONCLUSIONS

To perform the both operations of encryption and decryption in VLSI architecture we proposed an algorithm that is Rijndael AES algorithm. To implement the multiplicative inverses between encryption and decryption we use S-boxes. As discussed earlier that round keys are used for implementation of each round which is generated in real time. Forward and reverse scheduling is implemented on the device to minimise the area. But here the encryption algorithm is less complex when compared to decryption algorithm.

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