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Design an Efficient Architecture of Fft-Based On Cska

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Abstract: *In this we are going to discuss about the structure of carry skip adder (CSKA) which performs the operation with high speed and low energy consumption. By using the both concatenation and increment techniques we can increase the efficiency of carry skip adder. For the purpose of skip logic we use the AND-OR and OR-AND inverter gates.The realization of carry skip adder circuit is done by using two styles, one is fixed stage size style and another is variable stage size style. By adding a hybrid variable latency extension to the proposed structure we can reduce the power consumption and as well as speed also increases. In the same way to increase the slack time we usea modified parallel structure. Now to detect and correct the errors we use the fault tolerant method. One of the main examples of this fault tolerant method is fast Fourier transform (FFT). At last fault tolerant parallel FFT efficiency is increased by protecting the FFTS (.i.e) FFT using CSKA.*

Key Words: Fast Fourier Transform (FFT), AND-OR-INVERT (AOI), OR-AND-INVERT (OAI), CSKA.

I. INTRODUCTION

In arithmetic and logical units (ALUs) we use adders for the purpose of high speed operations and low power consumption. In general purpose processors it is difficult to perform high speed operations and low power consumptions. To reduce the power consumption one of the effective Technique is sub threshold current which is occurred due to the quadratic dependence of switching energy. Based on the reduction of supply voltage it decides in which region it should be. The regions are subthreshold region, super threshold region and near threshold region.Sub threshold region gives lower delay and high switching and leakage powers compared to both of near and sub threshold voltage.

Coming to the sub threshold voltage the logic gate delay and leakage power will exhibit exponential dependence on supply voltage and threshold voltage. In sub threshold regionthe small sub threshold current causes a large delay for the circuits operating. Next one is near threshold region which provides the desirable trade off point between delay and power dissipation when compared to the sub threshold. Lower switching and leakage powers are obtained when compared to the super threshold region.

For designing the circuits power depends upon the dynamic voltage and frequency scaling factors. To reduce the power consumption the system should change voltage depends upon the requirement. For this type of systems operates with wide range of supply voltages. So to get lower power consumption and high speed operations adders are used which is the basic block in the systems. Depend on the supply voltage the adder's gives specified response.

Basically, many types of adders are used in delays, power consumptions and areas. Examples of adders are given as ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). Let us discus each adder in detail manner… Coming to the RCA, it is a simplest structure which occupies small area and power consumption but with worst critical path delay. Compared to RCA, the CSLA gives large area, speed and power consumption. Next one is PPAs which is also called as carry look ahead adders. In these PPAs they use directly parallel prefix structures to generate the carry as early as possible.

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Next one is CSKA which is an efficient method because it occupies low area & power consumption and produces high speed operations. We use CMOS technology for the protection as well as for faster calculations. This CMOS technology will enables the integration of transistors on single device. Here soft errors will be obtained and different techniques are proposed to verify the soft errors. First proposed technique is SOS with FFTs to detect and correct the errors. But this does not gives perfect output. So now a new proposed structure is introduced that is given as parseval-SOS-ECC technique. In this proposed technique, the main purpose of the ECC is to correct the errors and in the same way the main purpose of SOS is to detect the errors. From the below sections we can observe the existed system which is shown in figure (1) and the proposed system is shown in figure (2). The results are shown below

II. EXISTED SYSTEM

The below figure (1) shows the existed conventional carry skip adder structure. The main intent of this existed system is to reduce the delay of skip logic in conventional CSKA structure. Generally, the conventional structure is denoted as CL-CSKA. Here we use the both the concatenation and the incrementation schemes. The both concatenation and incrementation schemes gives ability to use the simple carry skip logics.

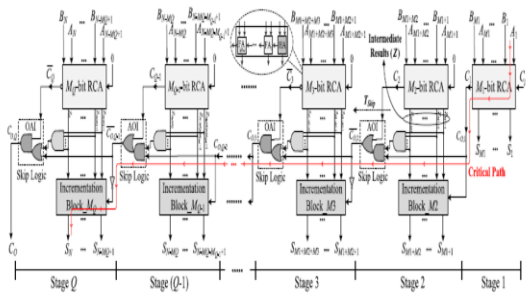

Fig. 1. Existed CI-CSKA structure

is

compound gates. These gates provide the low area delay and low power consumption. Here the carry propagates through the skip logic and gets complemented in the existed structure. After propagation at the output the complement carry is generated. This is about the operation involved in the existed structure, now let us discuss about the internal structure of existed system.

From figure (1) we can say that there are two N bits inputs, A and B and Q stages. Each stage in the structure consists of RCA block which is also known as the first block having size M_j. This RCA block gives the output as the summation of N input bits. Coming to the other blocks, it gives intermediate results. This is about the first block and coming to the second block, it consists two blocks of RCA and incrementation. Here the intermediate block gives the incrementation block. This is about the existed system, now let us discuss about the proposed system in detail.

III. PROPOSED SYSTEM

The below figure (2) shows the architecture of proposed system. In the proposed architecture we use two modules and it performs fast opeartions without zero padding. As shown in below figure (2) there are multiple adders, riplle carry adder, FFT, shift module and control unit. All these componenets combine together and gives an specified output,

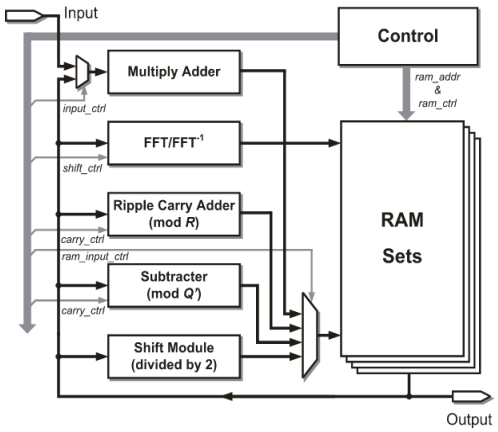

Fig. 2. Proposed system

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In this proposed sytem, for the purpose of modular reduction and conditional sequences we are using number of muliple opeartions units. Here the pipeline architectures are designed inside the each unit and the entire operation is performed sequentially.Next coming to the block of FFT/ FFT^{-1}, it performs the forward and inverse NWTs. In multiple adder unit, the component wise multiplication and addition operatiions are performed. Now for time domian operations we are using ripple carry adder, subractor and shift module units. Control uniit is used to generate the control signals in the system. Coming to RAM, it consists of several RAM sets which stores the precomputed data and intermidiate rresults.

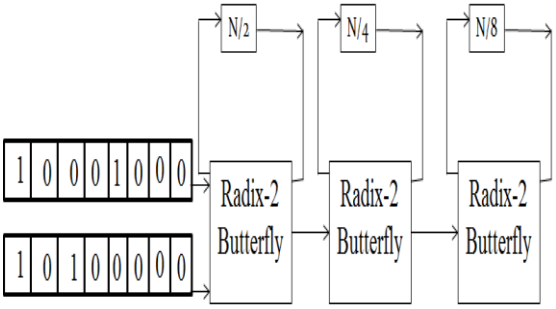

Figure 3: Flow Graph of the Radix-2 SDF Pipeline Architecture

The above figure (3) shows the flow graph of the Radix-2 SDF pipeline architecture. Subtractor:- Subtractor is consist of half subtractor and full subtractor depends on word length in algorithm. Single-path Delay Feedback Pipeline Architecture:- Herbert L. Groginsky and George A. Works introduced a feedback mechanism in order to minimize the number of delay elements. In the proposed architecture one half of outputs from each stage are fed back to the input data buffer when the input data are directly sent to the butterfly.

V. RESULTS

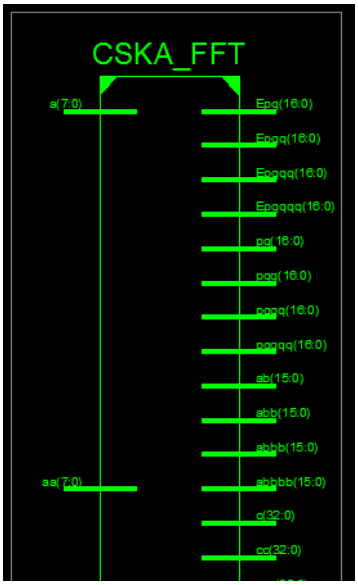

Fig 4. Technology Schematic Diagram

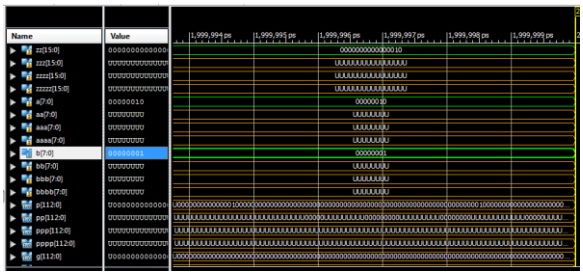

Fig.5 Input Waveform Of FFT

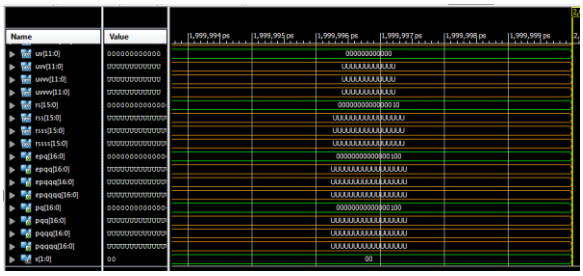

Fig 6 Output Waveform Of FFT

V. CONCLUSION

By using carry skip adder the speed of operation has increased and occupies low area which is shown above from the existed and proposed system. Different techniques are used to perform high speed operations but here by incrementation and concatenation techniques we can get better

results. For the purpose of correcting and detecting errors, we proposed a technique that is parsevals- SOS- ECC which is an efficient technique. By this technique we can detect and correct the errors for speed operation. The SOS is used to detect and locate the errors and in the same wayECC is used to correct the errors. At last we can conclude that the proposed system will detect and correct the errors and gives high speed operation.

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