

# Design and Implementation of a Novel Multilevel DC-AC Inverter

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**Abstract-** *In this paper, a novel multilevel inverter for nine level application is proposed. The proposed multilevel inverter generates level ac output voltage with the appropriate gate signals' design. Also, the low-pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multilevel inverter. Multilevel inverter (MLI) plays a vital role in the field of power electronics and being widely used in many industrial and commercial applications. Moreover the advantages like high quality power output, low switching losses, low electro-magnetic interference (EMI) and high output voltage made multilevel inverter as a powerful solution converter topology. The multilevel inverter topology is the proper option from the point of view of modularity and simplicity of control. Main disadvantage of multilevel configuration is increase in number of power semiconductor switches and its complexity to design gate driver circuit individually, its cost and switching losses. Complexity of the induction motor system reduces reliability of the inverter. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary multilevel inverter. Voltage source converters are also required for various industrial applications, smart induction motor drive applications etc. Due to high power requirement in these applications, using one power semiconductor switch directly is not advisable. For high power and medium voltage applications multilevel converters are introduced.*

**Keywords:** DC-AC inverter, digital signal processor (DSP), maximum power point tracking (MPPT), multilevel.

## 1.INTRODUCTION

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters

include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac systems. A half-bridge is the simplest topology, which is used to produce a two level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter

structures are the main focus of discussion in this chapter; however, the illustrated structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections. The purpose of the multilevel topology is to reduce the voltage rating of the power switch. Therefore, it usually is used at high-power application. By combining output voltages in multilevel form, it has advantages of low  $dv/dt$ , low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years [7], [8].

A digital signal processor (DSP) is a specialized microprocessor (or a SIP block), with its architecture optimized for the operational needs of digital signal processing. The goal of DSPs is usually to measure, filter and/or compress continuous real-world analog signals. Most general-purpose microprocessors can also execute digital signal processing algorithms successfully, but dedicated DSPs usually have better power efficiency thus they are more suitable in portable devices such as mobile phones because of power consumption constraints. DSPs often use special memory architectures that are able to fetch multiple data and/or instructions at the same time. Digital signal processing algorithms typically require a large number of mathematical operations to be performed quickly and repeatedly on a series of data samples. Signals (perhaps from audio or video sensors) are constantly converted from analog to digital, manipulated digitally, and then converted back to analog form. Many DSP applications have constraints on latency; that is, for the system to work, the DSP operation must be completed within some fixed time, and deferred (or batch) processing is not viable.

## II. POWER STAGE

### A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors  $C_1$ ,  $C_2$ , and  $C_3$ . The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is sent to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design.

### B. Operating Principles

1) The required seven voltage output levels ( $\pm 1/3V_{dc}$ ,  $\pm 2/3V_{dc}$ ,  $\pm V_{dc}$ , 0) are generated as follows.

1) To generate a voltage level  $V_0 = 1/3V_{dc}$ ,  $S_1$  is turned on at the positive half cycle. Energy is provided by the capacitor  $C_1$  and the voltage across H-bridge is  $1/3V_{dc}$ .  $S_5$  and  $S_8$  are turned on, and the voltage applied to the load terminals is  $1/3V_{dc}$ . Fig. 3 shows the current path at this mode.

2) To generate a voltage level  $V_0 = 2/3V_{dc}$ ,  $S_1$  and  $S_4$  are turned on. Energy is provided by the capacitor  $C_1$  and  $C_2$ . The voltage across H-bridge is  $2/3V_{dc}$ .  $S_5$  and  $S_8$  are turned on, and the voltage applied to the load terminals is  $2/3V_{dc}$ . Fig. 4 shows the current path at this mode.

3) To generate a voltage level  $V_0 = V_{dc}$ ,  $S_1$  and  $S_2$  are turned on. Energy is provided by the capacitor  $C_1$ ,  $C_2$ , and  $C_3$ .

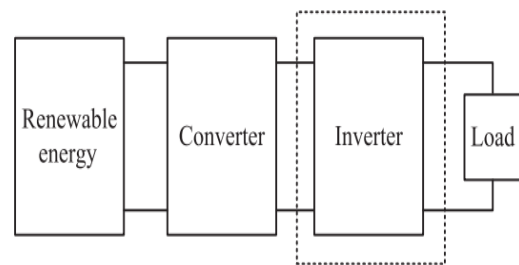


Fig. 1. Block diagram of renewable system.

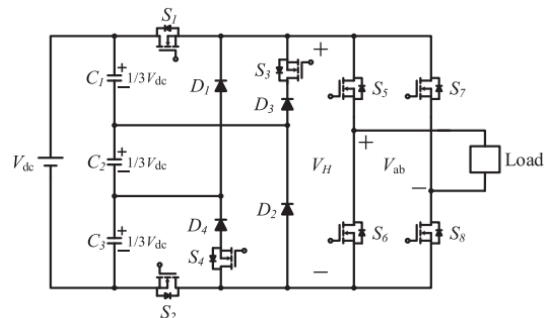


Fig. 2. Proposed seven-level inverter topology

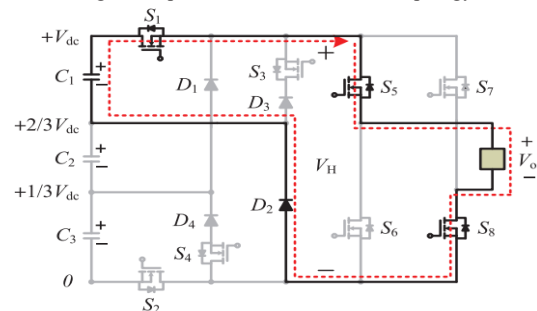


Fig. 3. Switching combination of output voltage level  $1/3V_{dc}$ .

The voltage across H-bridge is  $V_{dc}$ .  $S_5$  and  $S_8$  are turned on, and the voltage applied to the load terminals is  $V_{dc}$ . Fig. 5 shows the current path at this mode.

4) To generate a voltage level  $V_0 = -1/3V_{dc}$ ,  $S_2$  is turned on at the negative half cycle. Energy is provided by the capacitor  $C_3$ , and the voltage across H-bridge is  $1/3V_{dc}$ .  $S_6$

and  $S_7$  are turned on, and the voltage applied to the load terminals is  $-1/3V_{dc}$ . Fig. 6 shows the current path at this mode.

5) To generate a voltage level  $V_o = -2/3V_{dc}$ ,  $S_2$  and  $S_3$  are turned on. Energy is provided by the capacitor  $C_2$  and  $C_3$ . The voltage across H-bridge is  $2/3V_{dc}$ .  $S_6$  and  $S_7$  are turned on, and the voltage applied to the load terminals is  $-2/3V_{dc}$ . Fig. 7 shows the current path at this mode.

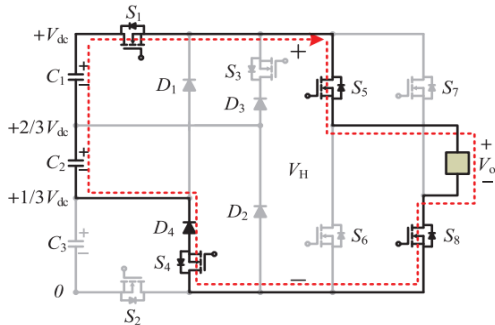


Fig. 4. Switching combination of output voltage level  $2/3V_{dc}$

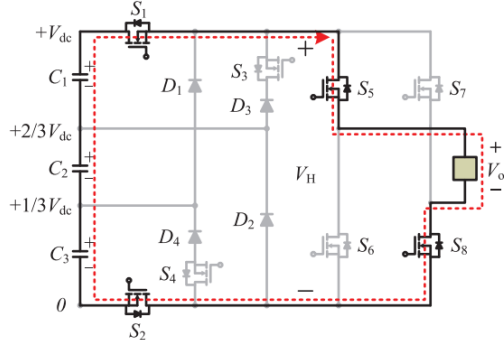


Fig. 5. Switching combination of output voltage level  $V_{dc}$ .

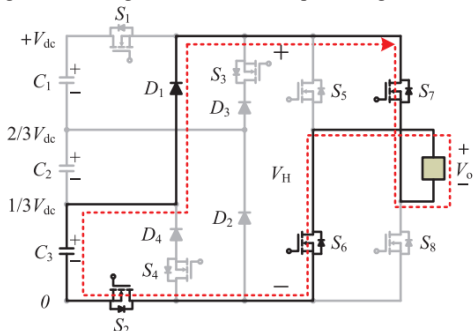


Fig. 6. Switching combination of output voltage level  $-1/3V_{dc}$ .

6) To generate a voltage level  $V_o = -V_{dc}$ ,  $S_1$  and  $S_2$  are turned on. Energy is provided by the capacitor  $C_1, C_2$ , and  $C_3$ , the voltage across H-bridge is  $V_{dc}$ .  $S_6$  and  $S_7$  is turned on, the voltage applied to the load terminals is  $-V_{dc}$ . Fig. 8 shows the current path at this mode.

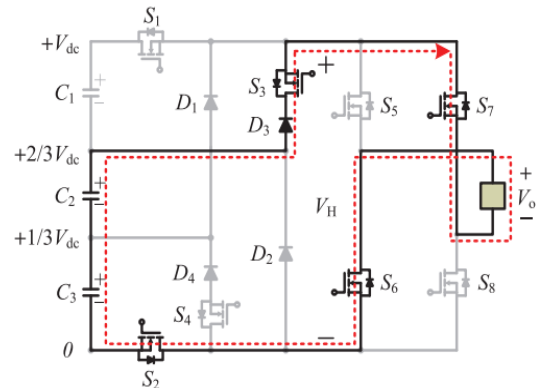


Fig. 7. Switching combination of output voltage level  $-2/3V_{dc}$ .

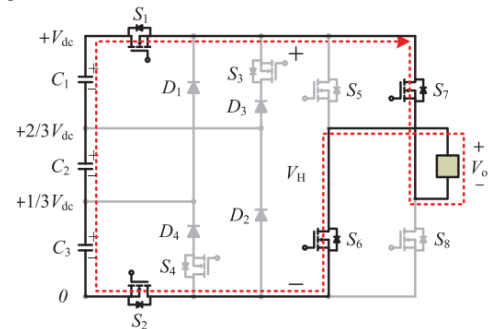


Fig. 8. Switching combination of output voltage level  $-V_{dc}$ .

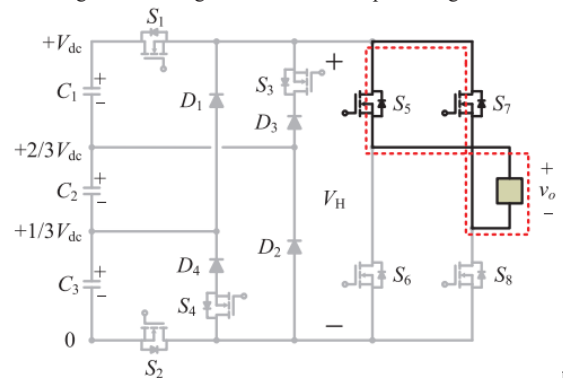


Fig. 9.

Switching combination of output voltage level 0.

7) To generate a voltage level  $V_o = 0$ ,  $S_5$  and  $S_7$  are turned on. The voltage applied to the load terminals is zero. Fig. 9 shows the current path at this mode. Table I lists the switching combinations at different output levels

### C. Topology Comparison

Table II presents the number of components required to implement a seven-level inverter using the proposed topology

TABLE I  
SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

Output voltage $V_o$	Switching combinations							
	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
$V_{dc}$	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II  
COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III  
VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	$V_o$	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	$V_o$	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

and three previously ones [9], [10] that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multicell inverter.

Table II shows that the new topology achieves the reduction in the number of power devices. Table III shows the voltage stress comparison between different type inverters.

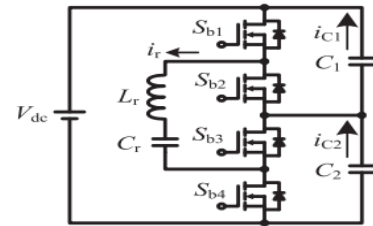


Fig. 10. Circuit configuration of RSCC

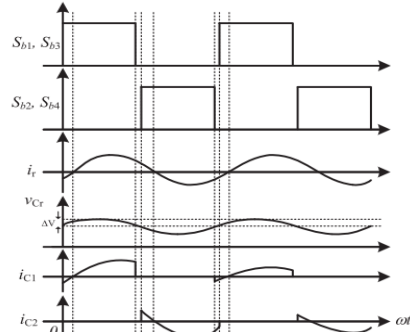


Fig. 11. Waveforms of RSCC.

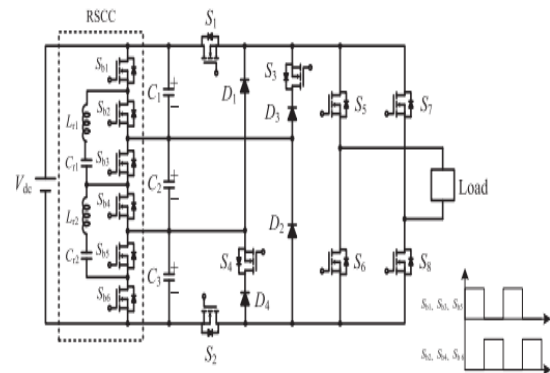


Fig. 12. Proposed multilevel inverter with RSCC.

### III. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage-balancing circuits are indispensable for the capacitors in the multilevel inverters [11]–[15]. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of the resonant switched-capacitor converter (RSCC). The duty cycle of every switch is equal to 50%. The voltage of  $C_1$  is higher than the voltage of  $C_2$ . Since the average current of  $C_1$  is higher than that of  $C_2$  at one switching cycle, most of the charges flow from  $C_1$  to  $C_2$ . After few switching cycles, the voltages of  $C_1$  and  $C_2$  are equal. Fig. 11 shows the waveforms of the RSCC. Fig. 12 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level

configuration, two switches  $S_{b5}$  and  $S_{b6}$ , resonant inductor  $L_r$ , and resonant capacitor  $C_r$  are added. In this application, switches  $S_{b1}$ ,  $S_{b3}$ , and  $S_{b5}$  are turned on at the same time;  $S_{b2}$ ,  $S_{b4}$ , and

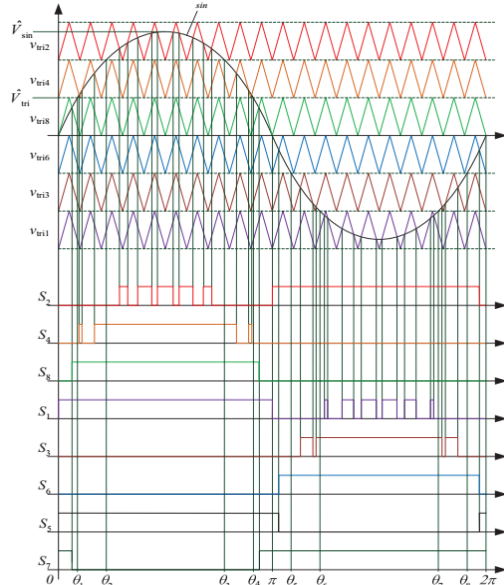


Fig. 13. Reference sine wave, carriers, and control signals of switches

$S_{b6}$  are turned on at the same time. The duty of each switch is equal to 50%.

#### IV. APPLICATION OF SPWM

In this paper, several triangular carriers are distributed by phase disposition technique. The advantage of phase disposition technique is uncomplicated to realize and less total harmonic distortion [16], [17]. These carriers are compared with a reference sine waveform  $v_{sin}$  to get signal of switches. The peak-to-peak value of triangular carrier is  $\hat{V}_{tri}$ . The frequency of carrier is switching frequency of inverter. The peak value of reference sine wave is  $\hat{V}_{sin}$ , and the modulation index  $m_A$  is defined as

$$m_A = \frac{\hat{V}_{sin}}{3 \cdot \hat{V}_{tri}} \quad (1)$$

According to (1), the relationship between the peak value of output sine wave and  $m_A$  can be expressed as

$$V_o = m_A \cdot V_{dc} \quad (2)$$

Fig. 13 shows the reference sine wave, carriers, and control signals of switches.

The method that determines switch signals in Fig. 12 is as follows.

- 1)  $v_{sin} < 0$  and  $v_{sin} > v_{tri2} \rightarrow S_2$  are turned on
- 2)  $v_{sin} > v_{tri4} \rightarrow S_4$  is turned on.
- 3)  $v_{sin} < v_{tri8} \rightarrow S_7$  is turned on.
- 4)  $v_{sin} > v_{tri8} \rightarrow S_8$  is turned on.

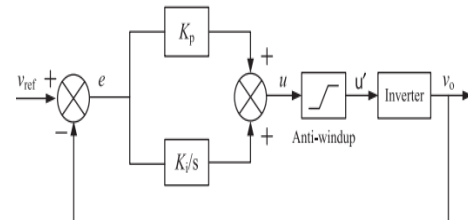


Fig. 14. Block diagram of PI control

- 5)  $v_{sin} > 0$  and  $v_{sin} < v_{tri1} \rightarrow S_1$  are turned on.
- 6)  $v_{sin} < v_{tri3} \rightarrow S_3$  is turned on.
- 7)  $v_{sin} > v_{tri6} \rightarrow S_5$  is turned on.
- 8)  $v_{sin} < v_{tri6} \rightarrow S_6$  is turned on.

#### IV. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in  $S$  domain as

$$u(s) = \left[ K_p + \frac{K_i}{s} \right] e(s) \quad (3)$$

From (3), the equation can be transformed in the  $Z$  domain as

$$u(z) = \left[ K_p + \frac{K_i}{1 - z^{-1}} \right] e(z) \quad (4)$$

Then, transform (4) becomes a difference equation is expressed as

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad (5)$$

Fig. 15 shows system configuration and control block. System detects output voltage first and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver.

The main idea of modified SPWM is to record the previous error of output voltage and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows the schematic of modified SPWM.

$V_{ref}[n]$  is defined as the reference output voltage,  $V_o[n]$  is the feedback of output voltage, and  $e[n]$  is error between

reference output and feedback output which is expressed as

$$e[n] = v_{ref}[n] - v_o[n]. \quad (6)$$

Let  $K_1 = K_p + K_i$ ,  $K_2 = K_p$  then  $e[n]$  is multiplied by  $K_1$  and  $e[n - 300]$  multiplied by  $K_2$ . Then, add the previous output signal  $u[n - 300]$ . Finally, it can obtain the output of PI controller after the process by the anti-windup.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n - 300] + u'[n - 300]. \quad (7)$$

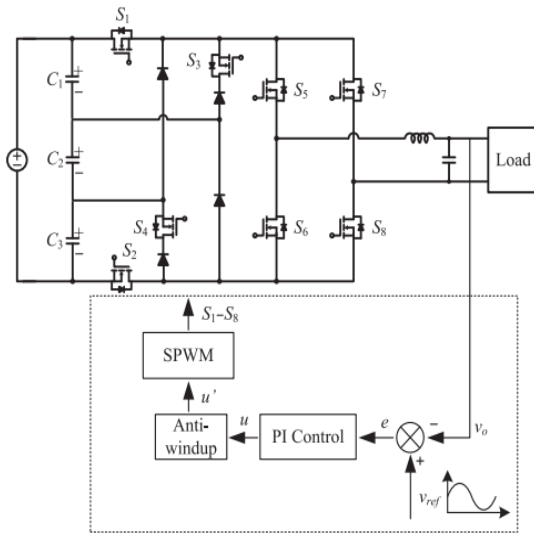


Fig. 15. Seven-level inverter with control algorithm.

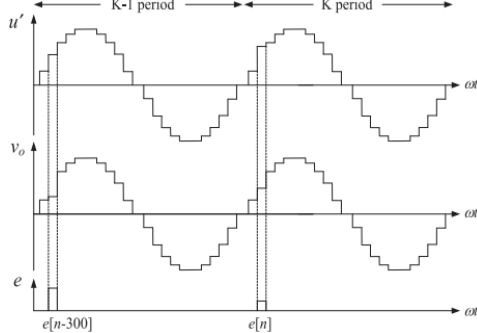


Fig. 16. Schematic of modified SPWM

TABLE IV  
SPECIFICATIONS OF THE PROPOSED INVERTER

Input voltage $V_{dc}$	400 V
Output voltage $V_o$	220 V <sub>rms</sub>
Rated output power $P_o$	2 kW
Switching frequency $f_s$	18 kHz

## V.SIMULATION RESULTS

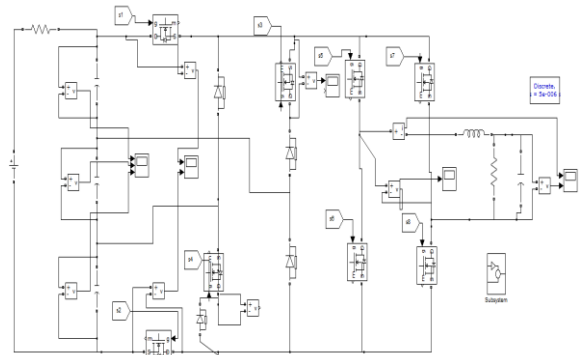


Fig.17.Simulink model of proposed seven level multilevel inverter

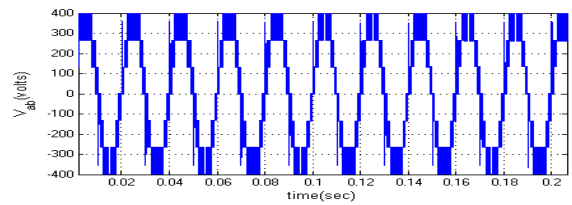


Fig.18.waveform of Vab

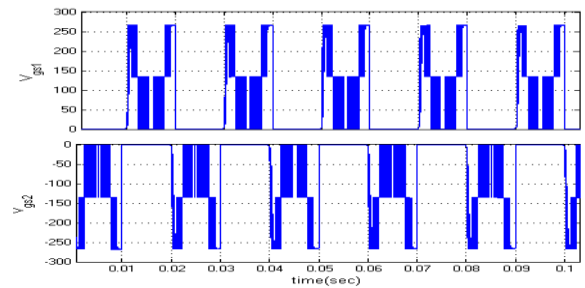


Fig.19.wave forms of Vgs1, Vgs2.

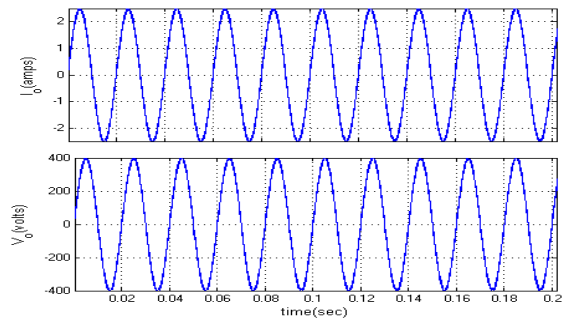


Fig.20.out put voltage and current

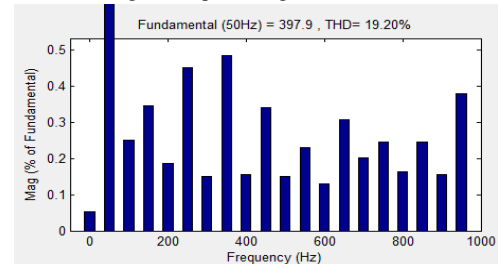


Fig.21. THD of out put voltage seven level

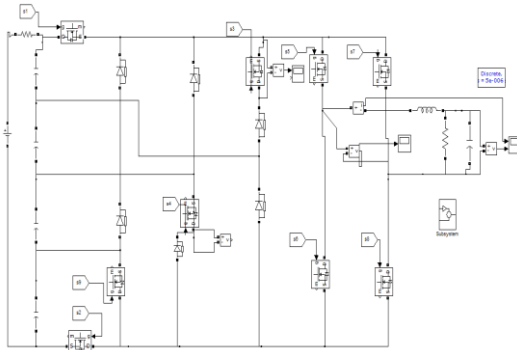


Fig. 22. Simulink model of proposed MLI for Nine level Output voltage

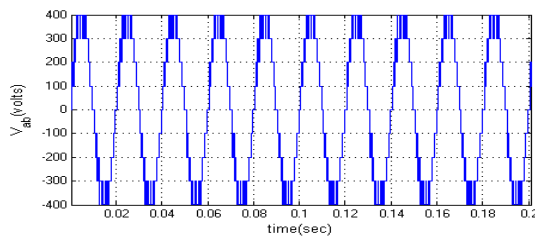


Fig. 23. Waveform of  $v_{ab}$ .

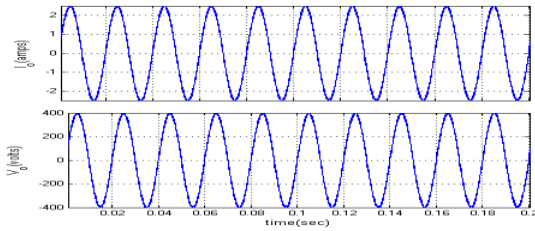


Fig. 24. Output voltage & current

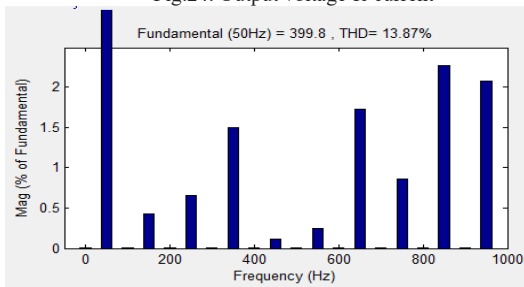


Fig. 25.

THD of Output voltage for Nine level

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

## VI. CONCLUSION

A novel seven-level inverter was designed and implemented with DSP in this paper. The main idea of the

proposed configuration is to reduce the number of power device. The reduction of power device is proved by comparing with traditional structures. Finally, a laboratory prototype of seven-level inverter with 400-V input voltage and output 220  $V_{rms}/2$  Kw is implemented. Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

## REFERENCES

- [1] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2694–2702, Jul. 2008.
- [2] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.
- [3] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated, ac module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.
- [4] R. A. Ahmed, S. Mekhilef, and W. P. Hew, "New multilevel inverter topology with minimum number of switches," in *Proc. IEEE Region 10 Conf. (TENCON)*, 2010, pp. 1862–1867.
- [5] M. R. Banaei and E. Salary, "New multilevel inverter with reduction of switches and gate driver," in *Proc. IEEE 18th Iran. Conf. Elect. Eng. (IECC)*, 2010, pp. 784–789.
- [6] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
- [7] K. Hasegawa and H. Akagi, "A new dc-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 841–852, Mar./Apr. 2011.
- [8] T. Ito, M. Kamaga, Y. Sato, and H. Ohashi, "An investigation of voltage balancing circuit for dc capacitors in diode-clamped multilevel inverters to realize high output power density converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2010, pp. 3675–3682.
- [9] A. Shukla, A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2249–2261, Jul. 2010.
- [10] C. L. Xia, X. Gu, T. N. Shi, and Y. Yan, "Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 18–29, Mar. 2011.
- [11] K. Sano and H. Fujita, "Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1768–1776, Nov./Dec. 2008.
- [12] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral point clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
- [13] Suroso and T. Noguchi, "New generalized multilevel current-source PWM inverter with no-isolated switching devices," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst. (PEDS)*, 2009, pp. 314–319.
- [14] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149–158, Jan. 2009.
- [15] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
- [16] N. Vazquez, H. Lopez, C. Hernandez, E. Vazquez, R. Osorio, and J. Arau, "A different multilevel current-source inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2623–2632, Aug. 2010.

- [17] K. A. Tehrani, I. Rasoanarivo, H. Andriatsioharana, and F. M. Sargos, "A new multilevel inverter model NP without clamping diodes," in *Proc. 34th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, 2008, pp. 466–472.
- [18] G. Ceglia *et al.*, "A new multilevel inverter topology," in *Proc. Devices Circuits Syst.*, 2004, vol. 1, pp. 212–218.
- [19] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Comparison of neutralpoint-clamped, symmetrical, and hybrid asymmetrical multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2297–2306, Jul. 2010.

## BIBLIOGRAPHY



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