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Design A Fault Tolerant Fft's Using Ahl Logic And Razor Flipflop

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ABSTRACT: *The complexity of communications and signal processing circuits increases every year. This is made possible by the CMOS technology scaling that enables the integration of more and more transistors on a single device. This increased complexity makes the circuits more vulnerable to errors. At the same time, scaling means that transistors operate with lower voltages and are more susceptible to errors which are caused by noise and manufacturing variations. Soft errors cause a reliability threat to modern electronic circuits. This makes protection against soft errors which is a requirement for many applications. Communications and signal processing systems do not have any exceptions to this trend. An interesting option is to utilize algorithmic-based fault tolerance (ABFT) techniques which is try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT technique. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, the Perseval or sum of squares check is the most widely known protection scheme. In proposed system, two improved protection schemes that combine the use of error correction codes and Perceval checks are proposed and evaluated.*

***Index Terms*—Error correction codes (ECCs), fast Fourier transforms (FFTs), soft errors.**

I.INTRODUCTION

The complexity of communications and signal processing circuits increases every year. This is made possible by the CMOS technology scaling that enables the integration of more and more transistors on a single device. This increased complexity makes the circuits more vulnerable to errors.

At the same time, the scaling means that transistors operate with lower voltages and are more susceptible to errors caused by noise and manufacturing variations.

The importance of radiation-induced soft errors also increases as technology scales. Soft errors can change the logical value of a circuit node creating a temporary error that can affect the system operation. To ensure that soft errors do not affect the operation of a given circuit, a wide variety of techniques can be used. These include the use of special manufacturing processes for the integrated circuits like, for example, the silicon on insulator. Another option is to design basic circuit blocks or complete design libraries to minimize the probability of soft errors. Finally, it is also possible to add redundancy at the system level to detect and correct errors.

Error correction code (ECC) techniques have been widely used to correct transient errors and improve the reliability of memories. ECC words in memories consist of data bits and additional check bits because the ECCs used in memories are typically from a class of linear block codes. During the write operations of memories, data bits are written in data bit arrays, and check bits are concurrently produced using the data bits and stored in check bit arrays. The check bit arrays, just like the data bit arrays, should be tested prudently for the same fault models if reliable error correction is to be insured. Fast Fourier transform is used to convert a signal from time domain to frequency & this is

needed so that you can view the frequency components present in a signals.

II.EXISTED SYSTEM

A single Error Correction Hamming Code is presented. The original system consists of four FFT modules and three redundant modules which are added for detecting and correcting the errors. The inputs to the redundant modules are linear combination of inputs. They are used to check linear combinations of the outputs. In this technique, the overheads are lower than TMR as the number of redundant FFTs is related to the logarithm of the number of original FFTs. Let us take example, for protecting the four FFTs three redundant FFTs are needed and to protect eleven FFTs, four redundant FFTs are needed. Hence, it shows that decreasing the overheads with the number of FFTs.

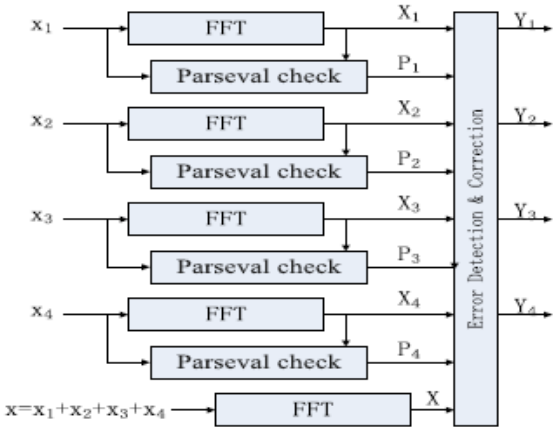

FIG 1.PARITY SOS FAULT TOLERANT PARALLEL FFTS

Sum of Squares (SOSs) check is one of the techniques for protecting the FFT. This technique is based on the Parseval theorem that states that the SOSs of the inputs to the FFT are equal to the SOSs of the outputs of the FFT excluding a scaling factor. This relationship can be used for detecting the errors with low overhead for each input or output sample.

SOS check can be combined with the ECC for reducing the protection overhead for the parallel FFTs. Hence SOS check only detects the errors and ECC should implement the correction. This can be achieved by using a single parity bit for all FFTs. The combination of parity FFT and the SOS check can reduces the number of additional FFTs. This scheme will be referred as parity-SOS.

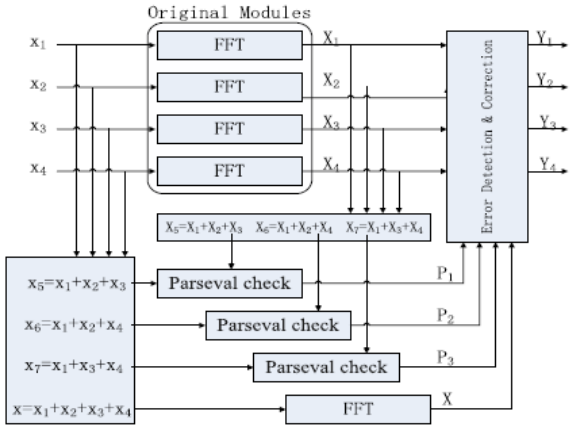

FIG 2. PARITY SOS-ECC FAULT TOLERANT PARALLEL FFTS

An additional parity FFT is used for correcting the errors in Parity-SOS scheme. This technique is shown in above fig 2. The main advantage is to reduce the number of SOS checks needed. This scheme is referred as parity-SOS-ECC technique. Hence, final observation is that ECC scheme can detect all the errors which exceed a threshold and SOS can detect most errors. Therefore, fault injection experiments to be done for determining the percentage of errors which are actually corrected.

III.PROPOSED SYSTEM

A new scheme is proposed which is based on the Error Correction Codes (ECC). In this technique, each filter can be equivalent of a bit and by using addition parity check bits can be computed. The operation of this technique is the output of the sum of the several inputs is the

sum of the individual outputs. So, this is valid for any linear operation.

A final observation is that the ECC scheme can detect all errors that exceed a given threshold (given by the quantization used to implement the FFTs). On the other hand, the SOS check detects most errors but does not guarantee the detection of all errors. Therefore, to compare the three techniques for a given implementation, fault injection experiments should be done to determine the percentage. Implementations of the SOS check errors that are actually corrected. This means that an evaluation has to be done both in terms of overhead and error coverage.

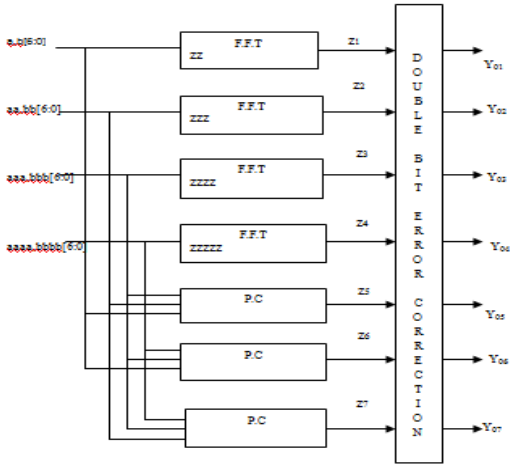

FIG 3. PARALLEL FFT PROTECTION USING ECCS

It is assumed that there is only a double error on the system at any given point in time. There are three main contributions. They are

1) Error Correction Code is assessed to protect the parallel FFTs which show its effectiveness in terms of overhead and protection effectiveness.

2) A new technique is proposed depends on the use of Parseval or sum of squares (SOSs) checks combined with parity FFT.

3) A new technique is proposed on which the ECC is used on the SOS checks instead of the FFTs.

This scheme is evaluated by using FPGA implementations to assess the protection overhead. The protection overhead can be reduced by combining the use of ECCs and parseval checks. For the less error prone applications technique two can be used with Partial summation block replacing the Parseval check. Both the new techniques proposed uses minimum hardware resources compared to the existing design by the modification of Partial summation block for Sum of Squares.

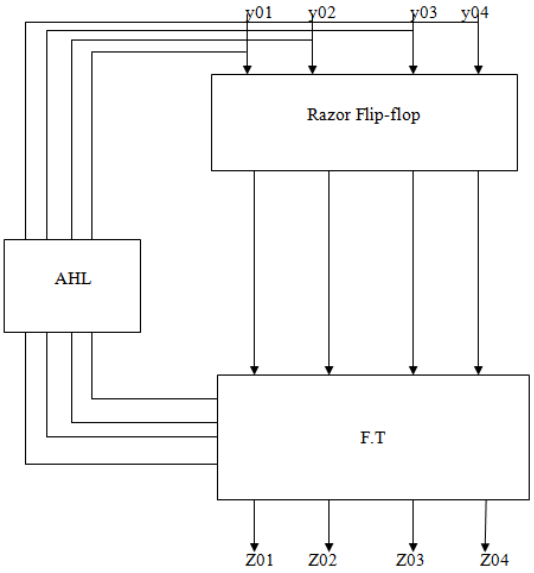

FIG. 4 BLOCK DIAGRAM OF PROPOSED SYSTEM

Block diagram of proposed system is shown in Fig 4. Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and multiplexer. The main flip-flop catches the execution result for the combination circuit using a normal clock signal. The shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal.

If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the

system to re-execute the operation. It also notifies the AHL circuit that an error has occurred.

IV.RESULTS

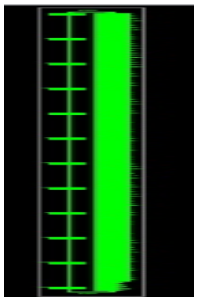

FIG. 4 RTL SCHEMATIC DIAGRAM

Figure 4 shows the RTL schematic of the proposed system.

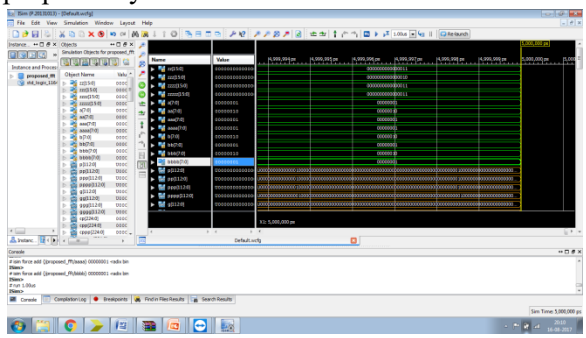

FIG.5 OUTPUT WAVEFORM

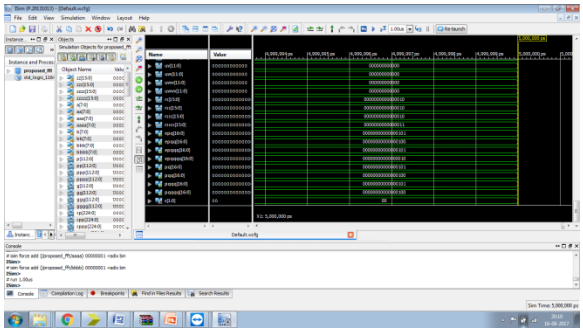

FIG.6 OUTPUT WAVEFORM

Figure 5 & 6 shows the output waveforms for parallel FFT

V.CONCLUSION

Detecting and correcting errors such as critical reliability are difficult in signal processing which increases the use of fault tolerant implementation. In modern signal processing circuits, it is common to find several filters operating in parallel. Proposed system is an area efficient technique to detect and correct single errors. This The approach is based on applying SOS-ECC check to the parallel FFT outputs to detect and correct errors. The SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. The 8 point FFT with the input bit length 32 is protected using the proposed technique. . The detection and location of the errors can be done using an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. This technique can detect and correct only single bit error and it reduces area results in high speed compared to existing techniques.

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