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# Design of 3t Gain Cell Edram for Low Power Application

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**ABSTRACT:** *Logic compatible gain cell (GC)-embedded DRAM (eDRAM) arrays are considered an alternative to SRAM because of their small size, non rationed operation, low static leakage, and two-port functionality. But traditional GC-eDRAM implementations require boosted control signals in order to write full voltage levels to the cell to reduce the refresh rate and shorten access times. The boosted levels require an extra power supply or on-chip charge pumps, as well as nontrivial level shifting and toleration of high voltage levels. In this paper, we present a novel, logic compatible, 3T GC-eDRAM bit cell that operates with a single-supply voltage and provides superior write capability to the conventional GC structures.*

**Index Terms—Embedded DRAM, gain cell, data retention time, low power operation.**

## I.INTRODUCTION

Memories have occupied large proportion of the die area of VLSI system-on chips in recent years. Major reason for this is increasing number of components as in case of 6T SRAM it has large 6-transistor the various other reasons are area consuming, peripheral circuitry. Embedded memories have turned to be an important one in the long standby mode it continues to leak more power which characterizes the system performance.

Initially SRSAMs are used for storing data bits in memory. But it has some of the disadvantages like large area, more power consumption even though it has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free data retention time. It also has some other disadvantages like static leakage of current, under voltage scaling and large transistor count. These limitations can be overcome by usage of gaincell (GC)-embedded DRAM (eDRAM) such as circuit which provides full CMOS logic compatibility of 2-transistor (2T) or 2-transistor (3T) GC eDRAMS resulting in non-ratioed operation and low static leakage currents from VDD to GND. Inspite of overcoming most of the disadvantages of static memories GC-eDRAM requires periodic refreshing operation. However, as opposed to static memories the data retention time of GC-eDRAM depend on dynamically stored charge.

## II. EXISTING METHOD

**A. 6T SRAM:** Basic static RAM circuits can be viewed as vibrations on the designs used for latches and flip-flops more aggressive static RAMs make use of design tricks originally developed RAMs to speed up the system.

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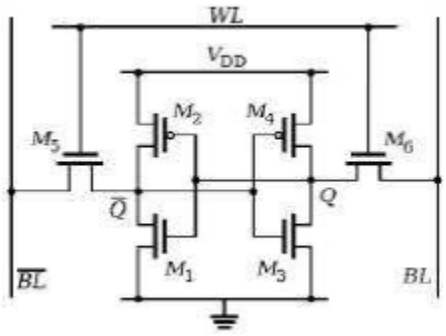


**Fig.1 6T RAM Cell**

The value is stored in the middle four transistors, of Fig.1 which form a pair on inverters connected in a loop. The other two transistors control access to the memory cell by the bit lines. When select = 0, the inverters reinforce each other to store the value. A read or write is performed when cell is selected.

To read, bit and bit are pre charged to before the select line is allowed to go high. One of the cell's inverters will have its output at 1, and the other at 0, which inverter is 1 depends on the value stored. The right hand inverter's pull down and the bit line will be drained to through that inverter's pull down and the bit line will remain high. If the opposite value is stored in the cell, the bit lines will be pulled own while bit remains high. To write, the bit and bit lines are set to the desired value, then select is set to 1.charge sharing forces the inverters to switch values, if necessary, to store the desired value. The bit lines have much higher capacitance than

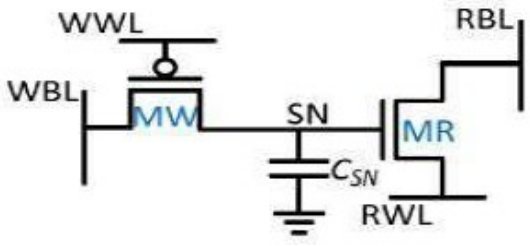


**Fig 2. 2T Mixed Gain Cell**

For a read operation a PMOS MR requires a pre-discharge of the parasitic RBL capacitance followed by raising the read word line (RWL). If the selected bit cell's storage mode (SN) holds a loop value, MR is the inverters, so the charge on the bit lines is enough to overwhelm the inverter pair and cause it to flip state.

**B. 2T Mixed Gain Cell:** 2T mixed GC can be implemented with either an NMOS or a PMOS device as shown in Fig.2. Moreover, both MW (write transistor) and MR (read transistor) can be implemented with standard threshold voltage core or high threshold voltage I/O devices in the considered CMOS technology. Due to the voltage drop across MW, a boosted write word line (WWL) voltage is required during write access above $V_{DD}$ for NMOS operation and below $V_{SS}$ for PMOS operation. Conducting and charges RBL post a detectable sensing threshold. If SN holds value MR is cut-off such that RBL remains discharged below the sensing threshold. For the NMOS implementation of MR, the operation is exactly opposite i.e. RBL is precharged and RWL is lowered to initiate a read.

## III. PROPOSED SYSTEM

We present a new topology for a 3TGC, featuring a complementary transmission gate in the write port. While the proposed solution is quite straight forward it is novel and its impact in very high. We demonstrate the functionality of the proposed system used in ultra-low power applications such as biomedical sensor nodes and implants.

**A. 3T Gain Cell eDRAM:** 3T GC consists of write port featuring a complementary transmission gate PMOS write (PW) and NMOS write (NW) a storage node (SN) composed $C_{SN}$ of the three transistors, a read port based on

NMOS read (NR) and the metal interconnect as in Fig 3. The GC is built that all the transistors operates with standard $V_T$ voltage and is fully compatible with standard digital CMOS technologies. The gates of PW and NW are connected to the world line of PMOS and NMOS WWLp and WWLn. A common write bit line is used to drive the data to the transmission gate during write operations. When the full-swing is given to the cells transmission gate enables the propagation of strong levels to the SN without any need for boosted world line.

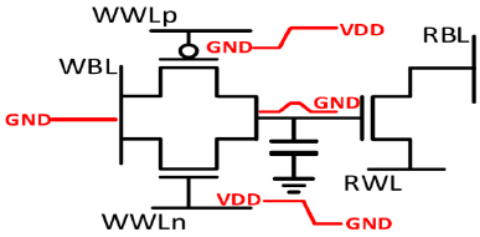


**Fig.3. 3T Gain Cell eDRAM**

Read operation is performed by precharging the read bit line (RBL) to $V_{DD}$ and subsequently driving the read word line (RWL) to GND. If the storage node is already high it discharges RBL capacitances or blocking the discharge path if SN is low. IN order to achieve a tradeoff between speed, area, power and reliability, a dynamic sense amplifier can be used to improve the read operation.

**B. Operation:** The voltage was chosen as a good medium voltage between $V_{DD}$ and $V_T$ since the data retention time (DRT) is proved to be efficient in GC-eDRAM design at this voltage starting with charged $C_{SN}$ WBL is driven low and the world lines WWLp is set to 0 and WWLn is set to $V_{DD}$. Then a strong 0 level is passed to the SN, during standby, the level on SN deteriorates due to leakage currents dominated by the sub threshold leakage of PW and NW in mature CMOS nodes. Hence in order to extend the retention time WBL is driven to $V_{DD}$ during standby and read cycles thereby significantly reducing the sub threshold leakage through the transmission gate for both stored low and high values compared with the condition where WBL is either driven to either $V_{DD}$ or GND.

During readout the 0 level blocks the discharge path through NR, maintaining the precharged voltage on RBL. During the next write operation WBL is driven high, resulting in a strong 1 stored on the SN. The subsequent read operation provides a strong gate overdrive to transistor NR, thereby discharging RBL to read a 1. It should be noted that during this operation (Read 1), bit cells storing 1 and sharing the same column turn on when RBL discharges by more than the $V_T$ of NR, causing it to saturate before it can completely discharge.

**C. Data Retention Time:** The data retention time (DRT) of GC embedded DRAMS is the time interval for writing a data level in the bit cell to the last moment the data can still correctly read out the stored information. For 2T and 3T cells methodology which are affected by the initially degraded voltage level corresponding to the data values due to the threshold voltage ($V_T$) drop across the write transistor DRT is primarily limited by the initial charge stored on the internal bit cell capacitance and the leakage currents that degrade the stored voltage level over time.

In order to describe this issue a boosted write world line (WWL) voltage is usually employed to pass a full swing level to the storage capacitance. Any how this requires the generation of boosted on-chip voltage, which entails substantial overhead. The magnitude of the voltage boost is set not only to overcome the

$V_T$ drop, but also to achieve short write access time which otherwise are typically longer than 6T SRAM implementation. The proposed bit cells provides strong initial data levels for enhanced DRT and robust operation as well as for fast write access time.

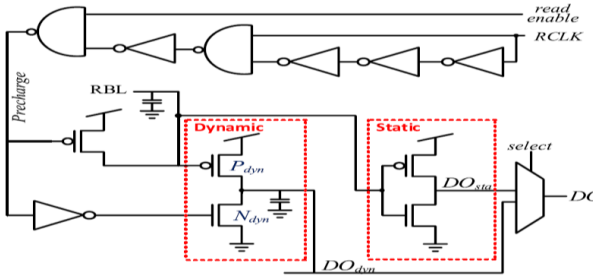


**Fig.4.ReadOut Circuitry**

## IV.RESULTS

## V.CONCLUSION

This paper proposes a novel 3T GC eDRAM microcell target and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations. When compared with 6T SRAM technology and 2T mixed gain cell technology it has less consumption of power. The proposed cell exhibits faster write-access than conventional GC circuits, thereby increasing DRTs and reducing refresh power consumption. The average power consumption at write access time is less than that of read access time. Testing is the major issue in eDRAM technology. So, in future various testing method can be used to check the better performance of the circuit.

## VI.REFERENCES

[1] Raychowdhuryet al., "PVT-and-aging adaptive word line boosting For 8T SRAM power reduction," in Proc. IEEE ISSCC, Feb. 2010, pp. 352353.

[2] A. Teman, P. Meinerzhagen, R. Giterman, A. Fish, and A. Burg, "Replica Technique for adaptive refresh timing of gain-cell-embedded DRAM,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 4, pp. 259–263, Apr2014

[3] D. Somasekharet al., "2 GHz 2 Mb 2T gain cell memory macro with 128 GBytes/sec bandwidth in a 65 nm logic process technology,"IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 174–185, Jan. 2009.

[4] G. M. S. Reddy and P. C. Reddy, "Design and implementation of 8k-bits Low power SRAM in 180nm technology," in Proc. IMCECS, vol. 2. 2009,

[5] K. C. Chun, P. Jain, T.-H. Kim, and C. H. Kim, "A 667 MHz logic compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," IEEE J. Solid-State Circuits, vol. 47, no. 2 pp. 547–559, Feb. 2012.

[6] K. C. Chun, P. Jain, J. H. Lee, and C. H. Kim, "A 3T gain cell embedded DRAM utilizing preferential boosting for high density and low power on die Caches," IEEE J. Solid-State Circuits, vol. 46, no. 6, pp. 1495–1505, Jun. 2011.

[7] K. C. Chun, W. Zhang, P. Jain, and C. H. Kim, "A 2T1C embedded DRAM macro with no boosted supplies featuring a 7T SRAM based Repair and a cell storage monitor," IEEE J. Solid-State Circuits, vol. 47,no. 10, pp. 2517–2526, Oct. 2012..