International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 04
February 2018

An Efficient Design of Three-Input Xor/Xnor Systematic Cell

Suthapalli Venkatrao, S.Sailaja, D Mohan Reddy

[1]PG Scholar,Dept of ECE, Amalapuram Institute Of Management Sciences & College of Engineering

[2] Assistant professors Dept of ECE, Amalapuram Institute of Management Sciences & College Of Engineering

[3]Professor & Principal, Amalapuram Institute of Management Sciences and College of Engineering, Mummidivaram, East Godavari District, Andhra Pradesh, India

Abstract:
An efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style is proposed in this paper. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy full swing and fairly balanced outputs. We can extend this project for designing of full adder design and it's topologies.

Keywords - XOR/XNOR Circuits, SCDM, Hybrid CMOS, Transmission Gate

I. INTRODUCTION

The rapid growth of portable electronic devices is a critical challenge to design low-power, high-speed circuits that occupy small chip areas. Such studies mostly rely on creative design thoughts but do not follow a systematic approach. As an importance, most of them suffer from some different drawback.

1. They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to the static power dissipation.
2. Most of them undergo from severe output signal degradation and cannot sustain low voltage operation.
3. They predominantly have a dynamic power consumption for non-balanced propagation delay inside and outside circuits, which results in glitches at the outputs.

A well-organized design methodology can be regarded as a strong clarification for the challenge. It is not try and-error-driven, which means that it systematically and intentionally aims to design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some narrow functions, such as two input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style. The predominant results persuade us to develop CDM through two stages:

1. Generating more complex functions and
2. Rectifying some remaining flaws.

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gate is the critical parts of several digital systems and it is highly used for very large scale integration (VLSI) system. The XOR/XNOR circuits used in parity checkers, comparators, crypto processors, arithmetic and logic circuits, test pattern generators. The SCDM methodology for design a XOR/XNORs

gate and design is implemented. The first time Systematic Cell Design Methodology (SCDM) designing a three-input XOR/XNORs. Its systematically generates elementary basic cell (EBC) by using the binary decision diagram (BDD), and wisely chooses circuit components based on a specific target.

II.SCDM FOR THREE-INPUT XOR/XNOR CIRCUITS

The methodology for three-input XOR/XNORs are presented according to the flowchart shown in Fig.1(a).In the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input a basic gate in arithmetic circuits has been chosen. If the efficiency of the circuits is confirmed in such an economic environment, it can be show that the strength of the methodology. In the second stage, Cell Design Methodology is matured as systematic Cell Design Methodology (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell using binary decision diagram, and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the Cell Design Methodology.

After the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) the wise selection of the basic cell; 2) the wise selection of the amend mechanisms; and 3) the transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets.

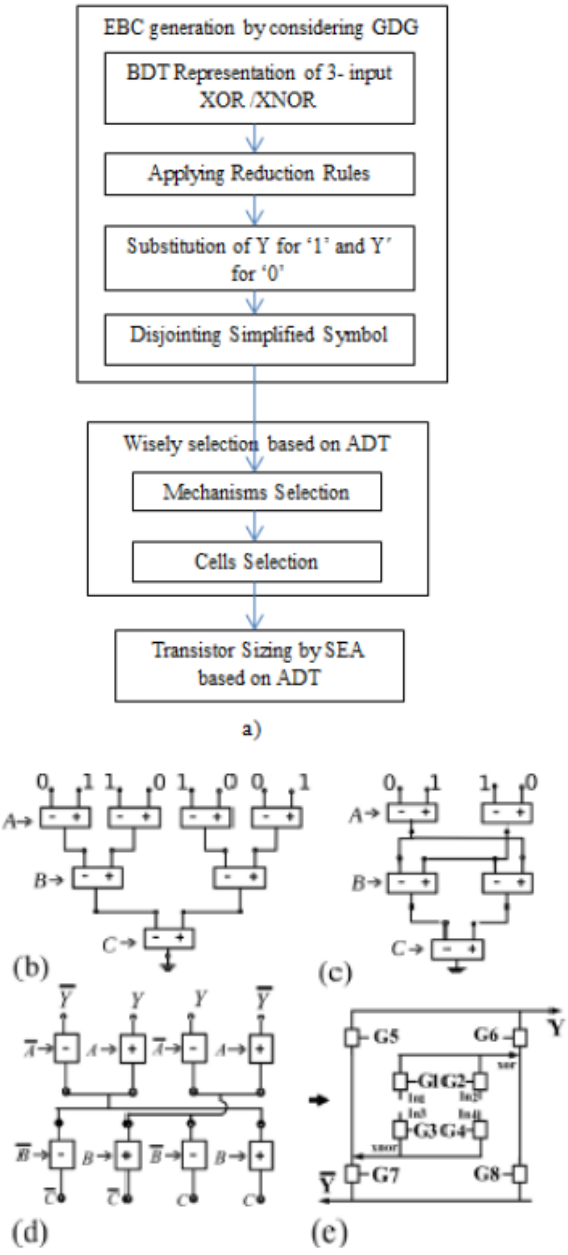

Fig.1. (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC.

III.ELEMENTARY BASIC CELL SYSTEMATIC GENERATION

In order to generate the Elementary Basic Cell (EBC) of three-input XOR/XNOR circuits, four steps are taken. Initially, three-input XOR and its complement are represented by one binary decision tree in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by the basic symbol controlled with input variables at each correspondent level. This construction simply implements the min-terms of the three-input XOR/XNOR function. This step is followed by applying reduction rules to simplify the BDT representation. This includes elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls.

A. Wisely Selection of Mechanisms and Cells Based on Design Target: The replacing elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce circuits for high-performance portable electronic applications. This Mechanisms include optimization mechanisms to resolve non-full swing inverter and feedback , correction mechanisms to resolve high impedance pull up-down network and feedback , or the combinations of them bootstrap-pull up-down, feedback pull up-down, bootstrap-feedback , inverter-feedback , and inverter-pull up-down.

B. Transmission Gates: Complementary Metal Oxide Semiconductor (CMOS) is a technology for integrated circuits. The CMOS circuits use a combination of p-type and n-type Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) to implement logic gates and other digital circuits. The transmission gate is made up of two field effect transistors thus the transistors are n-channel MOSFET and p-channel MOSFET are connected with parallel with each other. In that the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. A transmission gate must block flow in either direction thus the substrate terminals are connected to the supply voltage. The substrate terminal of the p-channel MOSFET is connected to the positive supply voltage and the substrate terminal of the n-channel MOSFET are connected to negative supply voltage.

C. Advantages of Transmission Gate:

1. Logic circuits can be constructed with the relief of transmission gates instead of traditional CMOS pull-up and pull-down networks.
2. The circuits can frequently be made more compact, which can be an important consideration in silicon implementations.
3. In a security application, they can selectively block critical signals or data from being transmitted without suitable hardware controlled authorization.

IV.RESULTS

V.CONCLUSION

To design a three input XOR/XNOR gate and the analytical expression of optimum frequency and supply voltage under minimum energy condition has been

verified. The performance of the proposed circuits can operate at low voltages, and have good output levels. According to the simulation results, the proposed circuit offers a better result and more competitive than other design. It offers the lowest power dissipation at a low supply voltage. It has a good driving capability with good output signal in all input combinations and well performance especially in low supply voltage compared to the previous designs. Thus, the proposed circuit is suitable for low-voltage and low-power application. In future work 8-bit adder architecture based on the design of three-input XOR/XNOR gate will be designed. The power consumption and delay performance are calculated and compared with the existing system.

VI.REFERENCES

[1] C.-K. Tung, S.-H. Shieh, and C.-H. Cheng, "Low-power high-speed full adder for portable electronic applications," *Electron. Lett.*, vol. 49, no. 17, pp. 1063–1064, Aug. 2013.

[2] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 718–721, Apr. 2011.

[3] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, T. Nikoubin, and O. Kavehei, "Novel direct designs for 3-input XOR function for low-power and highspeed applications," *Int. J. Electron.*, vol. 97, no. 6, pp. 647–662, 2010.

[4] S. Goel, M. A. Elgamel, M. A. Bayoumi, and Y. Hanafy, "Design methodologies for high-performance noise-tolerant XOR-XNOR circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 4, pp. 867–878, Apr. 2006.

[5] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[6] C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[7] T. Nikoubin, M. Grailoo, and S. H. Mozafari, "Cell design methodology based on transmission gate for low-power high-speed balanced XOR-XNOR circuits in hybrid-CMOS logic style," *J. Low Power Electron.*, vol. 6, no. 4, pp. 503–512, 2010.

[8] T. Nikoubin, A. Baniasadi, F. Eslami, and K. Navi, "A new cell design methodology for balanced XOR-XNOR circuits for hybrid- CMOS logic," *J. Low Power Electron.*, vol. 5, no. 4, pp. 474–483, 2009.

[9] T. Nikoubin, M. Grailoo, and C. Li, "Cell design methodology (CDM) for balanced Carry–InverseCarry circuits in hybrid-CMOS logic style," *Int. J. Electron.*, vol. 101, no. 10, pp. 1357–1374, 2014.