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Adaptive Approaches of Built-In-Self-Test for Low Power Integrated Circuits

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***Abstract*— A new low-power (LP) scan-based built-in self-test (BIST) technique is proposed based on weighted pseudo-random test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design-for-testability architecture is modified slightly while the linear-feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach.**

***Index Terms*— Low-power (LP) built-in self-test (BIST), reseeding, scan-based BIST, weighted test-enable signals.**

I. Introduction

The gap between functional and test power consumption is growing bigger and bigger technology node in the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power [8]. Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe [61], [62]. More details on how to provide more accurate power model can be found from [61] and [62]. A fast simulation approach was proposed for low-power (LP) off-chip interconnect design in [61]. An important through silicon via (TSV) modeling/simulation technique for LP 3-D stacked IC design was presented in [62].

Low Power Integrated Circuits with less Technology node brings more complex designs. More advanced functionalities with more gate count causes the design to be tested using adaptive methodologies and techniques bringing out high Fault Coverage (FC) and Test Coverage (TC). While Scan based designs are considered, power consumption and Timing analasys plays a major role. More care has to be taken to generate patterns and test the circuit at minimal power usage of less than 100 Mhz of frequency . Toggling of data at low frequency can reduce the power dissipation but may not meet the required Test Time (TT). So Adaptive Built-in Self-test (BIST) approaches might solve the issue of Power Dissipation by limiting the length of Scan chains.Furthermore , the power dissipation of scan -based built -in self -test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities caused by random. patterns. Therefore, it is essential to propose an effective LP BIST approach.

Recent methods in [10], [33], [43], [46], and [63] aim at reducing the switching activity during scan shift cycles, whose test generator allows automatic selection of their parameters for LP pseudorandom test generation. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudo-random testing schemes [21], [24], [37], [44] and methods in [20], [50], [56], and [57] can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG). This is one of the major motivations of this paper.

Most of the previous deterministic BIST approaches did not include LP concerns. We intend to present a new method that effectively combines an efficient LP PRPG and LP deterministic BIST. In order to reduce test power in deterministic BIST, we will propose a new LP reseeding scheme, since there is no other effective solution in this field. This is another motivation of this paper.

In this paper, we propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding. We present the major contributions of this paper in the following.

1) A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design-for-testability (DFT) architecture to implement the LP BIST scheme is presented. Our method generates a series of degraded subcircuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded subcircuits, which are activated to maximize the testability.
2) A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random-pattern-resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme

can cover a number of vectors with fewer care bits, which allows a small part of flip flops to be activated in any clock cycle.

The rest of this paper is organized as follows. The related work is presented in Section II. The new LP weighted pseudorandom test generation approach is described in Section III. The new LP deterministic BIST method with reseeding is presented in Section IV. Experimental results are shown in Section V. This paper is concluded in Section VI.

II. Related Work

Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. Tsai *et al.* [50] proposed a novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented in [20], selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST.

Weighted pseudorandom testing schemes [21], [24], [37], [44], [56], [57] can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pattern generation scheme was proposed for scan-based BIST in [56], according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. A reconfigurable scan architecture was used for the deterministic BIST scheme in [57] using the weighted test-enable signal-based pseudorandom test generation scheme. Lai *et al.* [29] proposed a new scan segmentation approach for more effective BIST.

LP BIST approaches were proposed early in [7], [15]–[17], and [64]. Zorian [64] proposed a distributed BIST control scheme in order to simplify the BIST execution of complex ICs. The average power was reduced and the temperature was reduced. The methods reduced switching activity during scan shifts by adding extra logic [7], [15]. A new random single-input change test generation scheme in [16] generates LP test patterns that provide a high level of defect coverage during LP BIST of digital circuits. An LP BIST scheme was proposed based on circuit partitioning [17].

New pseudorandom test generators were proposed to reduce power consumption during testing [1], [10], [28], [30], [33], [35], [36], [46], [49]. A new encoding scheme is proposed in [30], which can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test data volume. Lai *et al.* [28] proposed a new LP PRPG for scan-based BIST using a restricted scan-chain reordering method to recover the fault coverage loss. A low-transition test pattern generator in [35] was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions: 1) between consecutive patterns and 2) between consecutive bits. Abu-Issa and Quigley [1] proposed a PRPG to generate test vectors for test-per-scan BISTs in order to reduce the switching activity while shifting test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented.

A new adaptive low shift power pseudorandom test pattern generator was presented in [33] to improve the tradeoff between test coverage loss and shift power reduction in logic BIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation among adjacent test stimulus bits. Filipek *et al.* [10] and Solecki *et al.* [46] proposed LP programmable generators capable of producing pseudorandom test patterns with desired toggling levels.

Wang *et al.* [43] proposed a new LP BIST technology that reduces shift power by eliminating the specified high-frequency parts of vectors and also reduces capture power. Omaña *et al.* [36] proposed a novel approach to reduce peak power and power droop during capture cycles in scan-based logic BIST. An efficient BIST architecture was recently presented in [53] for targeting defects in dies and in the interposer interconnects.

A novel low-power BIST technology was proposed in [49] that reduces shift power by eliminating the specified high-frequency parts of vectors and also reduces capture power. Multicycle tests support test compaction by allowing each test to detect more target faults. The ability of multicycle broadside tests to provide test compaction depends on the ability of primary input sequences to take the circuit between pairs of states that are useful for detecting target faults. This ability can be enhanced by adding DFT logic that allows states to be complemented in [38].

A new DFT scheme for launch-on-shift testing was proposed in [39], which ensures that the combinational logic remains undisturbed between the interleaved capture phases, providing computer-aided-design tools with extra search space for minimizing launch-to-capture switching activity through test pattern ordering.

Complete fault coverage can be obtained [9] when the pseudorandom test generator is modified. A combination of a pseudorandom test generator and a combinational mapping logic was constructed by Chatterjee and Pradhan [9] to produce a given target pattern set of the hard-to-detect faults.

Deterministic vectors can be encoded into LFSR seeds [18], [19], [25]–[27], [32], [34], [42], [56]. Koenemann [27] proposed the seminal work, which encoded deterministic vectors into seeds. The requirement on the average size of the LFSR can be reduced by using multiple primitive polynomials [18]. Deterministic vectors were encoded by using a folding counter and compressed by a tree architecture in [19] and [32]. Li and Chakrabarty [34] proposed a reconfigurable scan architecture for effective deterministic BIST. LP design was implemented in the new methodology in [26] to increase the encoding efficiency by combining reseeding and bit fixing.

The work in [22] is about LP delay testing, whose scan architecture and test application scheme are completely different from the new method. Our method is about scan-based BIST for single stuck-at faults based on a new weighted

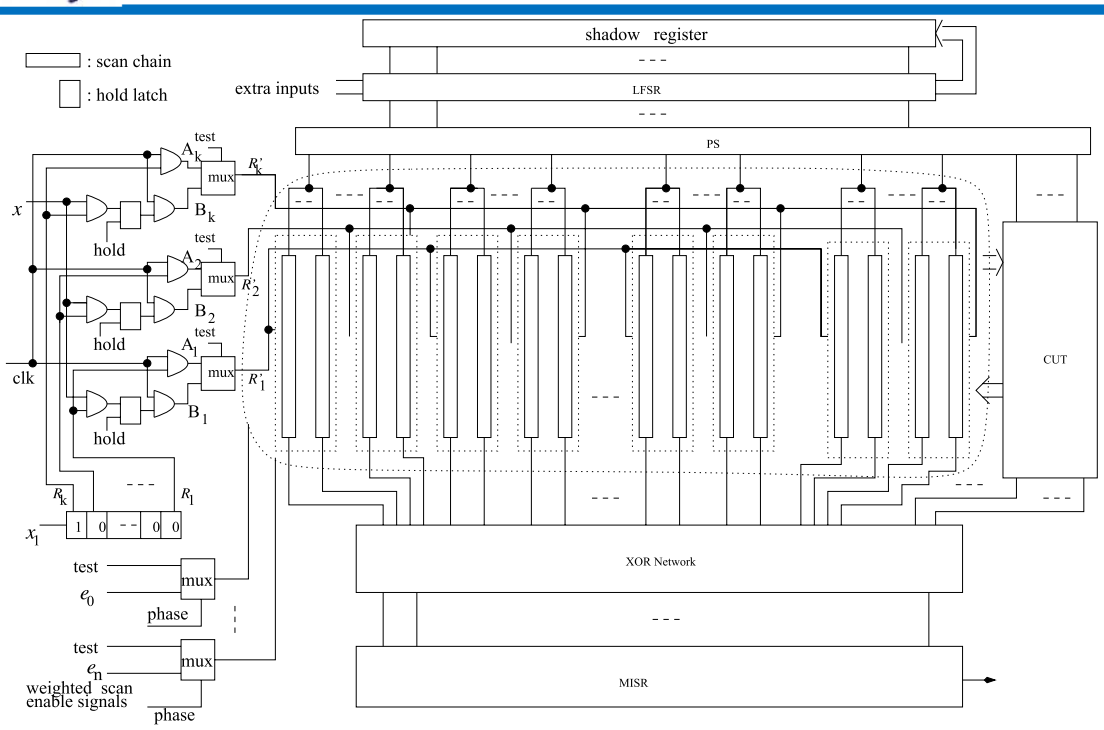

Fig. 1. General DFT architecture for LP scan-based BIST.

pseudorandom test generator and an LP deterministic BIST approach. The scan architecture in [23] is quite similar to the method in [22]. Both methods do not require test response shift-out operations, which do not cause zero aliasing.

Wen *et al.* [54], [55] proposed novel X-filling method by assigning 0 and 1 s to unspecified (X) bits in a test cube obtained during ATPG. This method reduces the circuit switching activity in capture mode and can be easily incorporated into any test generation flow to achieve capture power reduction without any area, timing, or fault coverage impact. A new scan shifting method based on the clock gating of multiple groups was proposed in [45] by reducing the toggle rate of the internal combinational logic. This method prevents cumulative transitions caused by shifting operations of the scan cells, because all scan flip flops are connected to the XOR network for test response compaction.

It is possible to implement LP scan testing in a test compression environment without any increase on test application cost [60]. Xiang *et al.* [59] proposed a new scan architecture to compress test data and compact test responses for delay testing. An important TSV modeling/simulation technique for LP 3-D stacked IC design was presented in [47]. The connectivity of TSVs in many important circuits [48] also needs to be tested in an efficient way.

III. New Low-Power Weighted Pseudorandom Pattern Test Generator

We present the DFT architecture to implement the LP BIST method in Section III-A. The process to implement LP pseudorandom pattern generation is presented in Section III-B.

A. DFT Architecture

As shown in Fig. 1, the scan-forest architecture [57] is used for pseudorandom testing in the first phase. Each stage of the phase shifter (PS) drives multiple scan chains, where all scan chains in the same scan tree are driven by the same stage of the PS. Unlike the multiple scan-chain architecture used in the previous methods [10], [42], the scan-forest architecture is adopted to compress test data and reduce the deterministic test data volume. Separate weighted signals e_0, e_1, . . . , and e_n are assigned to all scan chains [56], [57] in the weighted pseudorandom testing phase (phase = 0), as shown in Fig. 1, which is replaced by the regular *test* in the deterministic BIST phase (phase = 1). Each scan-in signal drives multiple scan chains, as shown in Fig. 1, where different scan chains are assigned different weights. This technique can also significantly reduce the size of the PS compared with the multiple scan-chain architecture where each stage of the PS drives one scan chain. The compactor connected to the combinational part of the circuit is to reduce the size of the MISR. The shadow register is used for LP deterministic and reseeding, more details of which are described in Section IV-B.

The size of the LFSR needed for deterministic BIST depends on the maximum number of care bits of all deterministic test vectors for most of the previous deterministic BIST methods. In some cases, the size of the LFSR can be very large because of a few vectors with a large number of care bits even when a well-designed PS is adopted. This may significantly increase the test data volume in order to keep the seeds. This problem can be solved by adding a small number of extra variables to the LFSR or ring generator [10], [42] without keeping a big seed for each vector.

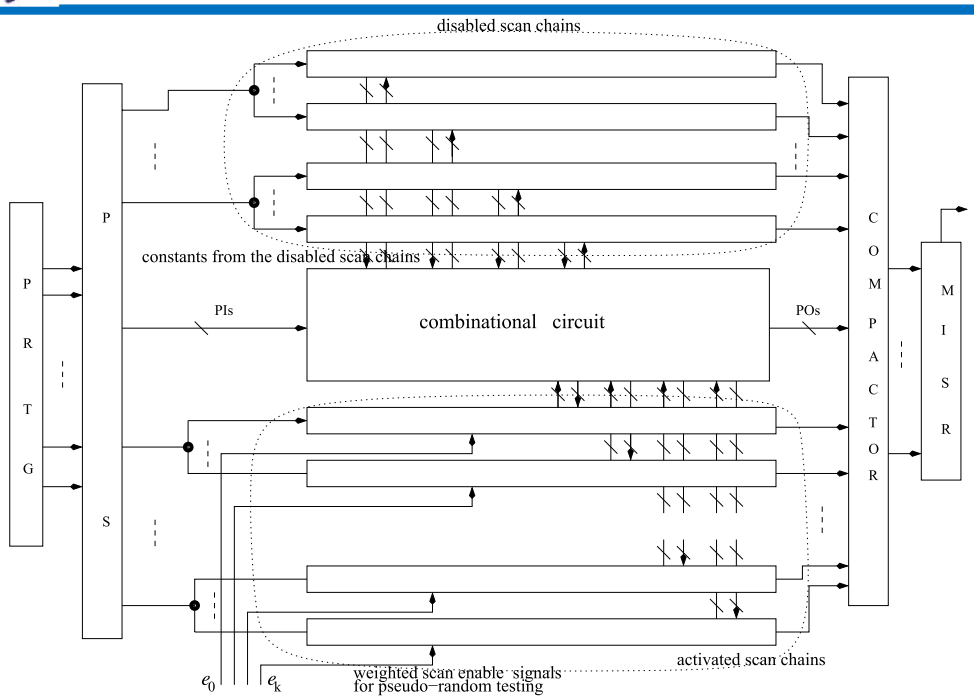

Fig. 2. Weighted pseudorandom test generator for scan-tree-based LP BIST.

We propose a new weighted PRPG for the new LP BIST approach. The new design is significantly different from the ones in [56] and [57]. This is mainly because the proposed LP design uses the gating technique to disable most of the scan chains, where the pseudoprimary inputs (PPIs) of the disabled scan chains are set to constant values. As shown in Fig. 1, all scan chains in the same scan tree are selected into the same subset of scan chains, which are driven by the same clock signal. Our method selects weights for each scan chain in the degraded subcircuits. Let the scan chains be partitioned into k subsets, where only one subset of scan chains is activated in any clock cycle. Our method selects optimal weights for all scan chains in the subset of scan chains in each round. It requires k separate rounds to determine optimal weights for all scan chains.

B. Weighted Pseudorandom Test Pattern Generation

Our method generates the degraded subcircuits for all subsets of scan chains in the following way. All PPIs related to the disabled scan chains are randomly assigned specified values (1 and 0). Note that all scan flip flops at the same level of the same scan tree share the same PPI. For any gate, the gate is removed if its output is specified; the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a noncontrolling value and it has at least three inputs. For a two-input AND or OR gate, the gate is removed if one of its inputs is assigned a noncontrolling value. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a noncontrolling value.

For an XOR or NXOR gate with more than three inputs, the input is simply removed from the circuit if one of its inputs is assigned value 0; the input is removed if it is assigned value 1, an XOR gate changes to an NXOR gate, and an NXOR gate changes to an XOR gate. For an XOR gate with two inputs, and one of its inputs is assigned value 0, the gate is deleted from the circuit. For a two-input NXOR gate, the gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input XOR gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input NXOR gate can be removed from the circuit.

We first propose a new procedure to generate the weights of the test-enable signals for all scan chains in the LP DFT circuit after the degraded subcircuits for each subset of scan chains, which are driven by a single clock signal, have been produced. The i-controllability $C_i'(l)$ ($i \in \{0, 1\}$) of a node l is defined as the probability that a randomly selected input vector sets l to the value i. The observability $O'(l)$ is defined as the probability that a randomly selected input vector propagates the value of l to a primary output. The *signal probability* of a node is defined in the same manner as its 1-controllability measure.

In the scan-based BIST architecture, as shown in Fig. 2, different weights e_0, $e_1, \ldots,$ and e_k are assigned to the test-enable signals of the scan chains SC_0, $SC_1, \ldots,$ and SC_k, respectively, where $e_0, e_2, \ldots, e_k \in \{0.5, 0.625, 0.75, 0.875\}$. Scan flip flops in all disabled scan chains are set to constant values. Our method randomly assigns constant values to all scan flip flops in the disabled scan chains. The circuit is degraded into a smaller subcircuit. All weights on the test-enable signals are selected in the degraded subcircuit.

The gating logic is presented in Fig. 1. We do not assign weights less than 0.5 to the test-enable signals, because we do not want to insert more capture cycles than scan shift cycles. We have developed an efficient method to select weights

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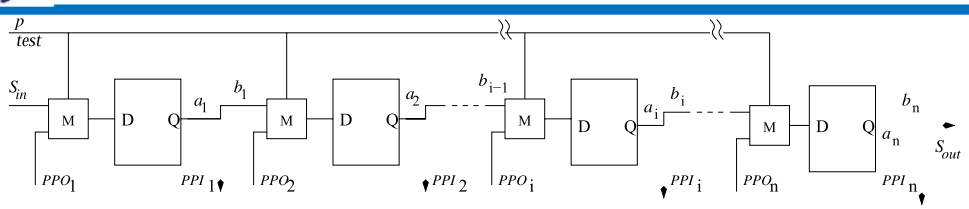


Fig. 3. Scan chain with a weighted test-enable signal.

for the test-enable signals of the scan chains. The selection of weights for the test-enable signals is determined by the following testability gain function:

$$G = \sum_{l/i \in F} \frac{|C_1'(l) - C_0'(l)|}{O'(l)} \tag{1}$$

where l/i represents the stuck-at i ($i \in \{0, 1\}$) fault at line l. In (1), F is the random-pattern-resistant fault set, defined as the set of faults whose detection probability is no more than ten times that of the hardest fault [6]. We attempt to minimize the testability gain function as given in (1).

Fig. 3 presents a scan chain with a weighted test-enable signal, where S_{in}, S_{out}, and test are the scan-in signal, scan-out signal, and the test-enable signal of the scan chain, respectively. Initially, all PPIs are assigned signal probability 0.5, and the observability of the pseudoprimary outputs (PPOs) is set to $1/n$. Let p be the selected weight of the test-enable signal, as shown in Fig. 3. Then

$$C_1'(\text{PPI}_i) = p \cdot C_1'(a_{i-1}) + (1 - p) \cdot C_1'(\text{PPO}_i). \tag{2}$$

The observability of PPO_i (PPO) can be estimated as follows:

$$O'(\text{PPI}_i) = (1 - p) \cdot O'(a_i) \tag{3}$$

$$O'(a_i) = 1 - (1 - O'(b_i)) \cdot (1 - O'(\text{PPI}_i)) \tag{4}$$

$$O'(b_{i-1}) = p \cdot O'(a_i). \tag{5}$$

The observability of the scan-out signal is set to 1. Even though the output of a scan chain is connected to the test response compactor, we can achieve zero aliasing by carefully connecting the scan chains to the XOR gates based on very simple structural analysis. We also have $O'(a_n) = 1$ and $C_0'(S_{\text{in}}) = C_1'(S_{\text{in}}) = 0.5$. Testability measures of the internal nodes, PPIs, and PPOs can be calculated iteratively using the controllability/observability program (COP) measures [11] and (2)–(5). We find that the testability measures for all nodes in the benchmark circuits converge within a few iterations.

The controllability of the PPI of the ith scan flip flop in a scan chain is set to 0.5, and the observability of the PPO of the ith scan flip flop is set to $1/d$, where d is the length of the scan chains. Iterative testability estimation is adopted for all nodes based on (2)–(5) and the COP measure. It is found that testability measures for all nodes become stable after a quite few rounds of testability calculation.

Separate weights from the set $\{0.5,\ 0.625,\ 0.75, 0.875\}$ are assigned to the test-enable signals of the scan chains. Algorithm 1 presents the details to select weights for all scan chains that are in the same scan chain subset. The inputs of Algorithm 1 are the scan chain set SC, which are partitioned into subsets $\{\text{SC}_0, \text{SC}_1, \ldots, \text{SC}_{k-1}\}$. Our method generates k degraded subcircuits for each scan chain subset $\text{SC}_i \in \{\text{SC}_0, \text{SC}_1, \ldots, \text{SC}_{k-1}\}$.

Algorithm 1 Select-Weights-for-Test-Enables()

Input:
The low-power BIST designed circuit;
Output:
Weights for the test-enable signals.
1: Assign the same values to the test-enable signals as the regular test-per-scan BIST scheme to all scan chains. Parttion the scan chains SC into k subsets $\{SC_0, SC_1, \ldots, SC_{k-1}\}$;
2: **while** the scan chain set $SC \neq \emptyset$ **do**
3: Select a scan chain subset SC_i from the scan chain set SC. Scan chains in SC_i are activated; $SC \leftarrow SC - \{SC_i\}$;
4: Randomly assign all PPIs related to all the disabled scan chains with constant values (1 or 0), and generate the degraded sub-circuit;
5: **for** each scan chain $C \in SC_i$ **do**
6: Assign each weight in $\{0.5,\ 0.625,\ 0.75,\ 0.875\}$ to the test-enable signal of scan chain C, testability estimation is adopted to evaluate the cost function as presented in Equation (1);
7: Randomly assign all PPIs related to all the disabled scan chains with constant values (1 or 0), and generate the degraded sub-circuit;
8: **end for**
9: For each scan chain, if no weight can be selected, simply leave its test-enable signal as the one in the conventional test-per-scan test scheme.
10: **end while**
11: Return the test pattern and the selected path set.

Our method selects a weight for the first scan chain test-enable signal to minimize the gain function. After the best weight has been selected for the first scan chain, a weight for the test-enable signal of the second scan chain is selected to minimize the cost function in (1). If no weight can be selected for any scan chain, our method sets its test-enable signal to the same value as the one in the conventional *test-per-scan* BIST scheme (the number of shift cycles is equal to the length of the scan chains, and a capture cycle follows). Continue the above process until appropriate weights have been chosen for all test-enable signals of the scan chains in SC_i.

The proposed DFT architecture, as shown in Fig. 1, has an implicit advantage over other BIST architectures [10]. Each stage of the PS drives a scan tree [57] instead of a single scan chain, while each stage of the PS requires a few number of XOR gates. In any case, flip flops of all disabled scan chains are assigned with specified values. Therefore, no unknown signals are produced to corrupt the compacted test responses kept in the MISR.

Fig. 2 presents a degraded subcircuit based on the proposed LP BIST method. PPIs corresponding to scan flip flops in all disabled scan chains are assigned with randomly selected constant values in the period of weighted pseudorandom test pattern application for the current subset of scan chains. The proposed LP weighted pseudorandom test pattern generation process is as follows. The first subset of scan chains is activated when all the remaining scan chains are disabled. The generated weighted pseudorandom pattern is applied to the degraded subcircuits if a scan chain is set to the capture cycle; otherwise, the scan chain is set to the scan shift mode. Our method turns to the next phase when the second subset of scan chains is activated after the given number of clock cycles. This process continues until all subsets of scan chains have been processed. The first subset of scan chains is again activated, and the above process is executed again. The process continues until the whole given number of clock cycles has run over.

The proposed LP weighted pseudorandom test generator is shown to be able to improve fault coverage compared with the conventional test-per-scan BIST approaches according to the experimental results presented in the experimental result section. The amount of test data to be stored on-chip is also significantly reduced.

IV. Low-Power Deterministic BIST

We use the same LFSR for both pseudorandom pattern generation and deterministic phases. First, we propose a new algorithm to select a proper primitive polynomial; after that the LP deterministic BIST and LP reseeding schemes are presented.

A. Selecting a Primitive Polynomial and the Extra Variable Number

Some extra variables are injected just like EDT [42]. We propose a new scheme to select the size of the LFSR and the number of extra variables simultaneously in order to minimize the amount of deterministic test data. Usually, a small LFSR constructed by a primitive polynomial is sufficient when a well-designed PS is adopted in the pseudorandom testing phase. In our method, a combination of a small LFSR and the PS from [41] is used to generate test patterns in the pseudorandom testing phase. The weighted test-enable signal-based pseudorandom test generator generates weighted pseudorandom test patterns. The size of the LFSR is not determined by the maximum number of care bits for any deterministic test vector. That is, the same LFSR is used for both phases.

For any degree less than 128, it is computationally feasible to generate enough primitive polynomials in reasonable time, out of which one (whose degree is equal to the maximum number of care bits in the deterministic vectors) can be selected to encode all deterministic test vectors. The tool that we used to generate primitive polynomials can only handle polynomials up to degree 128 of the word-length limit of the computer [40]. However, only very small LFSRs are used for all circuits according to all experimental results (no more than 30).

Algorithm 2 Primitive-Polynomial-and-Extra-Variable-Selection()

Input:
The primitive polynomial sets, two thresholds L_1 and L_2, the circuit, and the deterministic patterns;
The selected primitive polynomial.

Output:
The longest testable path for each transition on every node;

1: Let all primitive polynomials with degree i be kept in Q_i; $i \leftarrow 20$, $v \leftarrow 0$.
2: **while** $i \leq L_1$ **do**
3: Check whether the LFSR established by p with the extra variables can encode all deterministic vectors.
4: continue the above process until finding a primitive polynomial p that encode all deterministic test vectors; exit.
5: **for** each $p \in Q_i$ **do**
6: Check whether the LFSR established by p with the extra variables can encode all deterministic vectors.
7: Continue the above process until finding a primitive polynomial p that encode all deterministic test vectors; exit.
8: **if** no primitive polynomial with degree i has been found and $v \leq L_2$ **then**
9: $v \leftarrow v + 1$;
10: **end if**
11: **end for**
12: $i \leftarrow i + 1$;
13: **end while**
14: Return the selected primitive polynomial p and the number of extra variables.

This is mainly because we inject some extra variables to the LFSR. To encode a few deterministic test vectors with a large number of care bits, the injected extra variables and the seed kept in the LFSR are combined just like the EDT tool [42]. Therefore, it is not necessary to provide an LFSR whose size is at least the maximum number of care bits by injecting some extra variables unlike the previous methods [18], [19], [32], [56].

A well-designed LFSR is needed in order to encode all deterministic vectors after the pseudorandom testing phase. A new procedure is proposed to select a primitive polynomial with the minimum degree that can encode all deterministic test vectors for the hard faults. An efficient algorithm, as presented in Algorithm 2, is used to generate primitive polynomials of any desired degree. For any $i \leq 30$, assume that all primitive polynomials are kept in Q_i. As for $i > 30$, only a number of primitive polynomials are provided in Q_i. The following procedure returns a primitive polynomial with the minimum degree that encodes all deterministic vectors for the random-pattern-resistant (hard) faults.

Usually, the numbers of care bits of all deterministic test vectors is quite different. Therefore, it is recommended to use an LFSR, whose size is more than the maximum number of care bits $S_{\max}$ of all deterministic vectors. Unlike the method in [57], the new method selects a primitive polynomial of relatively low degree when some extra variables are injected into the LFSR. The commercial tool EDT [42] used similar technique to reduce the amount of test data stored in the on-chip ROM or automatic test equipment (ATE).

Algorithm 2 selects a primitive polynomial whose degree is not less than 20. The LFSR with no extra variables is

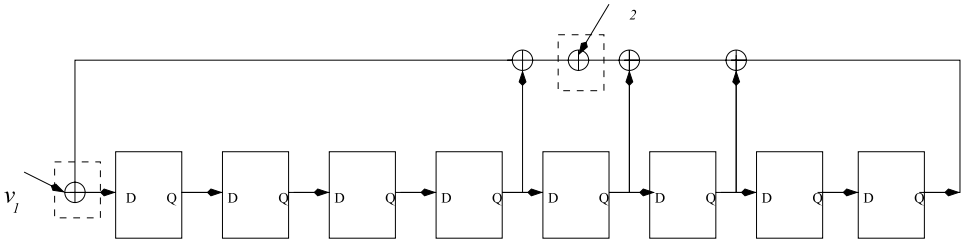


Fig. 4. LFSR with extra variables.

considered first. If the LFSR-based pseudorandom test generator cannot encode all deterministic vectors, we consider the case when a single extra variable is injected. If all deterministic test vectors still cannot be encoded, our method considers the case when two extra variables are injected. This process continues until the given number of extra variables L_2 have been considered. If the LFSR-based test generator still cannot encode all deterministic vectors, we consider the second primitive polynomial of degree i. Similarly, if all other primitive polynomials of degree i have been checked, and our method still cannot find a proper primitive polynomial, we check primitive polynomials of degree $i + 1$. This process continues until we find a primitive polynomial that can encode all deterministic vectors.

Fig. 4 presents an example eight-stage LFSR with two injected extra variables v_1 and v_2. The primitive polynomial for the LFSR is $x^8 + x^6 + x^5 + x^4 + 1$. The two extra variables are injected into the first stage, and the place between items x^4 and x^5. Certainly, implementation of the XOR network can be refined when the number of items is large enough in the primitive polynomial.

B. Low-Power Deterministic BIST and Reseeding

An effective seed encoding scheme is used here to reduce the storage requirements for the deterministic test patterns of the random-pattern-resistant faults. The encoded seed is shifted into the LFSR first. A deterministic test vector is shifted into the scan trees that are activated by the gating logic, where each scan-in signal drives a number of scan trees, and only one of the scan trees driven by the same scan-in signal is activated. The extra variables are injected into the LFSR when the seed is shifted into the activated scan trees. The gating logic, as shown in Fig. 1, partitions scan trees into multiple groups.

The first group of scan trees is disabled after they have received the test data. The second group of scan trees is activated simultaneously, and all other scan trees are disabled. The seed can be stored in an extra shadow register, which is reloaded to the LFSR in a single clock cycle. The scan shift operations are repeated when the extra variables are injected into the LFSR. This process continues until all scan trees have received test data.

The outputs of all scan chains, which are driven by the same clock signal, are connected to the same response compactor during the deterministic BIST phase. This offers additional flexibility for test encoding. The test responses of the previous test vector can be shifted out with only a few clock cycles (corresponding to the depth of the scan trees in the pseudorandom testing phase). For a scan chain architecture, the number of clock cycles needed to shift-out test responses of the previous deterministic test vector is much larger. The proposed LP tree-based architecture makes the reseeding scheme much easier to implement.

Let us describe the details about constructing the scan forest. Assume that the number of scan flip flops at each level in the same scan tree is l and the depth of the scan forest is d. For a given scan-in pin, l scan flip flops are selected among all scan flip flops for the first level of the scan tree. The routing overhead is minimized when constructing the scan trees, which can be easily estimated using tools, such as *Astro* from synopsys [4]. Experimental results reported in this paper were obtained using the *Astro* tool. All scan flip flops at the same level in the same scan tree meet the following condition. Each pair of scan flip flops has no combinational successor in the circuit [57]. Each scan flip flop p at the first level of the scan tree is connected to a scan flip flop f at the second level that has the minimum distance from p among all scan flip flops that can be placed at the second level of the scan tree, where all scan flip flops at the second level of the same scan tree have no common combinational successor. Repeat the above process until the scan trees have been constructed. It is not necessary for scan flip flops at the same level of the same scan tree to be in the neighborhood.

Let L, i, v, and $S_{\max}$ be the size of the LFSR, the number of consecutive cycles to inject the extra variables, the number of extra variables, and care bits, respectively. Assume that the number of care bits for all scan chains at level k is b_k, and the total number of injected extra variables after j shift cycles is V_j. The necessary conditions to encode all deterministic vectors [18], [27] can be stated as follows: 1) $L + i \cdot v \geq S_{\max}$ and 2) $\sum_{k=d-1}^{k=d-1-j} b_k \leq (L + V_j)$.

The summation of the size of the LFSR and the total number of extra variables injected into the LFSR must be at least the maximum number of care bits of the deterministic vectors. Therefore, the condition $L + i \cdot v \geq S_{\max}$ must be satisfied. At any clock cycle, the summation of the size of LFSR and the whole number of injected extra variables must be greater than the total care bits in the scan flip flops that have been shifted test data in the process of test application. The condition $\sum_{k=d-1}^{k=d-1-j} b_k \leq (L + V_j)$ must be satisfied in order for the linear equations to be solvable.

As shown in Fig. 1, the signals A_1, $A_2, \ldots,$ and A_k drive all subsets of scan trees in capture cycles while

B_1, B_2, . . . , and B_k drive all subsets of scan trees in the shift cycles. The signals R'_1, R'_2, . . . , and R'_k are outputs of the multiplexers. One input of each multiplexer is the original functional clock signal that drives all scan trees of the whole test period.

We propose an LP deterministic BIST scheme with reseeding. The deterministic test vectors for the random-pattern-resistant faults are ordered according to the number of care bits. Our method partitions all scan chains into multiple subsets, while only one subset of scan trees is activated at any clock cycle. The gating logic controls the whole test application process. The first deterministic test vector is shifted into all scan trees as follows. The seed is first shifted into the LFSR. The extra variables with calculated values are injected into the LFSR when the seed is applied to the first subset of activated scan trees. The same values on the extra inputs are delivered after the same seed is loaded to the LFSR again for the second subset of activated scan trees. This process continues until all scan trees have received the test vector.

The capture process starts after the LP shift period. The first subset of scan trees captures test responses when all other scan trees are disabled. The seed is loaded to the LFSR, and the extra variables with the calculated values are injected again simultaneously in order to fill the deterministic test vector again. This can be implemented by using the shadow register of the same size as the LFSR to store the seed, as shown in Fig. 1. The captured test responses are shifted into the MISR when refilling the test vector. After the activated subset of scan trees has been refilled with the test vector, the second activated subset of scan trees captures test responses. This process continues until all scan trees have captured test responses. The captured test responses of the last subset of scan trees are shifted out when the second test vector is shifted into this subset of scan trees.

Our method turns to the reseeding process. The final values in the LFSR remain unchanged. The activated subset of scan trees performs d shift cycles when the extra variables with the same values are injected. The second subset of activated scan trees performs d shift cycles when the same values of the extra variables are injected. This process continues until the values of the extra variables have been shifted into all scan trees. Our method begins to check the values of the scan trees to see whether they are compatible with any remaining deterministic test vector. If so, the test vector is deleted from the ordered test sequence, and another LP capture period is applied as stated earlier from this state.

If the values kept in the scan chains are compatible with a deterministic vector, our method continues the responses capturing process. Assume that the initial values kept in the LFSR are stored in the shadow register. The first subset of scan trees is activated, which captures the test responses. The values kept in the shadow register are reloaded to the LFSR. The values of the extra variables are injected again when activated scan trees are filled. The above process continues until all scan trees have captured test responses.

If the values kept in the scan flip flops are incompatible with any other deterministic test vector, our method starts another LP shift-in period when injecting the extra variables that are stated earlier. The reseeding process continues until the given number of reseeding processes has been completed. In each round of the reseeding processes, the states of the scan trees are checked to see whether they are compatible with any deterministic test vector. If so, the deterministic vector is deleted.

Our method copes with the second deterministic vector after the reseeding processes have been completed. The whole reseeding process is the same as the one described earlier. This reseeding process continues until all deterministic test vectors have been proceeded.

TABLE I

STATISTICS OF THE CIRCUITS

circuits	gates	FFs	PIs	POs
s38417	23817	1636	28	106
b19	225800	6642	24	30
wb_conmax	46778	770	1129	1416
usb_funct	16401	1656	104	19
pci_bridge	32381	3359	160	207
des_perf	107378	8746	233	64
ethernet	115925	10554	94	115
vga_lcd	170743	17079	87	109
netcard	568986	97796	15	56

TABLE II

FAULT COVERAGE COMPARISON OF THE LP WEIGHTED PSEUDORANDOM TEST GENERATOR

-	The Proposed Method				[10]			
circuits	FC	FC(10)	FC(20)	FC(30)	FC	FC(10)	FC(20)	FC(30)
s38417	99.165	99.053	99.077	99.107	97.879	97.365	97.561	97.613
b19	84.832	84.332	84.645	84.679	83.237	82.859	82.883	82.994
wb_conmax	93.527	93.266	93.437	93.471	91.793	91.412	91.486	91.506
usb_funct	92.811	92.742	92.787	92.798	92.016	91.621	91.795	91.814
pci_bridge	95.447	95.003	95.224	95.287	94.841	94.597	94.772	94.768
des_perf	96.901	96.887	96.889	96.892	95.396	95.013	95.175	95.223
ethernet	96.318	96.089	96.117	96.226	95.904	95.457	95.682	95.726
vga_lcd	92.031	91.683	91.778	91.859	91.303	90.768	90.917	91.162
netcard	95.194	93.982	94.337	94.756	94.546	93.349	93.651	94.173

V. EXPERIMENTAL RESULTS

The proposed method has been implemented and evaluated on a Dell Precision 7810 workstation. The pseudorandom testing phase was used with the scan-forest scan architecture, and separate weighted test-enable signals were assigned to the scan chains. A very small number of scan-in pins were used, making the size of the PS very small. That is, the area overhead can be reduced significantly.

Table I presents the statistics of the benchmark circuits used for experiments. We used the ISCAS89 circuit s38417, the largest ITC99 circuit b19, the IWLS2005 circuits wb_conmax, usb_funct, pci_bridge, des_perf, ethernet, vga_lcd, and the open core netcard. The columns labeled FFs and gates show the number of flip flops and the number of gates in a circuit. The academic compact ATPG tool for single stuck-at faults, which is developed in our group, was used to generate test vectors for the random-pattern-resistant faults after the LP pseudorandom testing phase. The Synopsys commercial tool Astro [4] was used to construct the connection-overhead-aware DFT architecture to reduce the connection overhead.

Performance comparison for the proposed LP BIST scheme and the one in [10] is presented in Table II on the fault coverage of the pseudorandom test generators. The column FC shows the fault coverage of the original weighted

TABLE III

PERFORMANCE COMPARISON OF THE PROPOSED LP BIST APPROACH WITH THE PREVIOUS METHOD

-	The Proposed Method							[10]				
circuits	LFSR	lev	vec.	ROM	PC_1	MAX	PC_2	RG	lev	vec.	ROM	MAX
s38417	22	10	3	105	3.1	25	3.6	32	10	7	3417	691
b19	22	10	384	52762	3.3	121	3.0	32	10	428	1578139	4085
wb_conmax	24	10	21	2154	18.8	95	18.8	32	10	27	11436	473
usb_funct	21	10	40	1458	5.5	37	5.5	32	10	45	26499	673
pci_bridge	20	10	20	804	4.4	43	4.2	32	10	22	18480	1021
des_perf	21	6	6	89	0.2	12	0.2	32	6	9	43640	4980
ethernet	26	16	63	21636	22.2	523	26.0	32	16	71	97321	2011
vga_lcd	22	12	186	30504	3.4	244	3.8	32	12	204	897136	6397
netcard	23	10	173	49764	3.8	379	3.9	32	10	192	1314378	9843

TABLE IV

PERFORMANCE OF THE LP DETERMINISTIC BIST APPROACH WITH RESEEDING

circuits	vec.	ROM(bits)	reseed(10)	reseed(20)	reseed(30)	reduction rate(%)	AO	CO
s38417	3	105	105	105	80	76.2	1.1	3.3
b19	384	52762	48852	45320	42470	81.1	2.2	7.3
wb_conmax	21	2154	1876	1751	1542	72.5	2.8	9.7
usb_funct	40	1458	1306	1192	988	67.6	2.1	5.6
pci_bridge	20	804	724	606	534	66.2	3.5	8.8
des_perf	6	89	89	75	64	71.4	1.8	7.4
ethernet	63	21636	19580	17150	15874	73.6	1.3	3.2
vga_lcd	186	30504	28446	24928	22632	74.8	2.2	8.7
netcard	173	49764	43208	41386	39462	79.3	2.1	7.9

pseudorandom test generator. The columns FC(10), FC(20), and FC(30) present the fault coverages of the proposed LP BIST method after 500k clock cycles, where the number given in the bracket shows the percentages of the activated scan flip flops for the proposed LP BIST method and the one presented in [10].

Table III further presents performance comparison of the proposed LP pseudorandom test generator with the method in [10]. Columns LFSR, lev, and ring generator (RG) present the size of the LFSR, the depth of the longest scan trees (the method in [10] provides the same scan-chain length for fair comparison), and the number of stages of the ring generator used by the method in [10]. The number of scan chains for the method in [10] is far more than that of the new method, therefore, the size of the RG is a little larger than that of the LFSR size of the new method. Columns PC_1 and PC_2 present the percentages of ROM bits and the maximum care bits compared with the method in [10].

Columns vec., ROM, and MAX, as shown in Table III, give the number of deterministic vectors after the LP pseudorandom pattern generation phase, the amount of ROM (bits) to keep the on-chip seeds when 10% scan chains are activated, and the number of the maximum care bits for the deterministic vectors. Experimental results show that the proposed LP BIST scheme obtains slightly better fault coverage for all circuits than [10] in all cases because of the proposed LP weighted test-enable signal-based pseudorandom test pattern generator. The required amount of ROM bits to store the seeds for the proposed method is also much less than that for [10] in almost all cases.

The HOPE tool [31] was used for fault simulation in this paper on the separate degraded subcircuits by combining with the compact ATPG tool for the deterministic test vectors of the random-pattern-resistant faults. It is found that the number of deterministic vectors is very low for both methods. However, the numbers of maximum care bits for the deterministic vectors are quite different, which make the final amount of bits for the seeds to be stored on-chip quite different. This is mainly because the test data are well-compressed by the scan-forest architecture used in the new method.

The size of the ring generator for all circuits was set to 32, as shown in Tables II and III. Considering the circuit s38417, both LP BIST methods do not introduce apparent coverage loss. The new method obtains more than 1% coverage improvement. The test generator gets small test sets for random-pattern-resistant faults of both methods. However, the final amount of ROM (bits) is 105 and 3417, respectively, because the maximum care bits of the deterministic vectors for both methods are 25 and 691, respectively.

As for the circuit netcard, both LP BIST methods reach 93.98% and 93.35% fault coverage when only 10% scan chains are activated. The numbers of the deterministic test vectors for both methods are 173 and 192, respectively, and the final amount of on-chip data for the seeds is reduced approximately 26.8 times. It is shown that the number of maximum care bits of the deterministic vectors for both methods are 379 and 9873, respectively, which makes the amount of seeds to be kept on-chip completely different

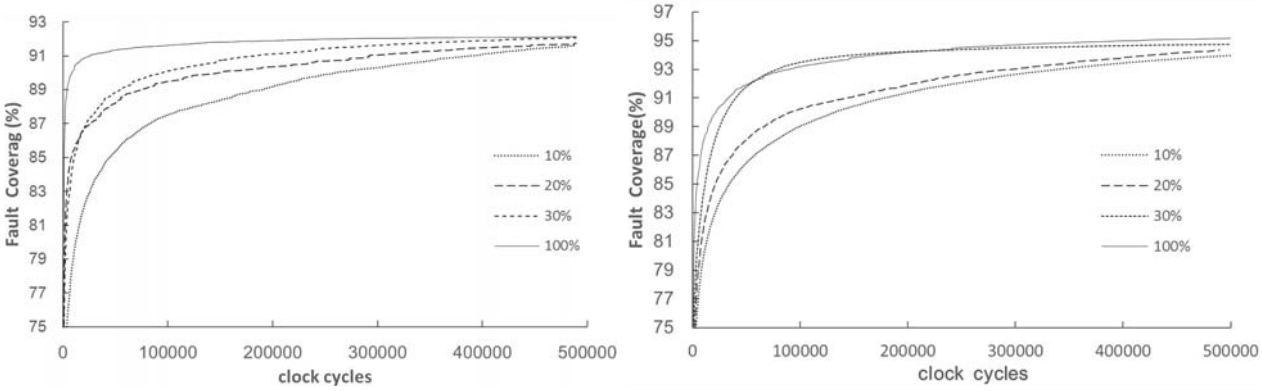
$$\text{CO} = \frac{\text{wl(lpbist)} - \text{wl(orig.)}}{\text{wl(orig.)}} \times 100\% \quad (6)$$

$$\text{AO} = \frac{\text{area of lpbist} - \text{area of the orig. cir.}}{\text{area of orig. cir.}} \times 100\%. \quad (7)$$

Equations (6) and (7) present the connection and area overheads of the proposed method by using a commercial tool Astro to estimate the wire length. Results on the connection overhead and area overhead are obtained based on the 65-nm TSMC cell library. The supply voltage is set to 1.5 V, and the frequency for scan-based BIST is set to 200 MHz. The connection overhead of the new method compared with the original multiple scan chain design is given in the column CO in Table IV. The connection overhead of the proposed method is no more than 10% for all circuits, and the area overhead for all circuits is no more than 3.5%, as shown in Table IV.

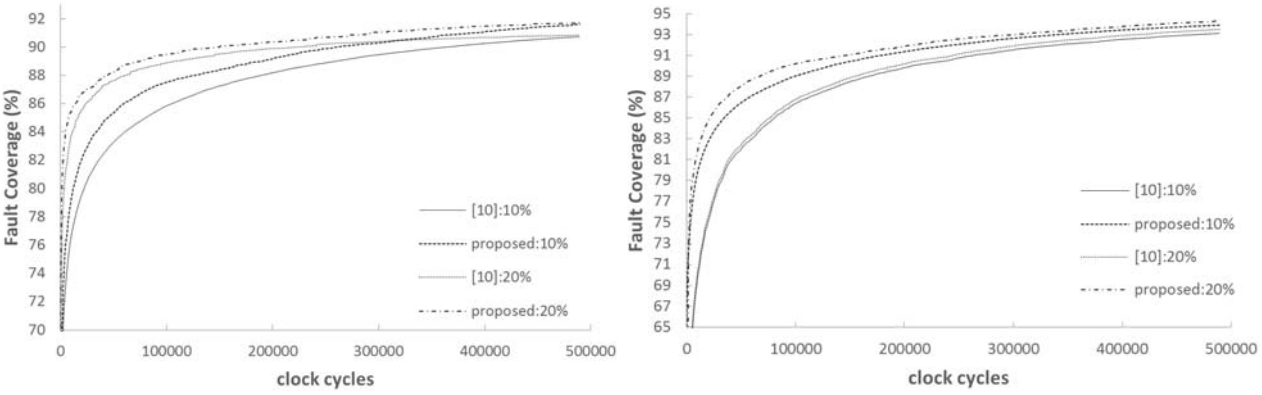
Table IV presents the performance of the proposed LP deterministic and the reseeding scheme when the number of reseeding processes is set to 10, 20, and 30, respectively. The results are presented in the columns reseed(10), reseed(20), and reseed(30), respectively. The number of ROM bits can be apparently reduced. The column reduction rate (%) presents the percentage of ROM (bits) reduction.

Fig. 5 presents the performance of the proposed LP PRPG for circuits netcard and vga when different percentages (10%, 20%, 30%, and 100%) of scan chains are activated. It is shown that the fault coverage is less when fewer scan chains are activated. Finally, the fault coverages for all four cases are quite close after 500 000 clock cycles. In a few cases, the fault coverage with 30% activated scan chains is slightly more than that with 100% activated scan chains for the circuit netcard. This anomaly also occurs for the circuit vga, as shown in Fig. 5(a). The cases for the circuit netcard are quite similar, as shown in Fig. 5(b).



(a) (b)

Fig. 5. Fault coverage with different toggle rates. (a) vga_lcd. (b) Netcard.



(a) (b)

Fig. 6. Performance comparison of the proposed LP PRPG with [10]. (a) vga_lcd. (b) Netcard.

TABLE V
POWER REDUCTION

-	low-power deterministic BIST			low-power PRPG		
circuits	peak(mW, before)	lp peak(mW, after)	rate(%)	peak(mW, before)	lp peak(mW, after)	rate(%)
s38417	6724	643	9.6	7695	704	9.1
b19	41933	5660	13.4	45334	5779	12.7
wb_conmax	10299	1111	10.8	11197	1255	11.2
usb_funct	6261	610	9.7	6342	639	10.1
pci_bridge	8119	984	12.1	8783	1014	11.5
des_perf	22771	2181	9.5	25552	2398	9.4
ethernet	28865	3746	12.9	29331	3823	13
vga_lcd	46372	4775	10.2	47432	4396	9.3
netcard	95165	9426	9.9	103676	9970	9.6

Fig. 6 presents the performance comparison of the proposed LP PRPG with the previous LP BIST scheme in [10] for circuits netcard and vga when different percentages (10% and 20%) of scan chains are activated. It is shown that the proposed method obtains better fault coverage in all cases when the number of clock cycles increases. The coverage difference for the circuit vga is still about 1% when the number of clock cycles has reached 500 000, as shown in Fig. 6(a). As shown in Fig. 6(b), the new method obtains apparently better fault coverage in all cases when the number of clock cycles increases.

Table V presents the performance of the proposed LP deterministic BIST scheme on peak power (milli-Watt, mW) reduction when 10% scan chains are activated. The supply voltage and frequency are set to 1.5 V and 200 MHz, respectively. The column's peak (mW, before) and lp peak (mW, after) show the peak power for the original deterministic BIST and weighted test-enable-based PRPG, and the proposed LP BIST method. The column rate(%) shows the percentage of peak power for the proposed method compared with the one without the LP design for both the weighted pseudorandom test generation phase and the deterministic BIST phase. Experimental results in Table V show that the proposed LP PRPG phase reduces the peak power to less than 13% for all circuits, and the LP deterministic BIST scheme reduces the peak power to less than 14% in all cases. Experimental results show that the peak power for the PRPG phase is a little more than that for the deterministic BIST phase for the all circuits except s38417 before the LP design is included. This is mainly because only 10% flip flops are activated in any case during the LP weighted pseudorandom testing and the LP deterministic BIST phases, as shown in Fig. 1.

VI. Conclusion

A new LP BIST method has been proposed using weighted test-enable signal-based pseudorandom test pattern generation and LP deterministic BIST and reseeding. The new method consists of two separate phases: 1) LP weighted pseudorandom pattern generation and 2) LP deterministic BIST with reseeding. The first phase selects weights for test-enable signals of the scan chains in the activated subcircuits. A new procedure has been proposed to select the primitive polynomial and the number of extra inputs injected at the LFSR. A new LP reseeding scheme, which guarantees LP operations for all clock cycles, has been proposed to further reduce test data kept on-chip. Experimental results have demonstrated the performance of the proposed method by comparison with a recent LP BIST method [10]. The LP reseeding technique is a little more complicated. This work can be extended to latch-on-capture transition fault testing and small delay defect testing [12]–[14], [59]–[61].

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