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Design of 3t Gain-Cell for Low-Voltage Low-Power Applications

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Abstract

Logic compatible gain cell (GC)-embedded DRAM (eDRAM) arrays are considered an alternative to SRAM due to their small size, nonratioed operation, low static leakage, and two-port functionality. However, traditional GC-eDRAM implementations require boosted control signals in order to write full voltage levels to the cell to reduce the refresh rate and shorten access times. These boosted levels require either an extra power supply or on-chip charge pumps, as well as nontrivial level shifting and toleration of high voltage levels. In this brief, we present a novel, logic compatible, 3T GC-eDRAM bitcell that operates with a single-supply voltage and provides superior write capability to the conventional GC structures. The proposed circuit is demonstrated with a 2-kb memory macro that was designed and fabricated in a mature 0.18-μm CMOS process, targeted at low-power, energy-efficient applications. The test array is powered with a single supply of 900 mV, showing a 0.8-ms worst case retention time, a 1.3-ns write-access time, and a 2.4-pW/bit retention power. The proposed topology provides a bitcell area reduction of 43%, as compared with a redrawn 6-transistor SRAM in the same technology, and an overall macro area reduction of 67% including peripherals.

Keywords:- Access speed, data retention time, embedded DRAM, gain cell, low power operation

1. INTRODUCTION

In recent years, memories have occupied increasingly large portions of the die area of VLSI systems-on-chip (SoCs), in general, and of microprocessors, in particular, as shown in. This is due to the large 6-transistor (6T) SRAM bitcell and its area-consuming peripheral circuitry that are the basis for the vast majority of these. In addition, the standby power of ultralow-power (ULP) systems, such as biomedical implants and wireless sensor networks, is often dominated by embedded memories, which continue to leak during the long retentive standby periods that characterize these systems. The 6T SRAM has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free static data retention. However, the 6T bitcell has several drawbacks in modern systems, including its large transistor count, its impeded

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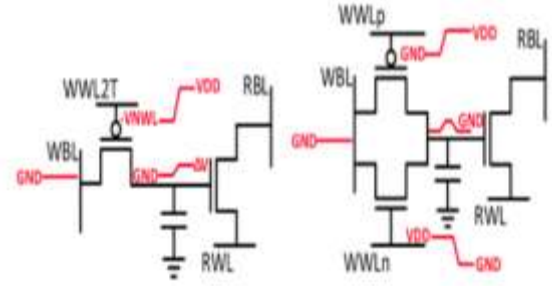
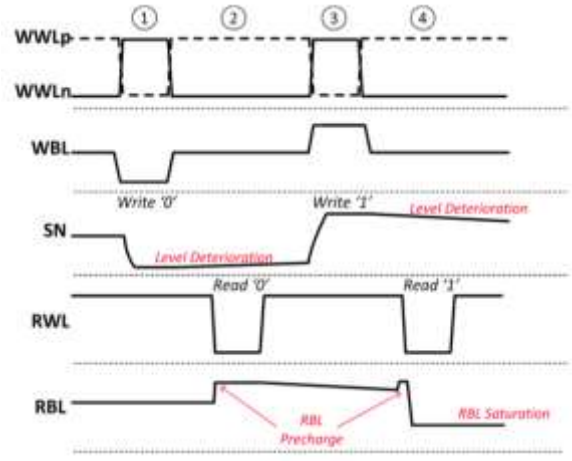
functionality under voltage scaling, and the aforementioned static leakage currents from the supply voltage (VDD) to GND. One of the interesting alternative implementations that addresses these limitations, while continuing to provide full CMOS logic compatibility, is gain-cell (GC)-embedded DRAM (eDRAM), such as the circuit shown in Fig. 1(a) . Most often consisting of 2-transistor (2T) or 3-transistor (3T), GC-eDRAMs provide a reduced silicon footprint, along with inherent two-port functionality, nonratioed circuit operation, and very low static leakage currents from VDD to GND. However, as opposed to static memories, such as SRAM, the data retention of GC-eDRAM depends on dynamically stored charge, and thereby requires periodic, power-hungry refresh operations. The data retention time (DRT) of GC-eDRAMs is the time interval from writing a data level into the bitcell to the last moment at which one can still correctly read out the stored information.



The DRT is primarily limited by the initial charge stored on the internal bitcell capacitance and the leakage currents that degrade the stored voltage level over time. For traditional 2T and 3T cells, the DRT is significantly affected by the initially degraded voltage level corresponding to data 0 or 1, due to the threshold voltage (VT) drop across the write transistor [MW in Fig. 1(a)].



In order to address this problem, a boosted write word line (WWL) voltage is usually employed to pass a full swing level to the storage capacitance. However, this requires

the generation of a boosted on-chip voltage, which entails substantial overhead [6]. The magnitude of the voltage boost is set not only to overcome the VT drop, but also to achieve short write-access times, which otherwise are typically longer than for 6T SRAM implementations. Furthermore, charge injection (CI) and clock feedthrough (CF) during WWL signal deassertion cause a voltage step at the storage node (SN), resulting in an initially degraded level at the end of a write access. As this undesired coupling even increases with WWL boost magnitude, a clear tradeoff between write speed, power, and DRT is introduced. In addition, the level-shifting and toleration of higher than nominal voltages can be complex, especially when this boosted voltage is a negative underdrive voltage, as required by implementations employing a pMOS MW. The propagation of such a negative voltage can easily lead to voltage drops over device terminals that violate the technology limitations.

2. SIMULATION IMPLEMENTATION

3T Gain-Cell Structure

The circuit comprises a write port featuring a complementary TG PMOS Write (PW) and NMOS Write (NW), a read port based on an nMOS device (NR), and a SN composed of the parasitic capacitance (CSN) of the three devices and the stacked metal interconnect. The cell is built exclusively from standard VT transistors and is fully compatible with standard digital CMOS technologies. The gates of PW and NW are connected to the complementary word lines, WWLp and WWLn. A common write bit line (WBL) is used to drive data through the TG during write operations. The full-swing passing capability of the TG enables the propagation of strong levels to the SN without the need for a boosted word line. Read is performed by precharging the read bit line (RBL) and subsequently driving the read word line to GND, thereby conditionally discharging the RBL capacitance if the SN is high (data 1) or blocking the discharge path if the SN is low (data 0). To achieve a reasonable tradeoff between speed, area, power, and reliability, a dynamic sense inverter is used on the readout path (Section III-A). However, other sense amplifiers can be used for improved read performance, such as demonstrated.

3T Gain-Cell Operation

Demonstrates bitcell operation through the application of subsequent write and read operations of both data values with VDD =

900 mV. This supply voltage was chosen as a good median voltage between VDD and VT, as previously shown to be DRT efficient in GC-eDRAM design. Starting with a charged CSN, WBL is driven low and the word lines are asserted (WWLp= 0 and WWLn = VDD). As expected, a strong 0 level is passed to the SN, and this level is retained with the deassertion of the word lines due to the opposing CI and CF effects from the PW and NW transistors. During standby, the level on SN deteriorates due to leakage currents, dominated by the sub-VT leakage of NW and PW in mature CMOS nodes. Therefore, in order to extend the retention time, WBL is driven to VDD/2 during standby and read cycles, thereby significantly reducing the sub-VT leakage through the TG, for both stored data 0 and 1, compared with the case where WBL is driven to either VDD or GND. The WBL biasing circuitry is described in. During readout the 0 level blocks the discharge path through NR, maintaining the precharged voltage on RBL. During the next write operation WBL is driven high, resulting in a strong 1 stored on the SN. The subsequent read operation provides a strong gate overdrive to transistor NR, thereby discharging RBL to read a 1. It should be noted that during this operation (Read 1), bitcells storing 1 and sharing the same column turn on when RBL discharges by more than the VT of NR, causing it to saturate before it can completely discharge. This phenomenon is common to many GC-eDRAM configurations, as discussed in.

3. SIMULATION RESULTS

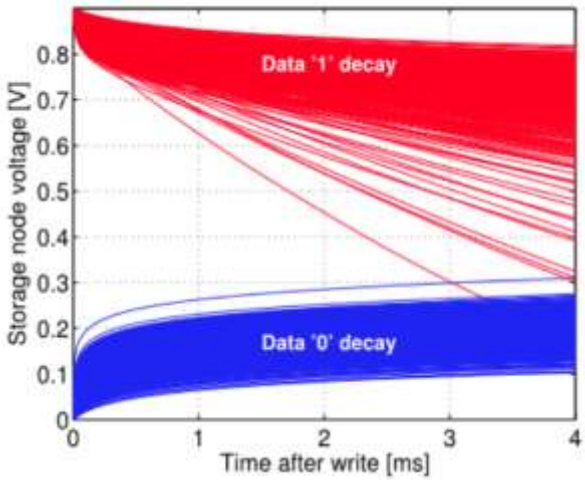


Fig:-3 SN degradation with worst case bias conditions.

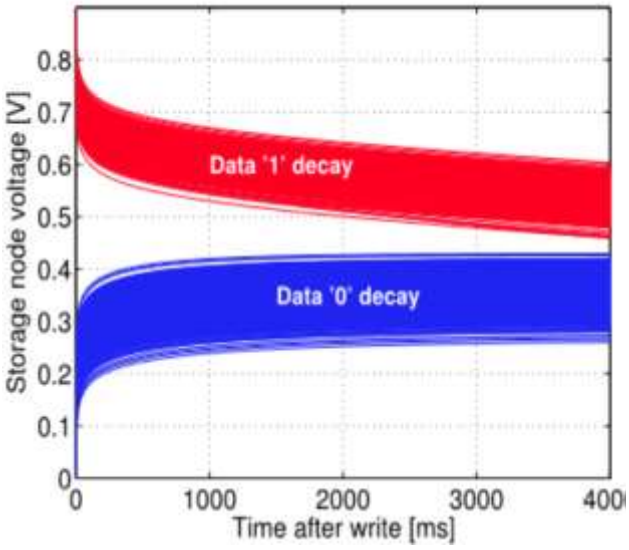


Fig:-4 SN degradation with VDD/2 WBL biasing

4. CONCLUSION

This brief proposes a novel 3T GC eDRAM macrocell targeted at ULP systems and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations. The proposed cell exhibits faster write-access than conventional GC circuits, while minimizing CI and CF through effects, thereby increasing DRTs and reducing refresh power consumption. The cell area is only 57% of a redrawn 6T SRAM in the same technology, making it a suitable alternative to SRAM for low-power memories. A test-chip containing a 2-kb memory macro based on the proposed 3T GC was fabricated in a mature 0.18-µm CMOS technology and several chips were tested. Measurement results show full functionality at voltages ranging from 600 mv to 1.8 V with retention power as much as 17×lower than a previously reported 6T SRAM in the same technology node.

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